## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>01/18/12</td>
<td>13.4</td>
<td>Initial version. <a href="#">AR45653</a> (Rev 2) applied.</td>
</tr>
</tbody>
</table>

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Overview

- Xilinx KC705 Board
- Software Requirements
- KC705 Setup
- KC705 BIST (Built-In Self Test)
- Compile KC705 BIST Design
- References

Note: This presentation applies to the KC705
**KC705 BIST Design Description**

- **Description**
  - The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

- **Reference Design IP**
  - EDK IP: MicroBlaze, axi_interconnect, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, axi_bram_ctrl, axi_uart16550, axi_ethernet, axi_dma, axi_gpio, clock_generator, axi_7series_ddrx, proc_sys_reset, axi_intc, axi_timer, axi_iic, axi_emc, axi2axi_connector

- **Reference Design Source**
  - rdf0102.zip
Xilinx KC705 Board

Note: Presentation applies to the KC705
ISE Software Requirement

- Xilinx ISE 13.4 software

Note: Presentation applies to the KC705
EDK Software Requirement

- Xilinx EDK 13.4 software

Note: Presentation applies to the KC705
EDK Software Requirement

- Xilinx SDK 13.4 software

*Note: Presentation applies to the KC705*
KC705 Setup

- Connect a USB Type-A to Mini-B cable to the USB UART connector on the KC705 board
  - Connect this cable to your PC
  - Power on the KC705 board for UART Drivers Installation
KC705 Setup

- **Install USB UART Drivers**
  - CP210x VCP Win XP S2K3 Vista 7.exe

*Note: Presentation applies to the KC705*
KC705 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager

Note: Presentation applies to the KC705
KC705 Setup

- Expand the Ports Hardware
  - Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties

Note: Presentation applies to the KC705
KC705 Setup

- Under Port Settings tab
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4

Note: Presentation applies to the KC705
KC705 BIST Setup

- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to 9600

Note: Tera Term may need to be restarted if the serial cable is disconnected
Hardware Setup

- **Set S13 to 11010 (1 = on, Position 1 → Position 5)**
  - This enables Master BPI configuration from the Linear Flash
    - Flash A25, A24 = 11
    - FPGA mode pins M[2:0] = 010

**Note:** Presentation applies to the KC705
KC705 BIST

- View initial BIST screen

**Note:** Presentation applies to the KC705
KC705 BIST

- **UART Test**
  - Type “1” to start the UART Test
  - After each test, press any key to return to the main menu

Note: Presentation applies to the KC705
KC705 BIST

- LED Test
  - Type 2 to begin LED Test

- View Walking 1’s pattern on GPIO LEDs
  - Sequence repeats twice

Note: Presentation applies to the KC705
KC705 BIST

- **IIC Test**
  - Type 3 to begin IIC Test

**Note:** Presentation applies to the KC705
KC705 BIST

- **Timer Test**
  - Type 4 to begin Timer Test

![Screenshot of Tera Term VT window with test results]

**Note:** Presentation applies to the KC705
KC705 BIST

- **Rotary Test**
  - Type 5 to begin Rotary Test
  - Turn the rotary switch (under the LCD) back and forth

Note: Presentation applies to the KC705
KC705 BIST

- **GPIO Switch Test**
  - Set 4-position GPIO DIP Switch (SW4)
  - Type 6 to begin GPIO Switch Test
    - Reads switch settings

![Image of Tera Term VT window with test options]

*Note:* Presentation applies to the KC705
- LCD Test
  - Type 7 to begin LCD Test

Note: Presentation applies to the KC705
External Memory Test

- Type 8 to begin External Memory Test

Note: Presentation applies to the KC705
**KC705 BIST**

- **Internal Memory Test**
  - Type **9** to begin BRAM Memory Test

![Terminal Output]

**Note:** Presentation applies to the KC705
KC705 BIST

- **Ethernet Test**
  - Type A to begin Ethernet Test

![Tera Term VT window](img.png)

**Note:** Presentation applies to the KC705
- **Button Test**
  - Type **B** to begin Button Test

Note: Presentation applies to the KC705
Compile KC705 BIST Design
Compile KC705 BIST Design

- Unzip the KC705 BIST Design Files (13.4 CES)
  - Available through http://www.xilinx.com/kc705

Note: Presentation applies to the KC705
Compile KC705 BIST Design

- If desired, FPGA compile can be skipped by opening SDK directly:
  Start → All Programs → Xilinx ISE Design Suite 13.4 →
  EDK → Xilinx Software Development Kit

- Select the workspace: <design files>\SW\SDK
- Go to SDK Software Compile
Compile KC705 BIST Design

- Open XPS project `<project directory>\system.xmp`
- Create the hardware design, system.bit, located in `<project directory>/implementation`
  - Click the **Generate Bitstream** button (1)
  - Or from the menu, select **Hardware** → **Generate Bitstream**

**Note:** Presentation applies to the KC705
Launch KC705 Design in SDK

- Open SDK
  - Click the **Export Design** button (1)
  - Click **Export & Launch SDK** (2)

**Note:** Presentation applies to the KC705
Compile KC705 Software in SDK

- **SDK Software Compile - Build ELF files in SDK**
  - Select **Project → Build All** (1)
  - **Note:** If by-passing the FPGA compile, the ELF files are already built; if desired, the ELF files can be re-built by selecting **Clean...** followed by **Build All**.
Program KC705 with BIST Design
KC705 Setup

- Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board
  - Connect this cable to your PC
Program KC705 with BIST Design

- **Init memory with the Bootloop ELF**
  - Update the bitstream (download.bit) with the Bootloop ELF
  - Select **Xilinx Tools → Program FPGA** (1)
Program KC705 with BIST Design

- **Init memory with the Bootloop ELF**
  - Select **bootloop** (1)
  - Click **Program**

*Note: Presentation applies to the KC705*
Program KC705 with BIST Design

- Launch XMD
  - Select Xilinx Tools → XMD Console (1)
Program KC705 with BIST Design

- **Connect XMD to the MicroBlaze:**
  
  cd C:/kc705_bist/SW/SDK
  
  connect mb mdm
Program KC705 with BIST Design

- Download the BIST Application with xmd:
  dow bist_app/Debug/bist_app.elf
Program KC705 with BIST Design

- Download the BIST Application with xmd:
  
  run
Program KC705 with BIST Design

- BIST Application runs in the terminal window

Note: Presentation applies to the KC705
Program KC705 with BIST Design

- Init memory with the BIST Application ELF
  - Update the bitstream (download.bit) with the BIST Application ELF
  - Select **Xilinx Tools → Program FPGA** (1)
Program KC705 with BIST Design

- Init memory with the BIST Application ELF
  - Select `bist_app.elf` (1)
  - Click Program

Note: Presentation applies to the KC705
Program KC705 with BIST Design

- BIST Application runs in the terminal window

** Xilinx Kintex-7 FPGA KC705 Evaluation Kit **

Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
4: FLASH Test
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit

Note: Presentation applies to the KC705
References
References

- **EDK Documentation**
  - Embedded System Tools Reference Guide

- **7 Series Configuration**
  - 7 Series FPGAs Configuration User Guide
Documentation

- **Kintex-7**
  - Kintex-7 FPGA Family

- **KC705 Documentation**
  - Kintex-7 FPGA KC705 Evaluation Kit
  - KC705 Getting Started Guide
  - KC705 User Guide
  - KC705 Reference Design User Guide