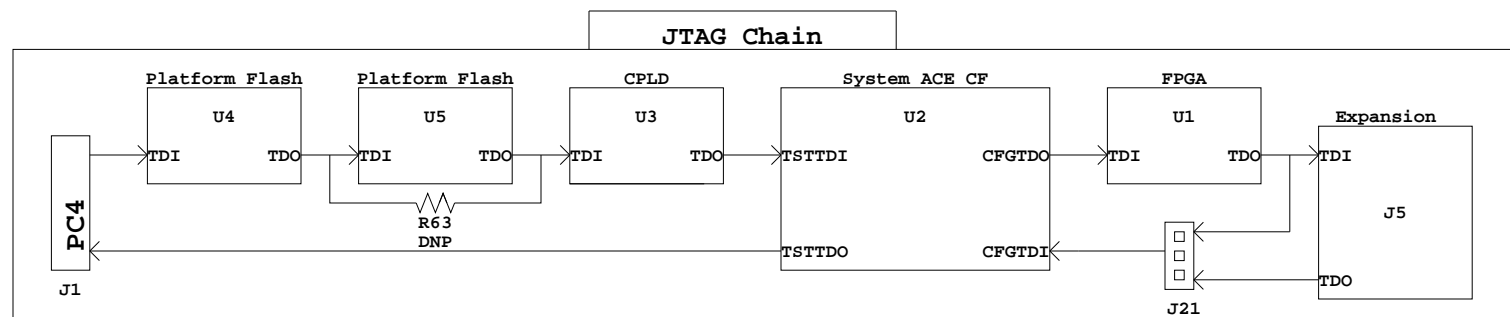
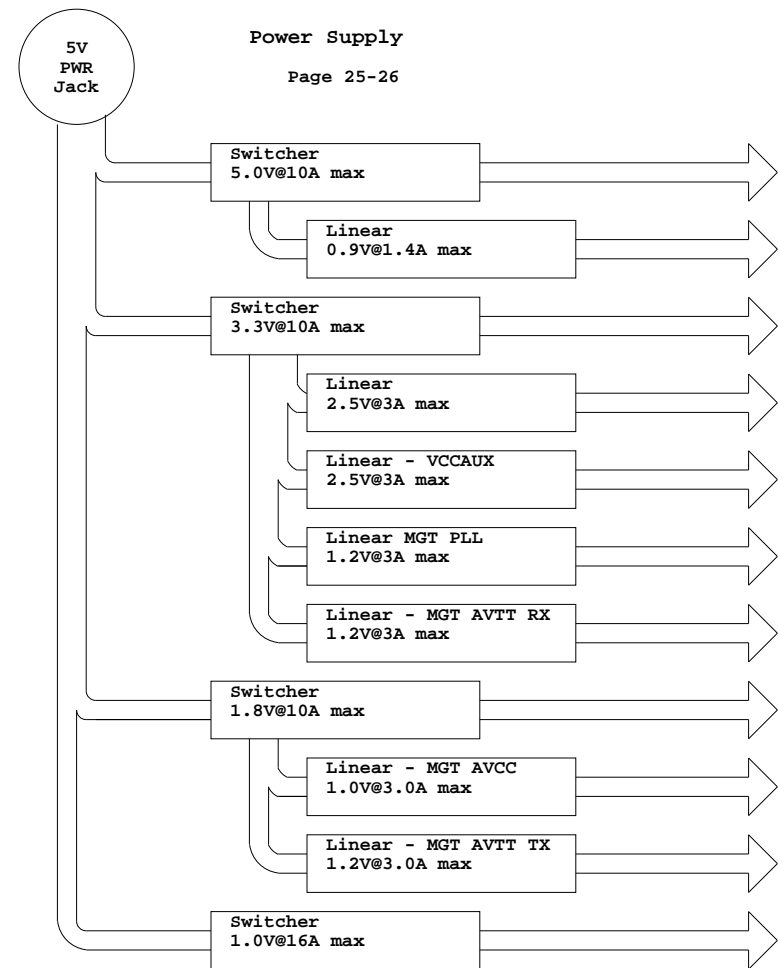
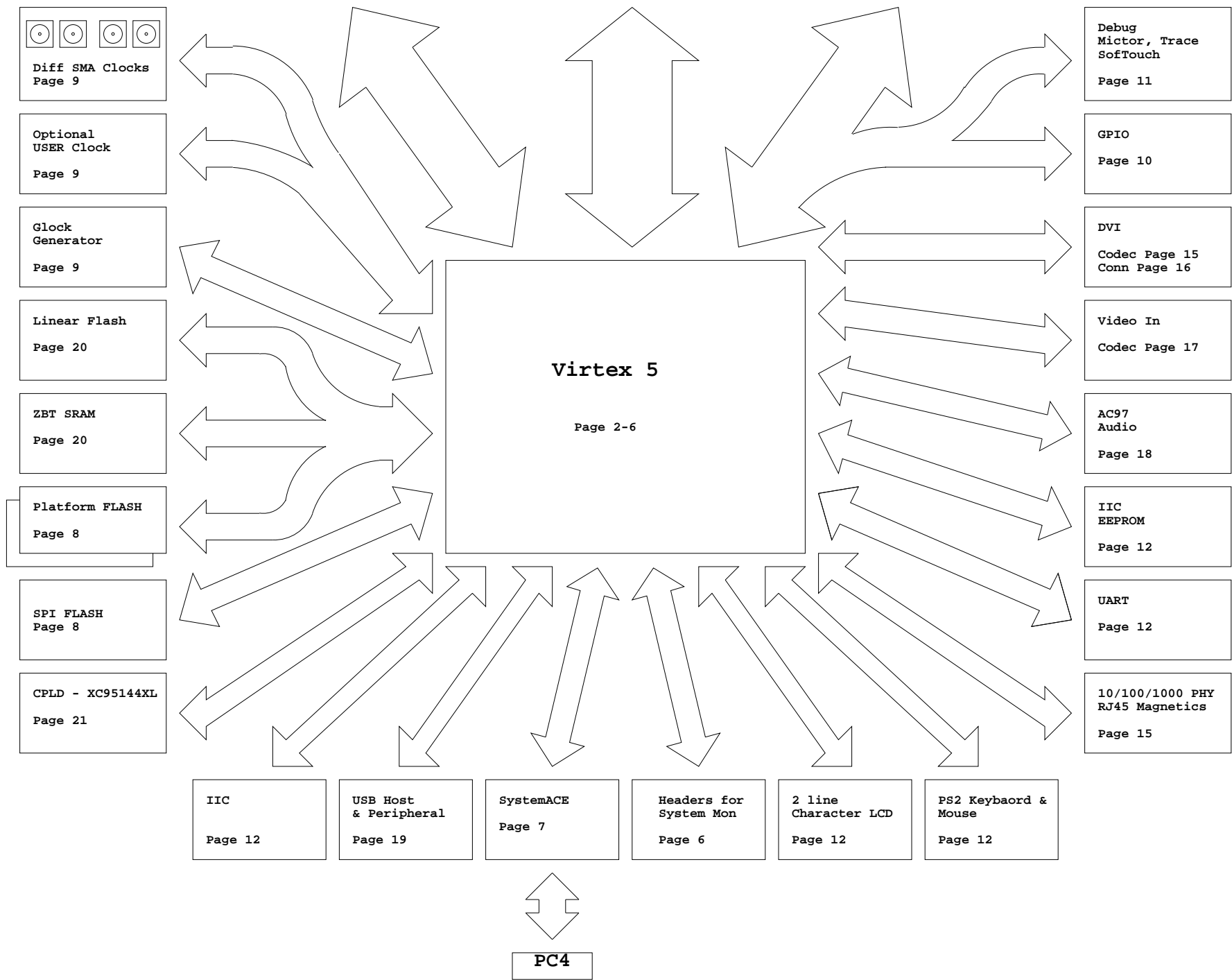


GTPs
SATA, SFP and SGMII
Page 22-24

64 Bit DDR2 SODIMM
Page 13

Expansion Header
Page 11



Title: ML505 Block Diagram
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

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D

C

B

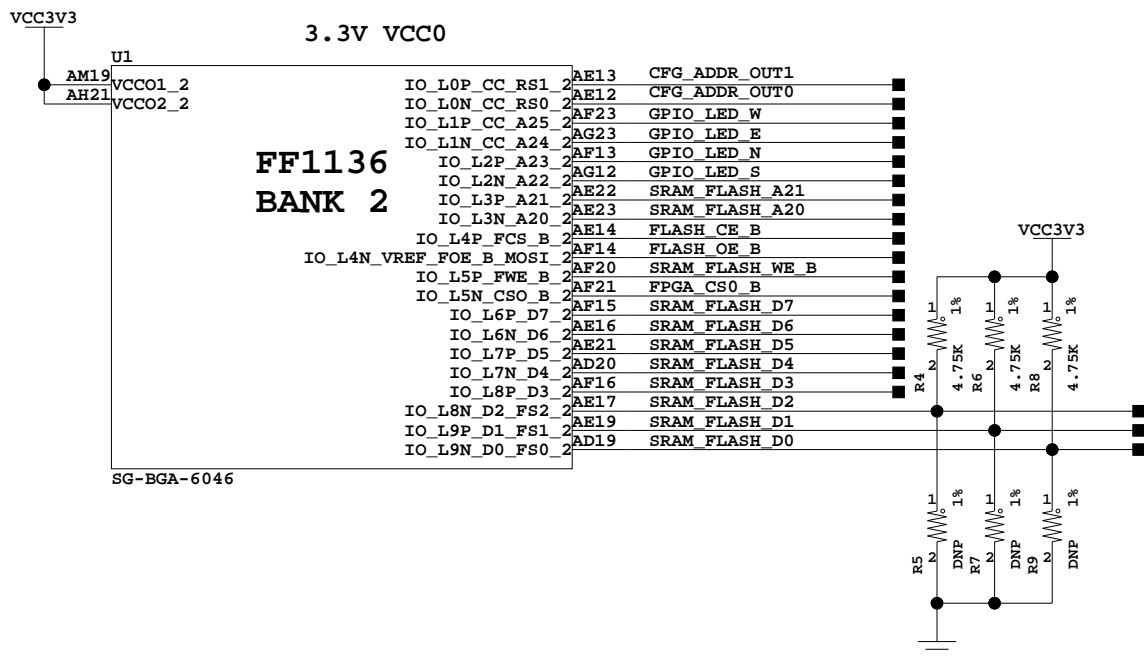
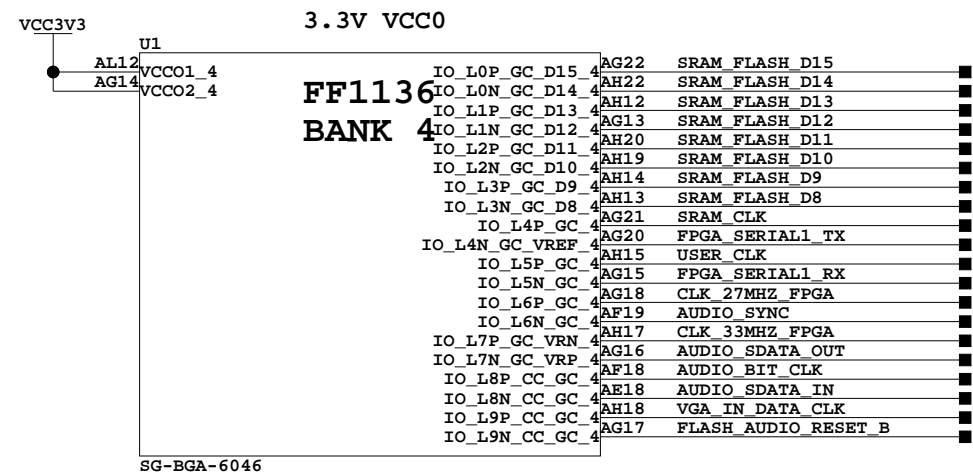
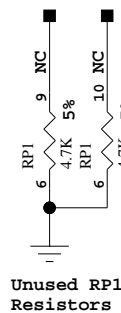
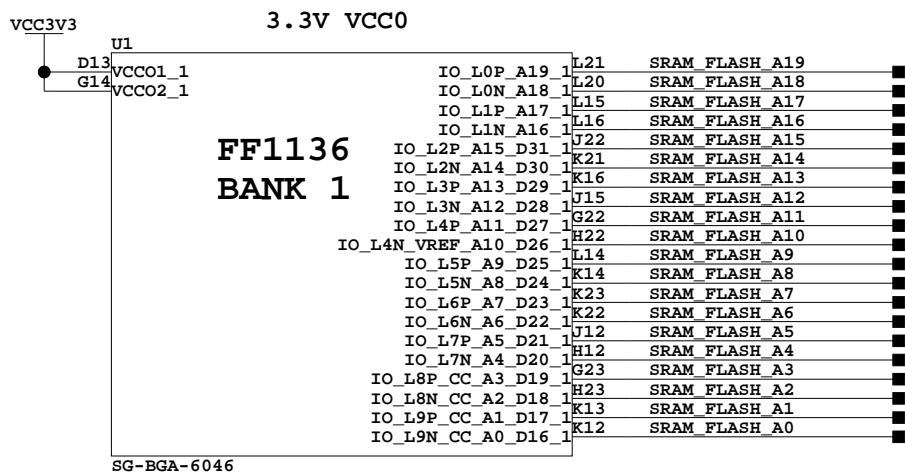
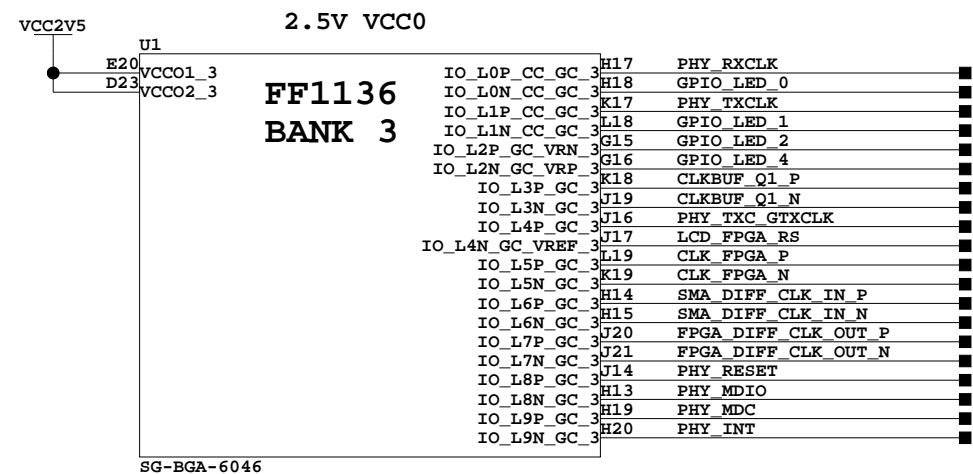
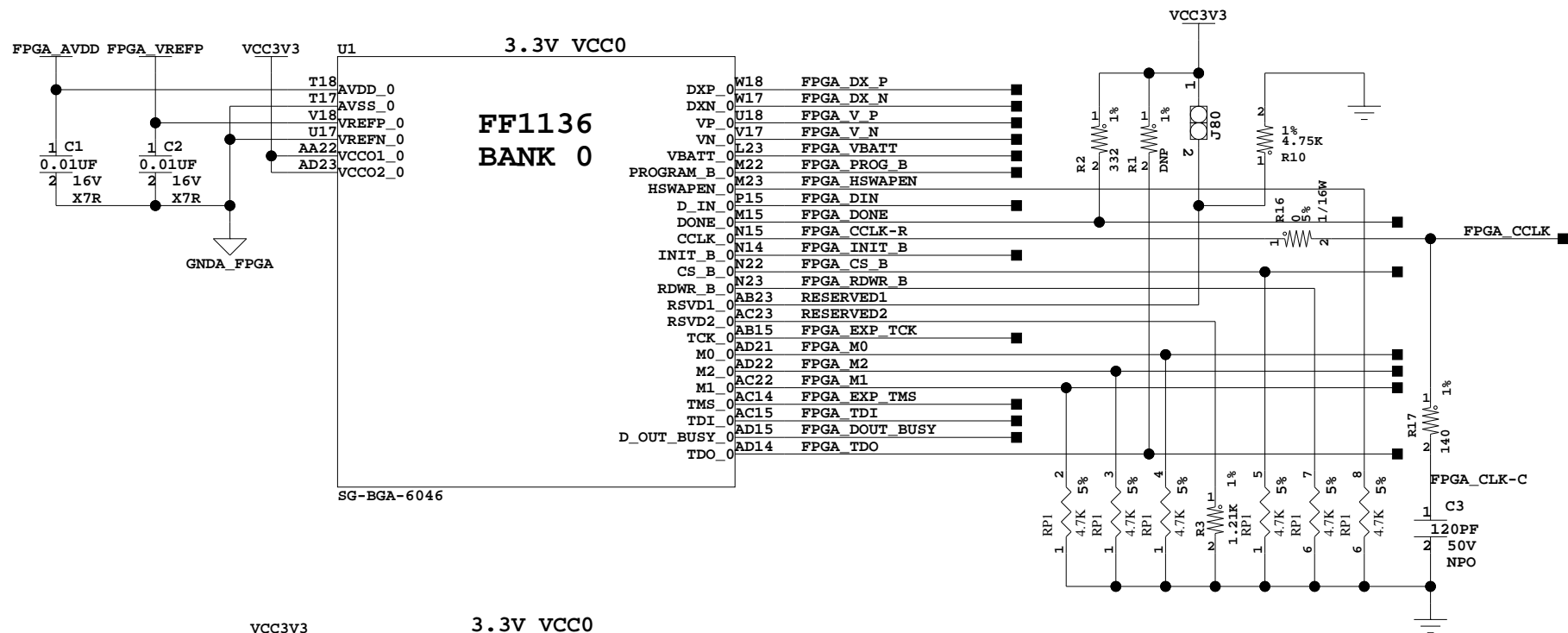
A

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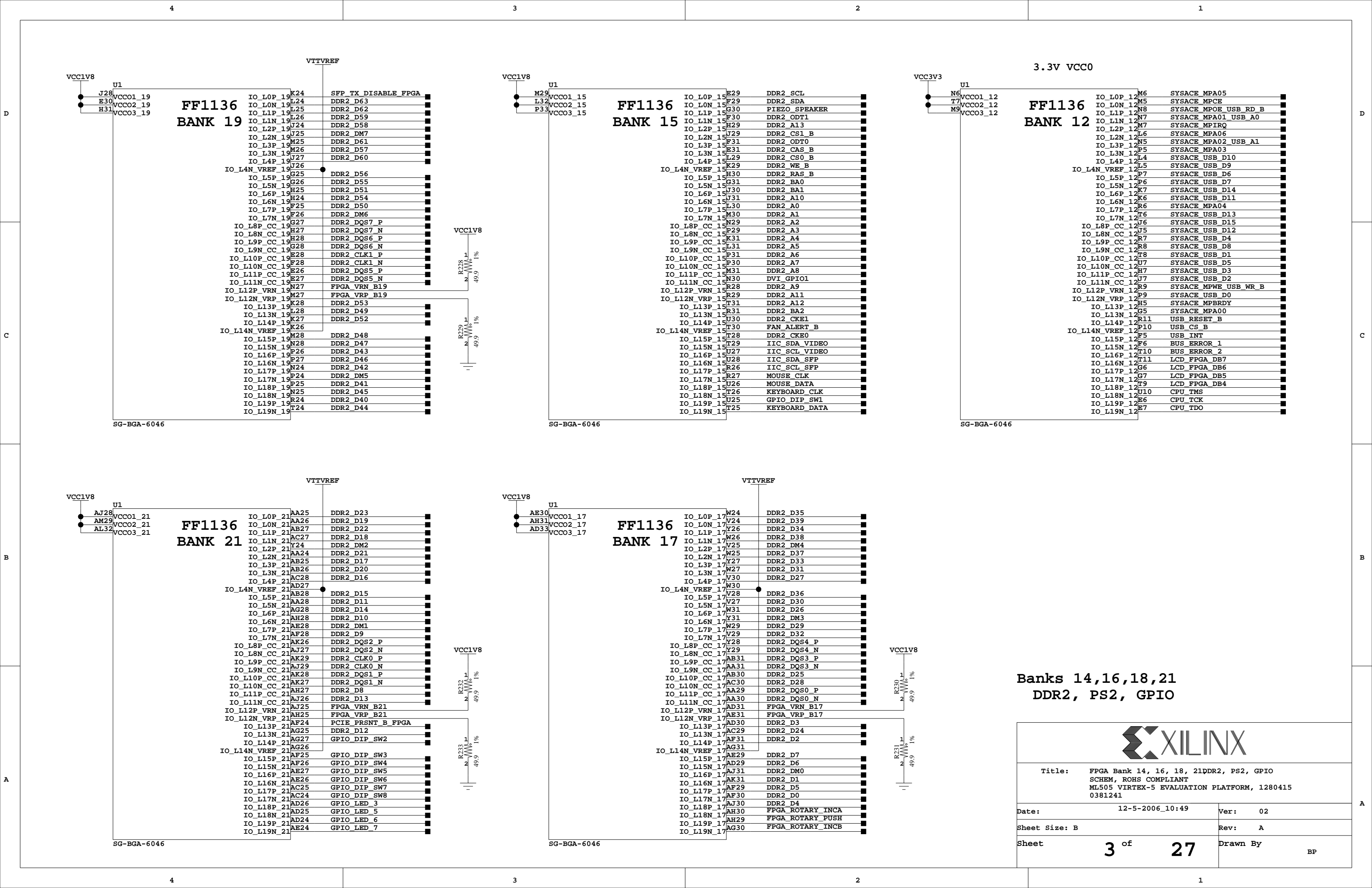
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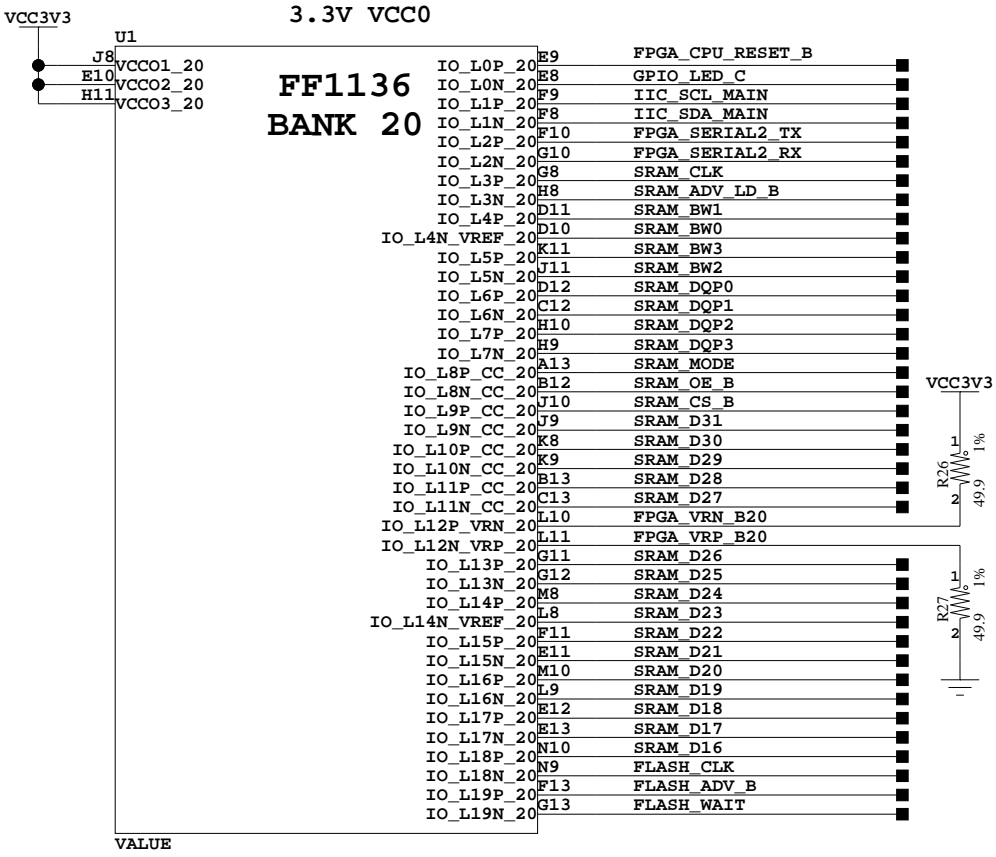
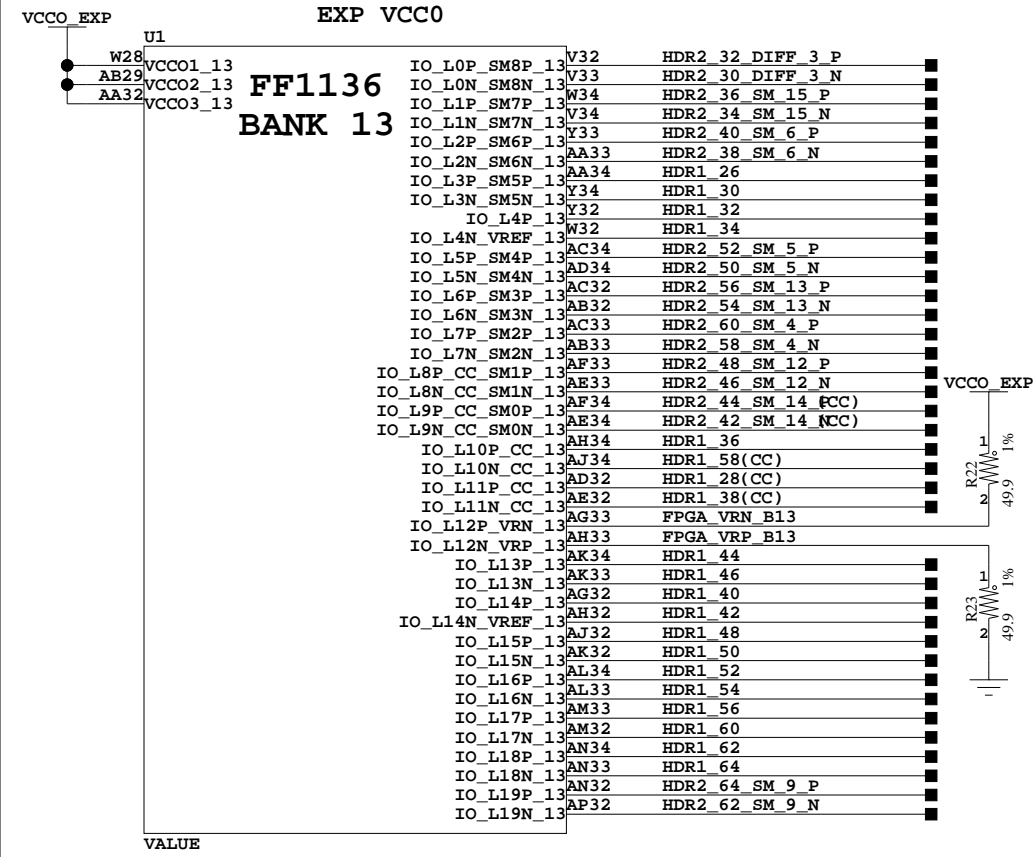
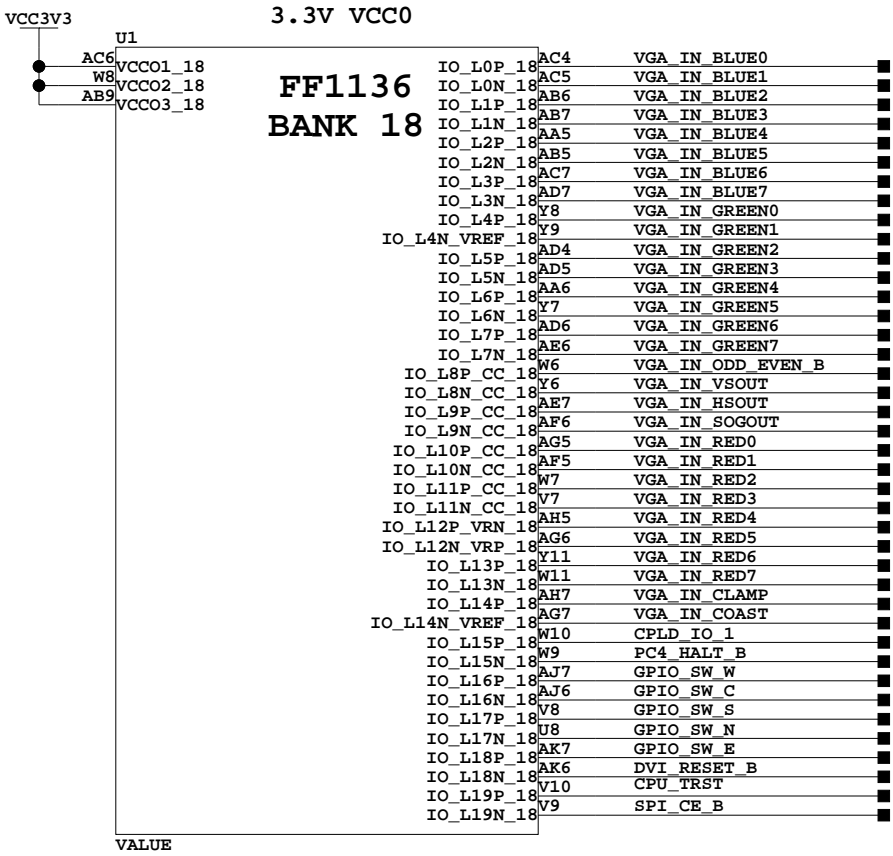
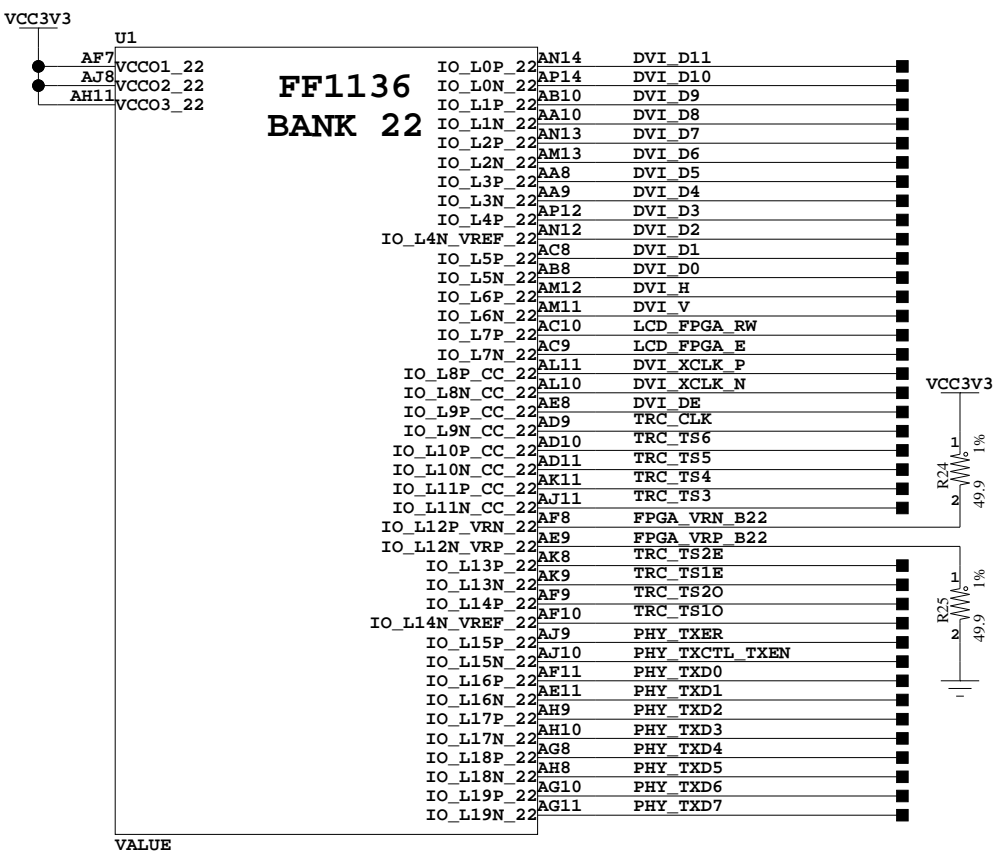
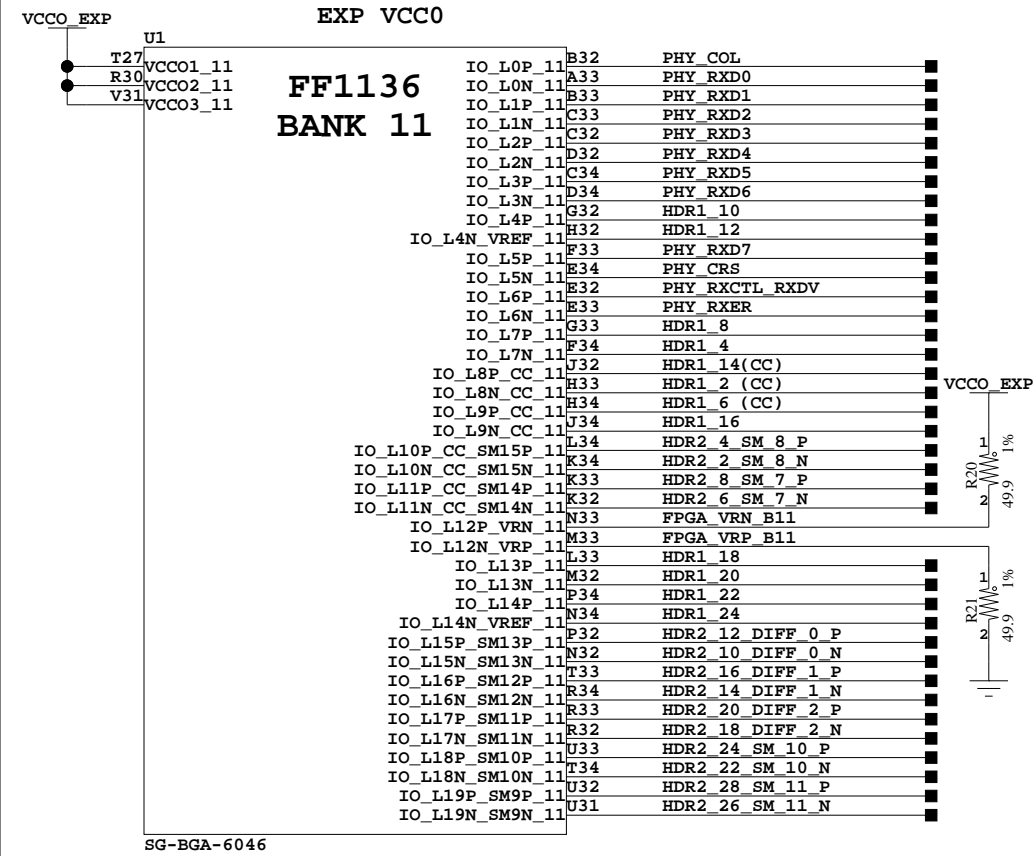


Banks 0,1,2,3,4
Config, FLASH, SRAM,
GPIO, CLKs



Title: FPGA Banks 0,1,2,3,@nfig, FLASH, SRAM, GPIO, CLKs SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 12-5-2006_10:49	Ver: 02	
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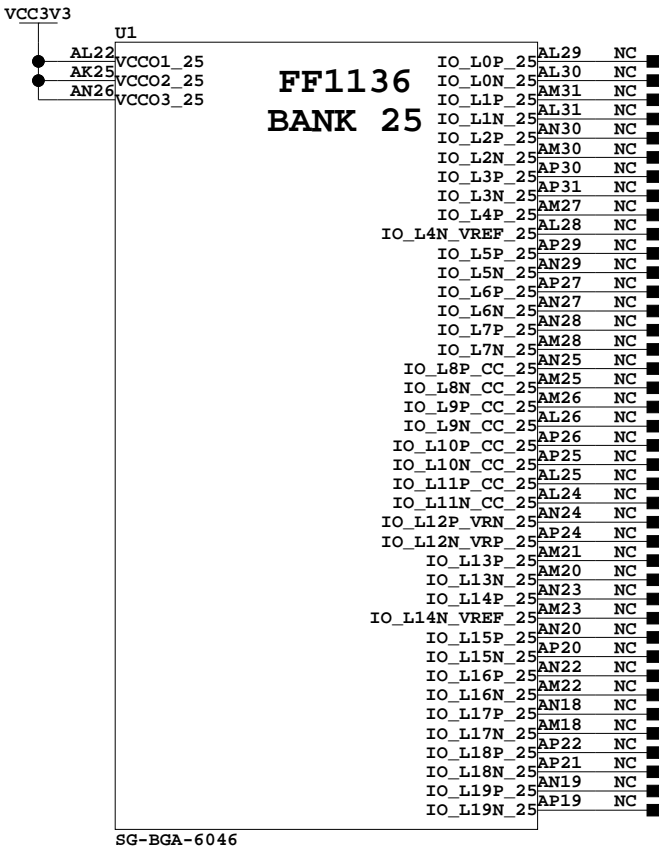
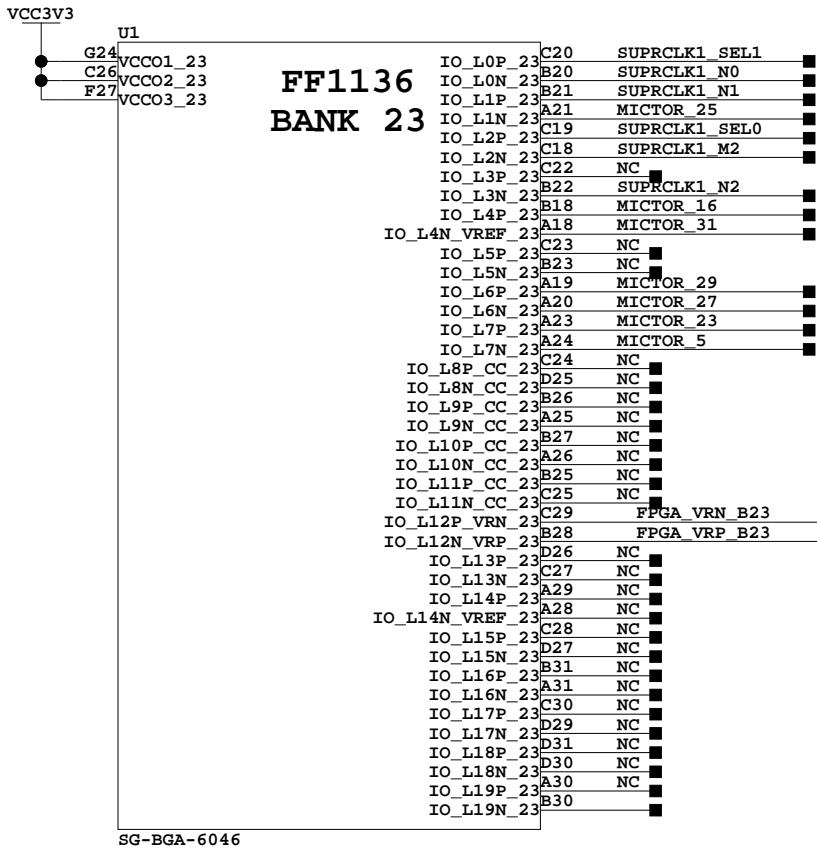
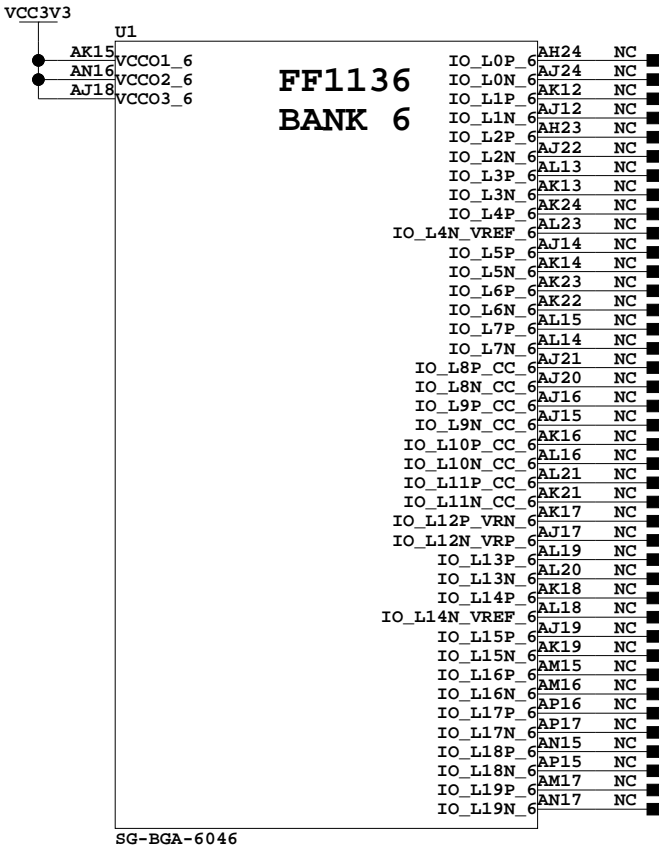
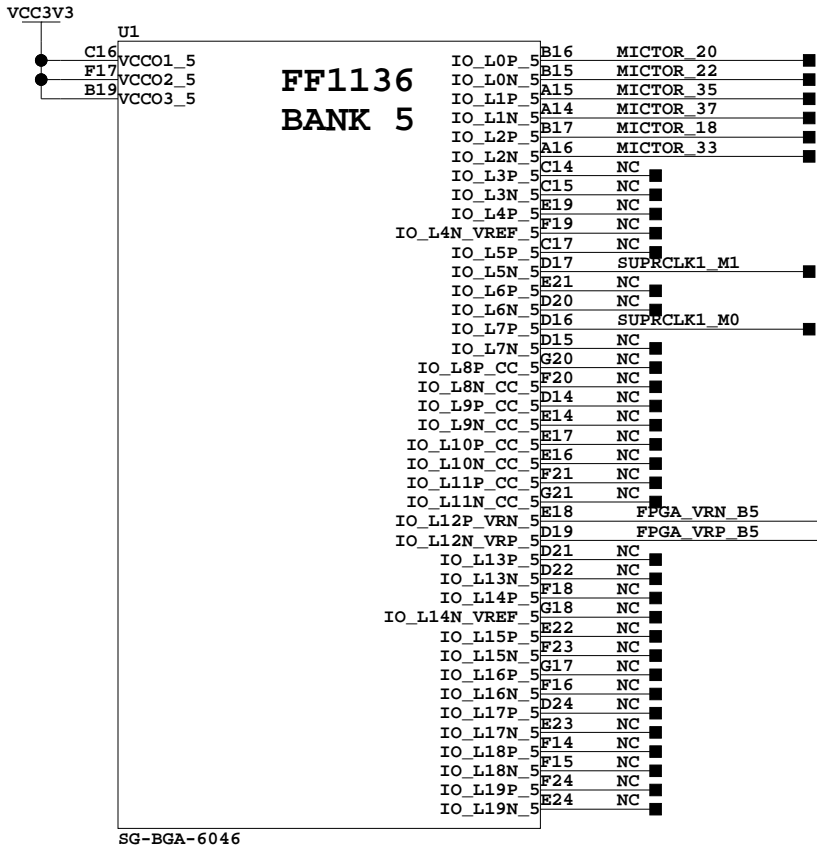


Banks 11,12,13
Sys ACE, XGI,
PHY, LCD




Title: Banks 11,12,13Sys ACE, XGI, PHY, LCD SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 12-5-2006_10:49	Ver: 02
Sheet Size: B	Rev: A
Sheet 4 of 27	Drawn By BP

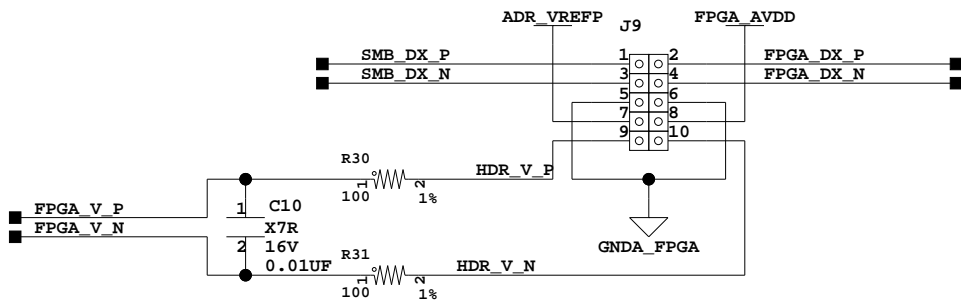
Unused banks on the LX50T and SX50T



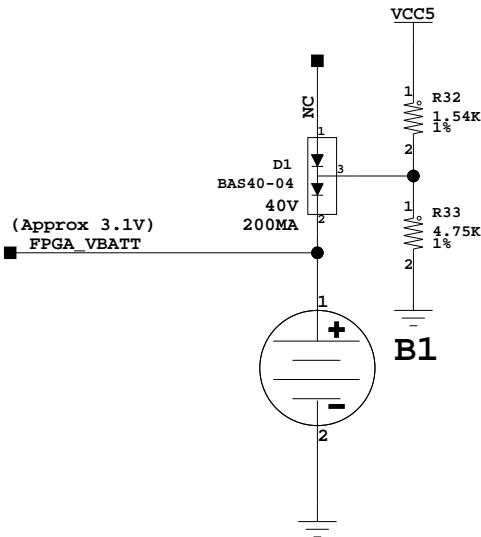
Banks 15, 17
VGA, IIC, PHY
SRAM, FLASH, GPIO

			
Title:		Banks 11,12,13,VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date:	12-5-2006_10:49	Ver:	02
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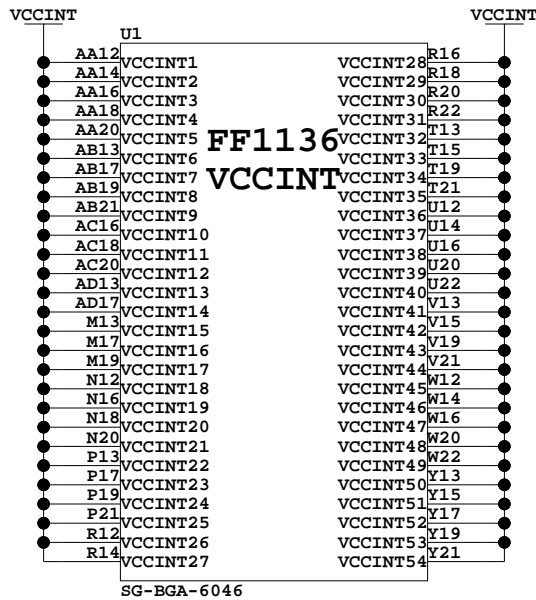
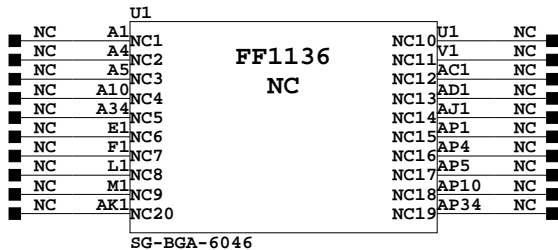
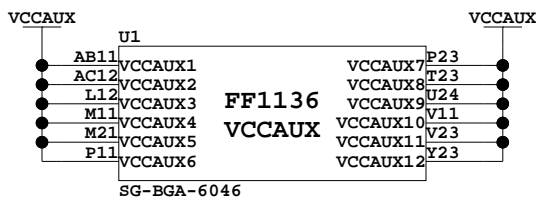
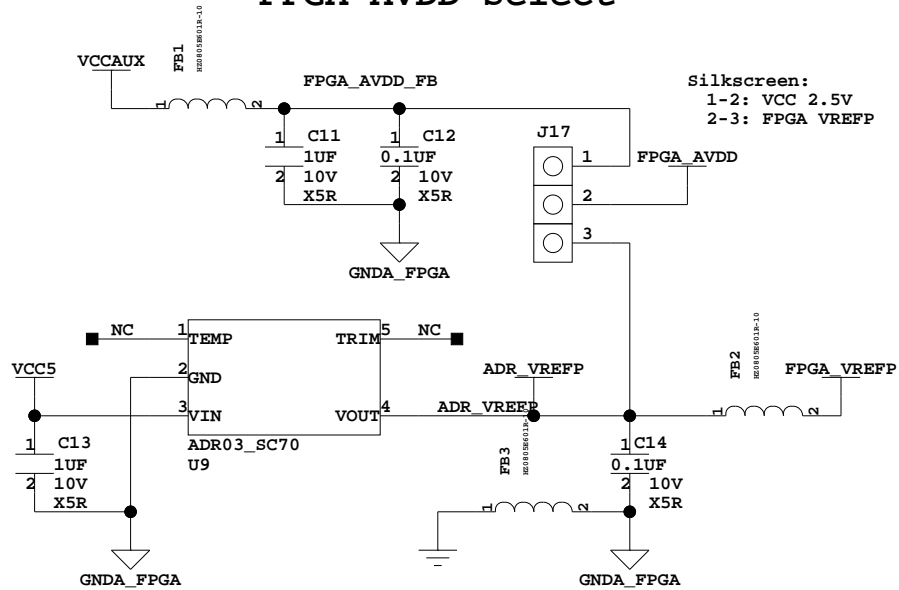
System Monitor Header



Rechargeable Battery



FPGA AVDD Select

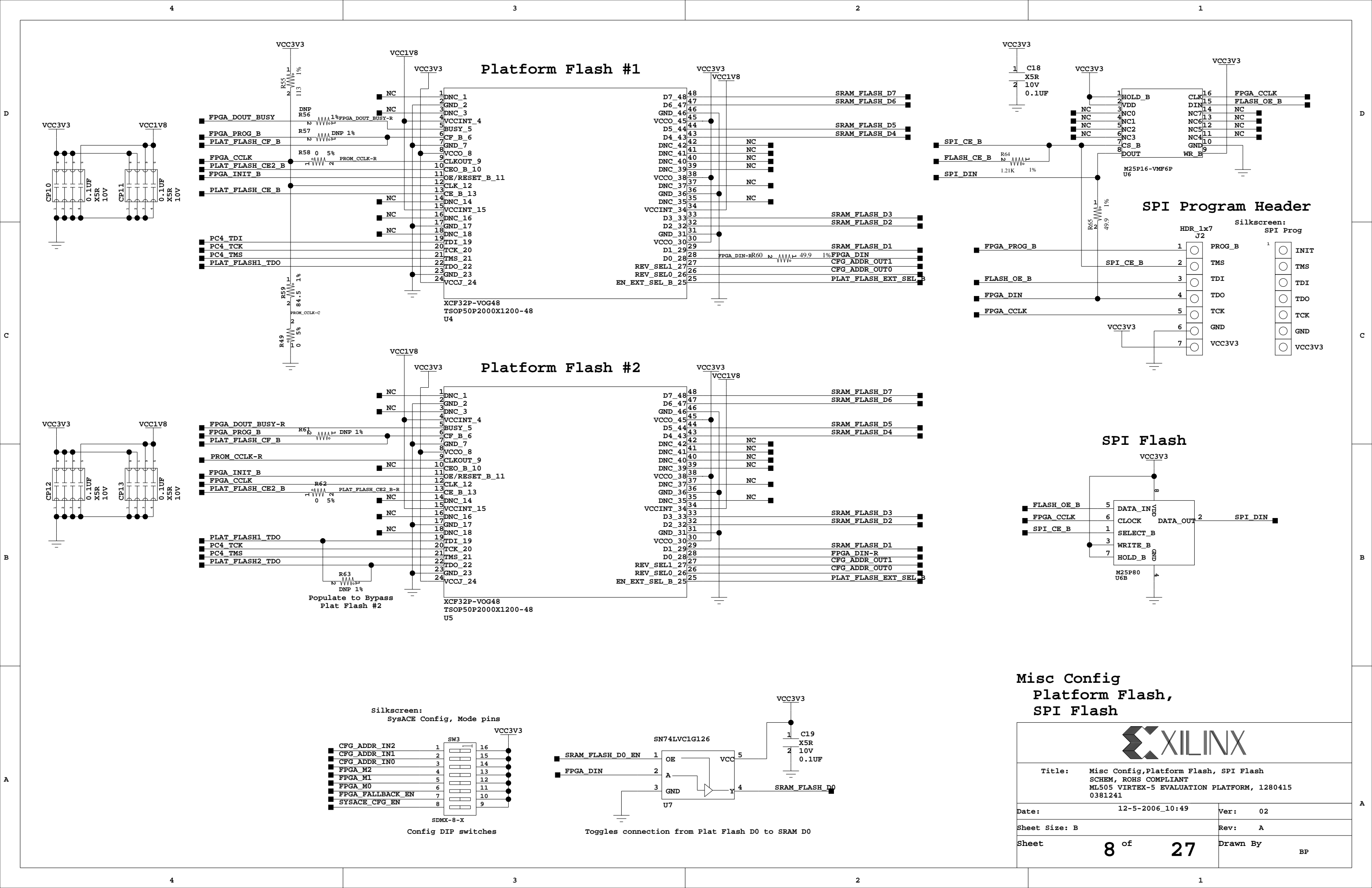


Power and Misc FPGA Banks
VCCINT, VCCAUX, NCs, GND
Battery and System Monitor



Title: FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

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C

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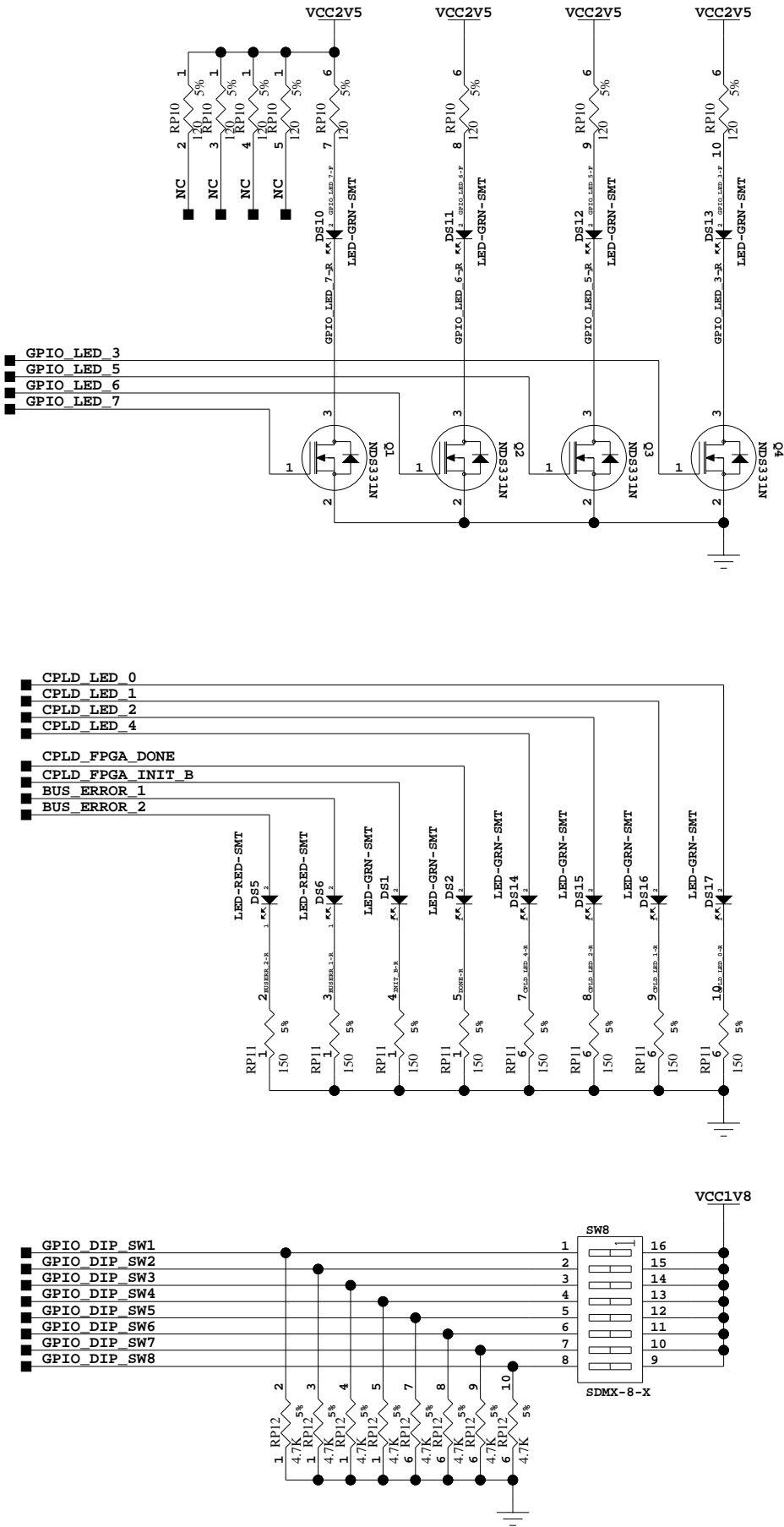
A

D

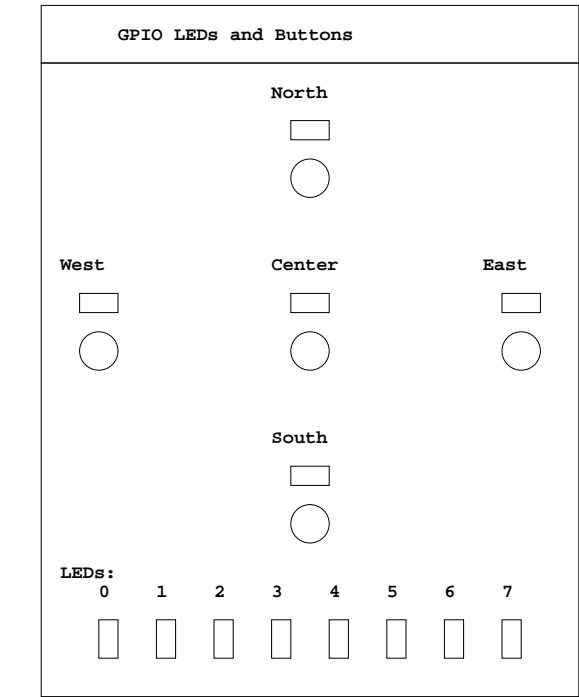
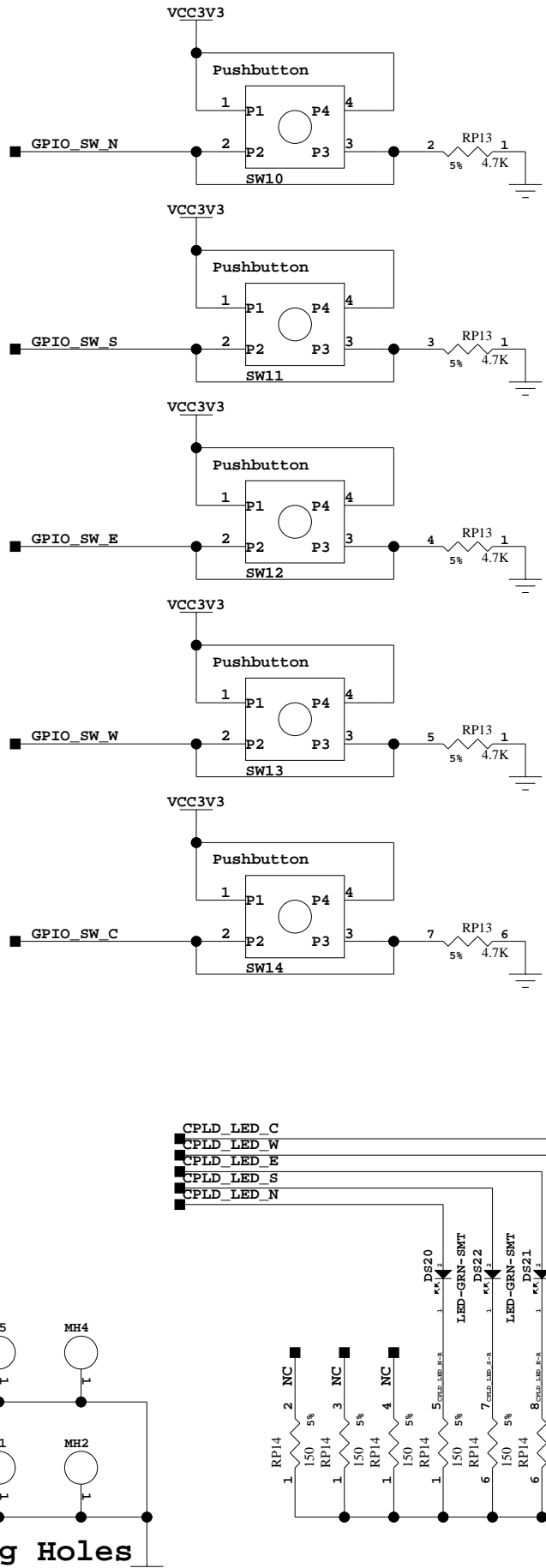
C

B

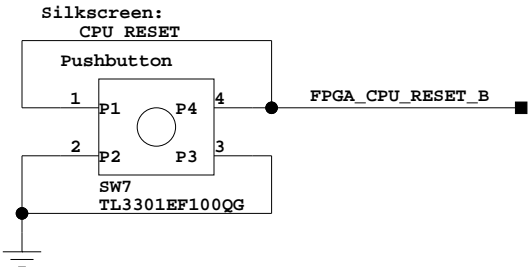
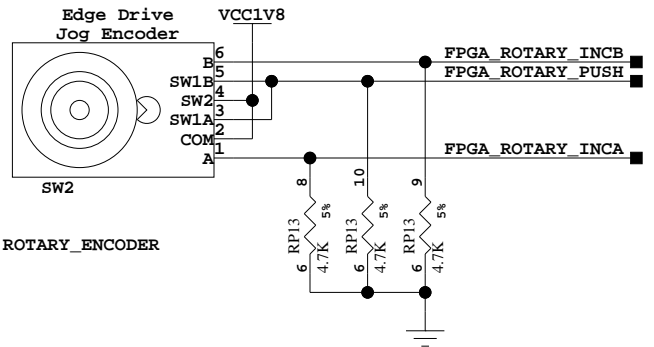
A



Mounting Holes



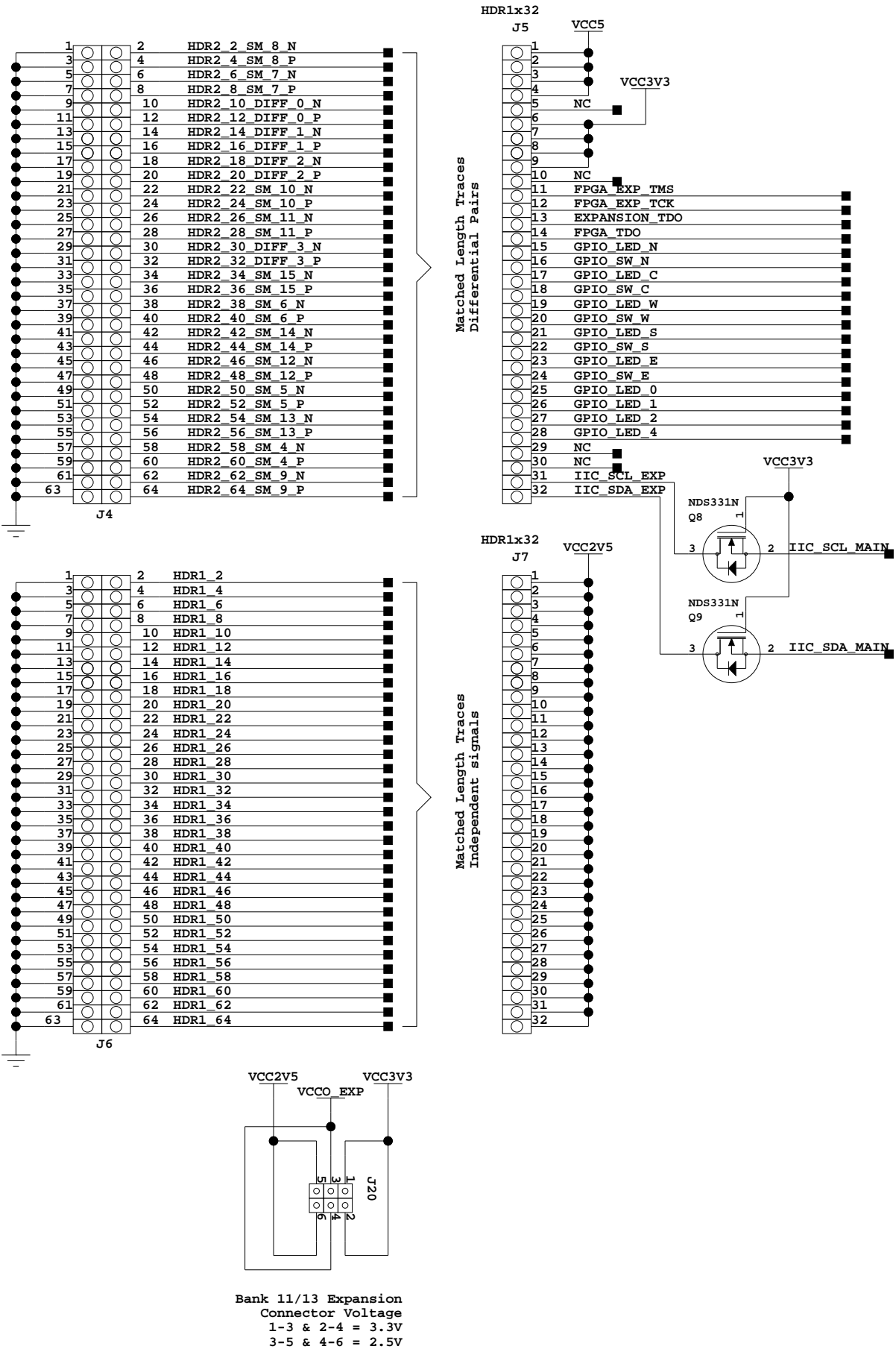
Edge Drive Jog Encoder Switch



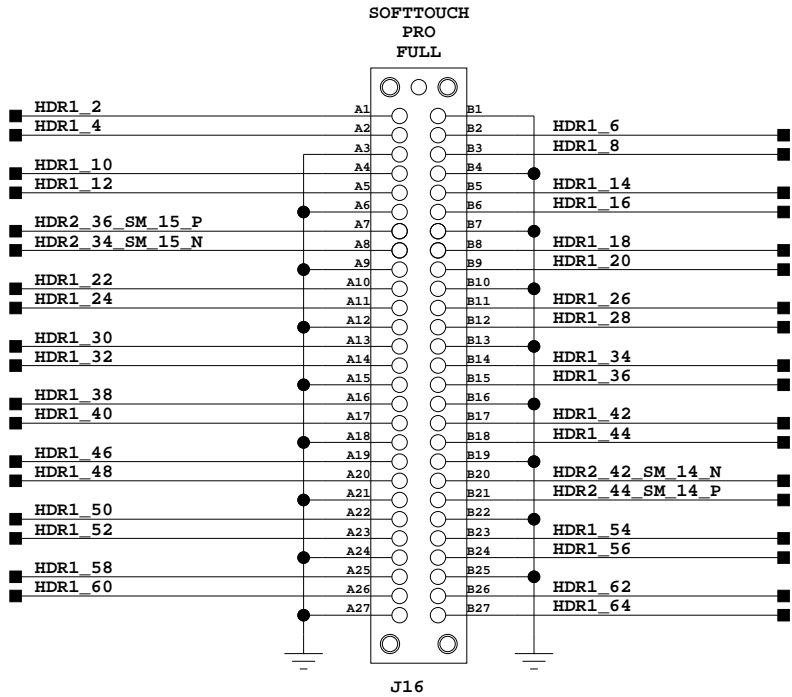
GPIO - Buttons, LEDs, Switches

Title: GPIO Buttons, LEDs, Switches SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241			
Date:	12-5-2006_10:49	Ver:	02
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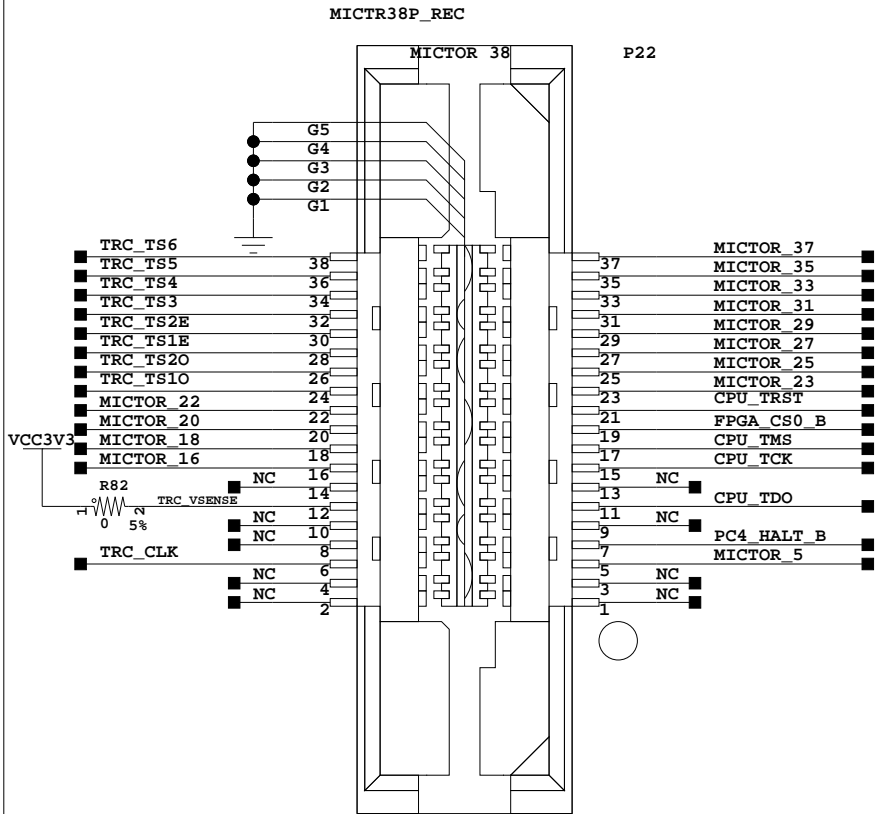
XGI Expansion Interface



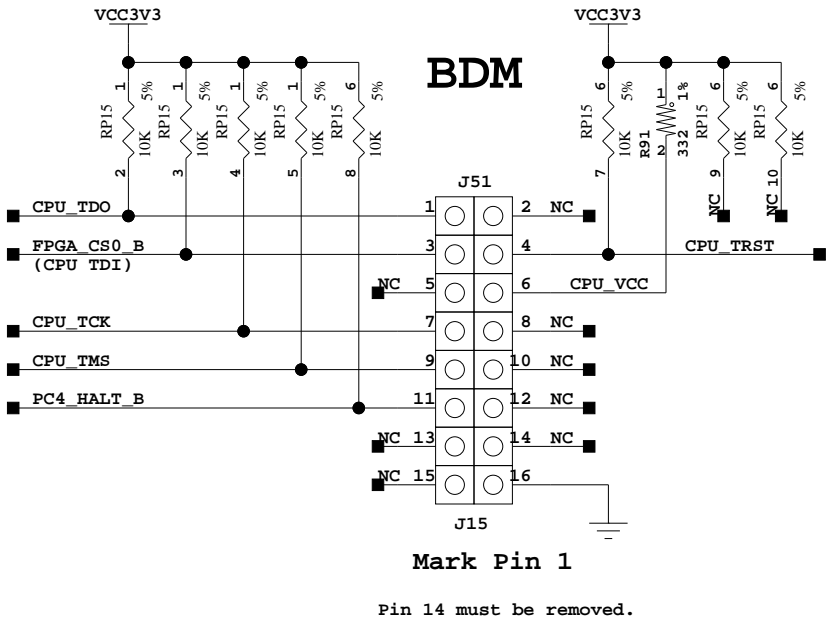
SoftTouch Pro



Mictor



BDM



XGI - Expansion Connector



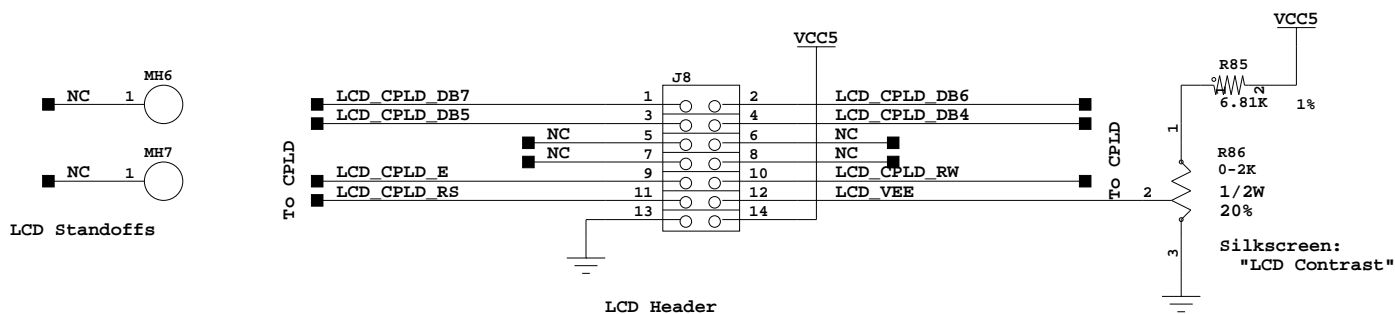
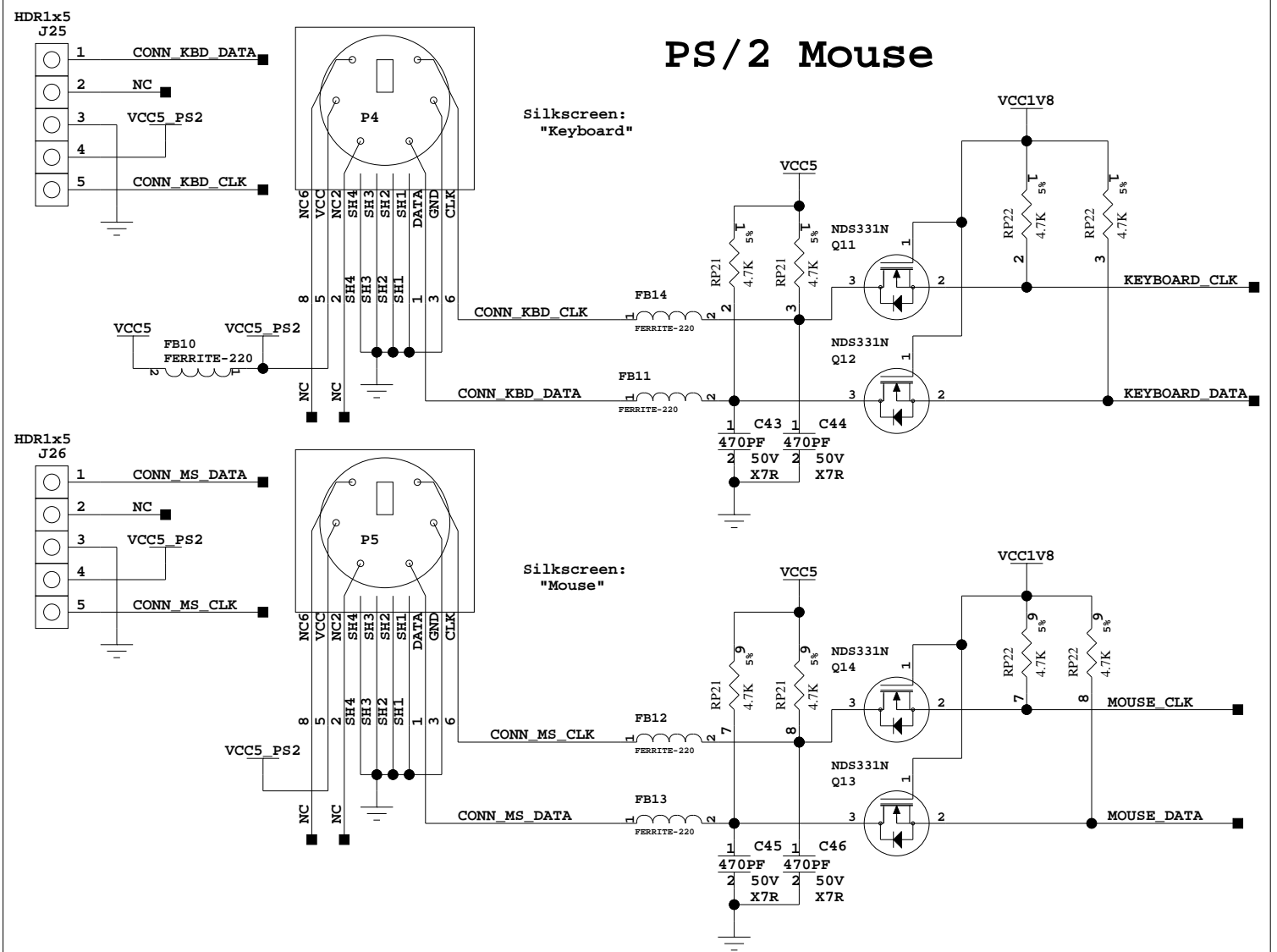
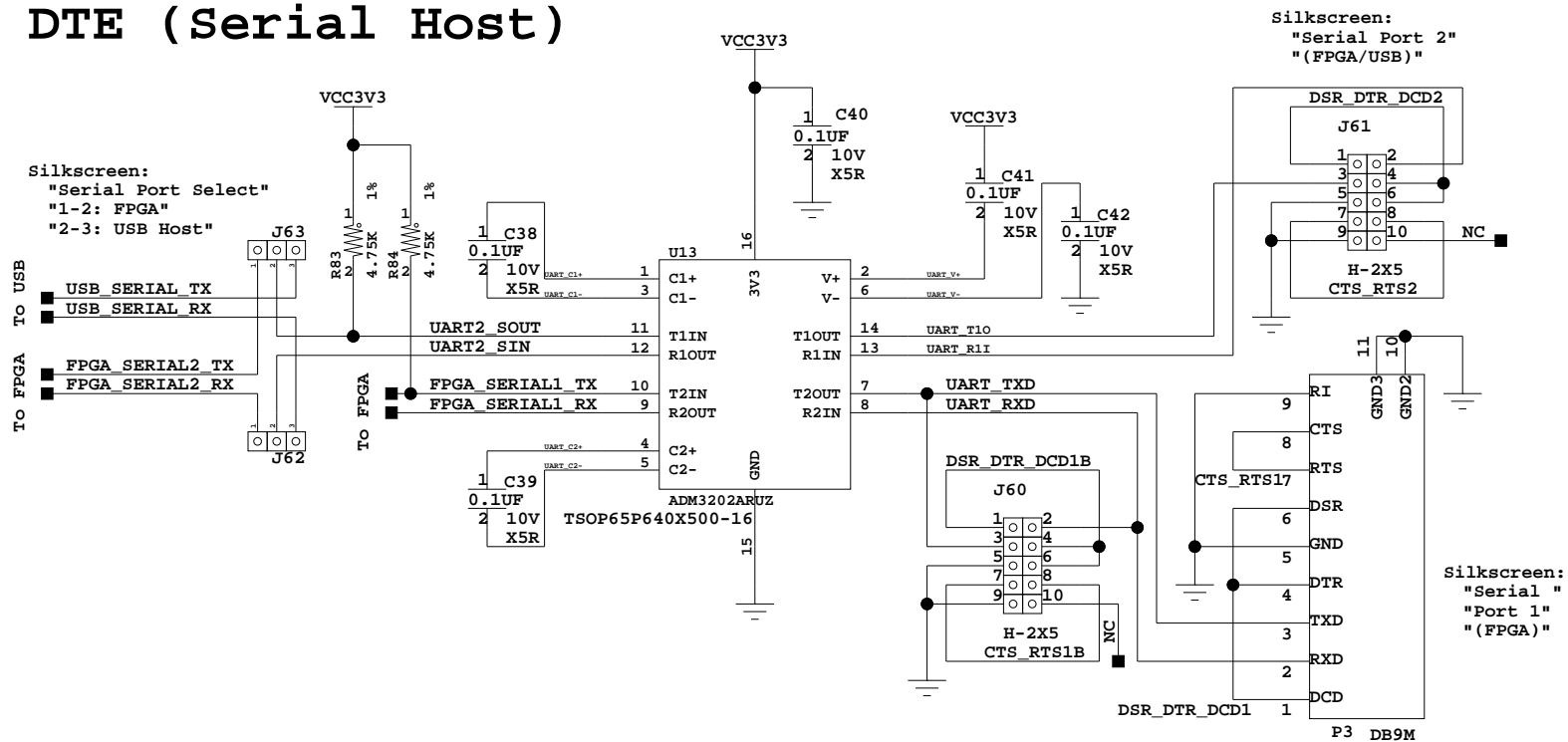
Title: XGI - Expansion Headers
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

Date: 12-5-2006_10:49 Ver: 02

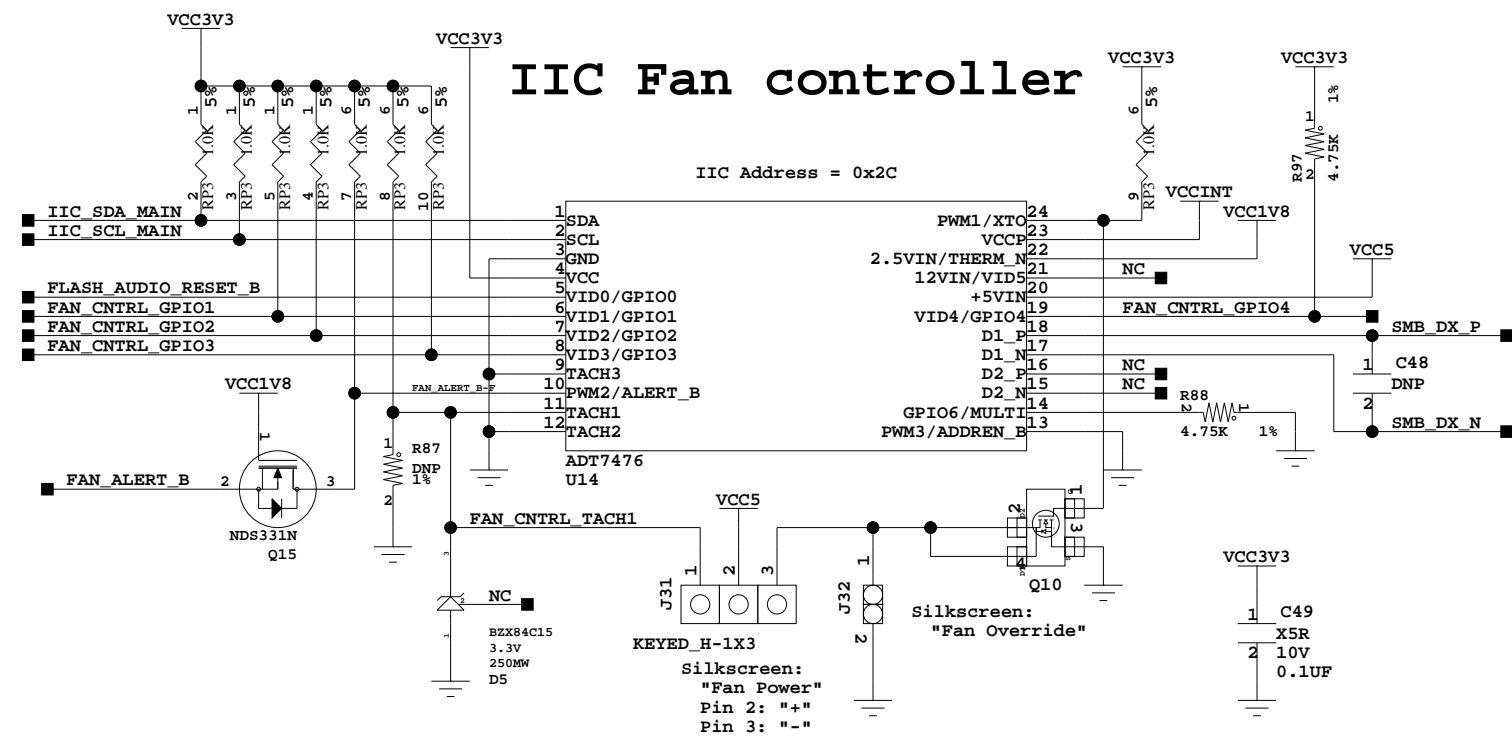
Sheet Size: B Rev: A

Sheet 11 of 27 Drawn By BP

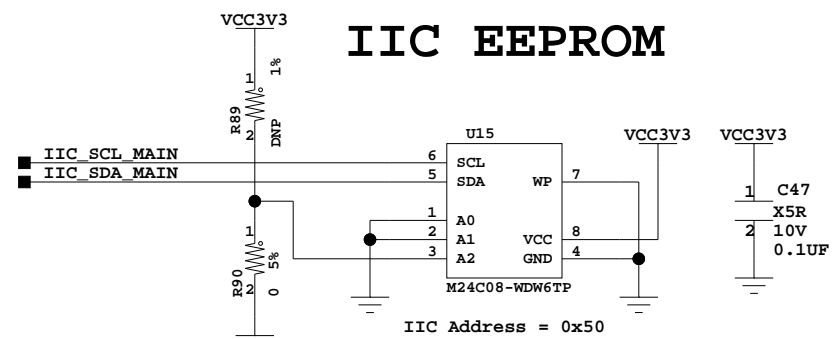
DTE (Serial Host)



IIC Fan controller



IIC EEPROM

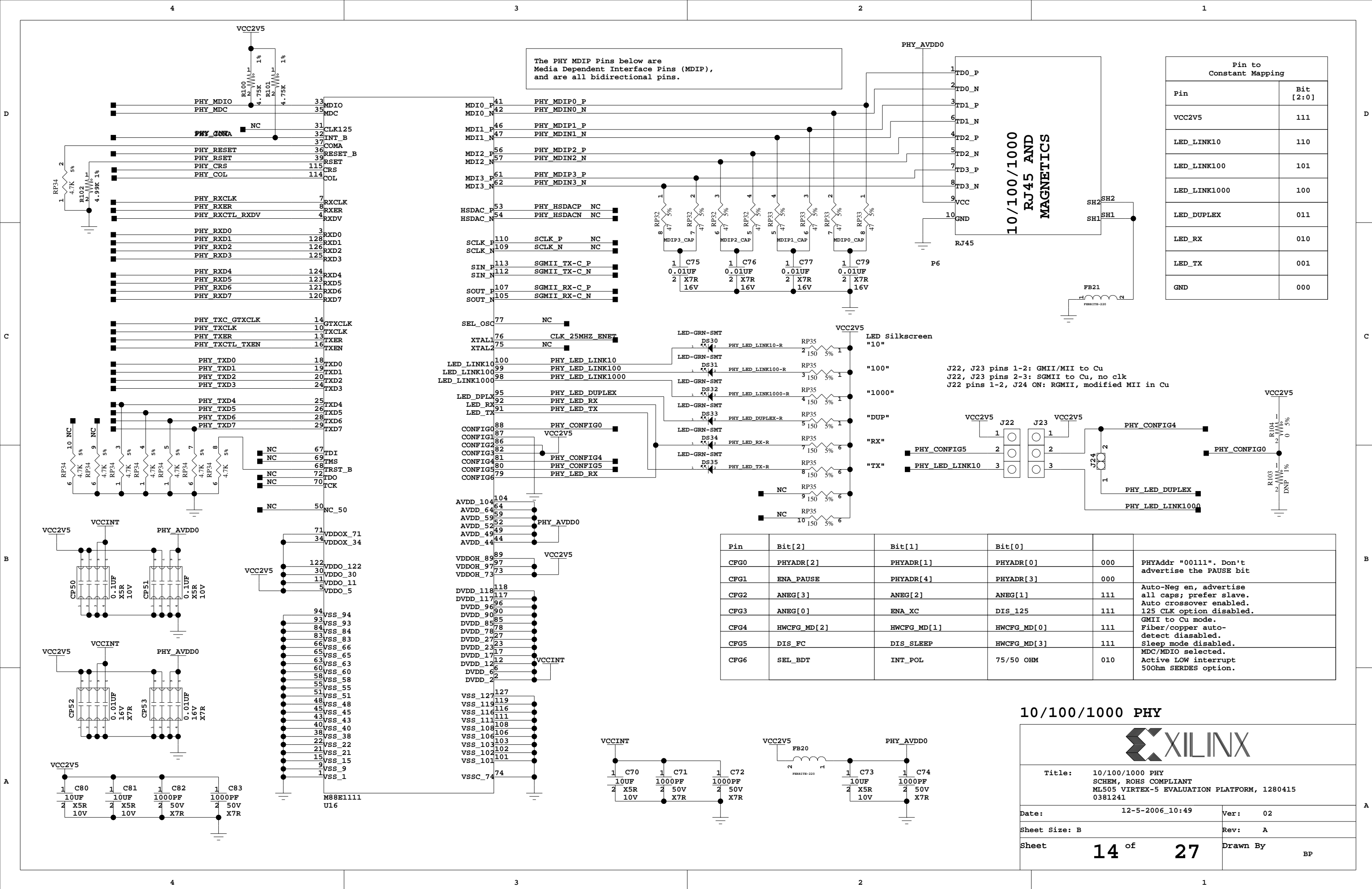


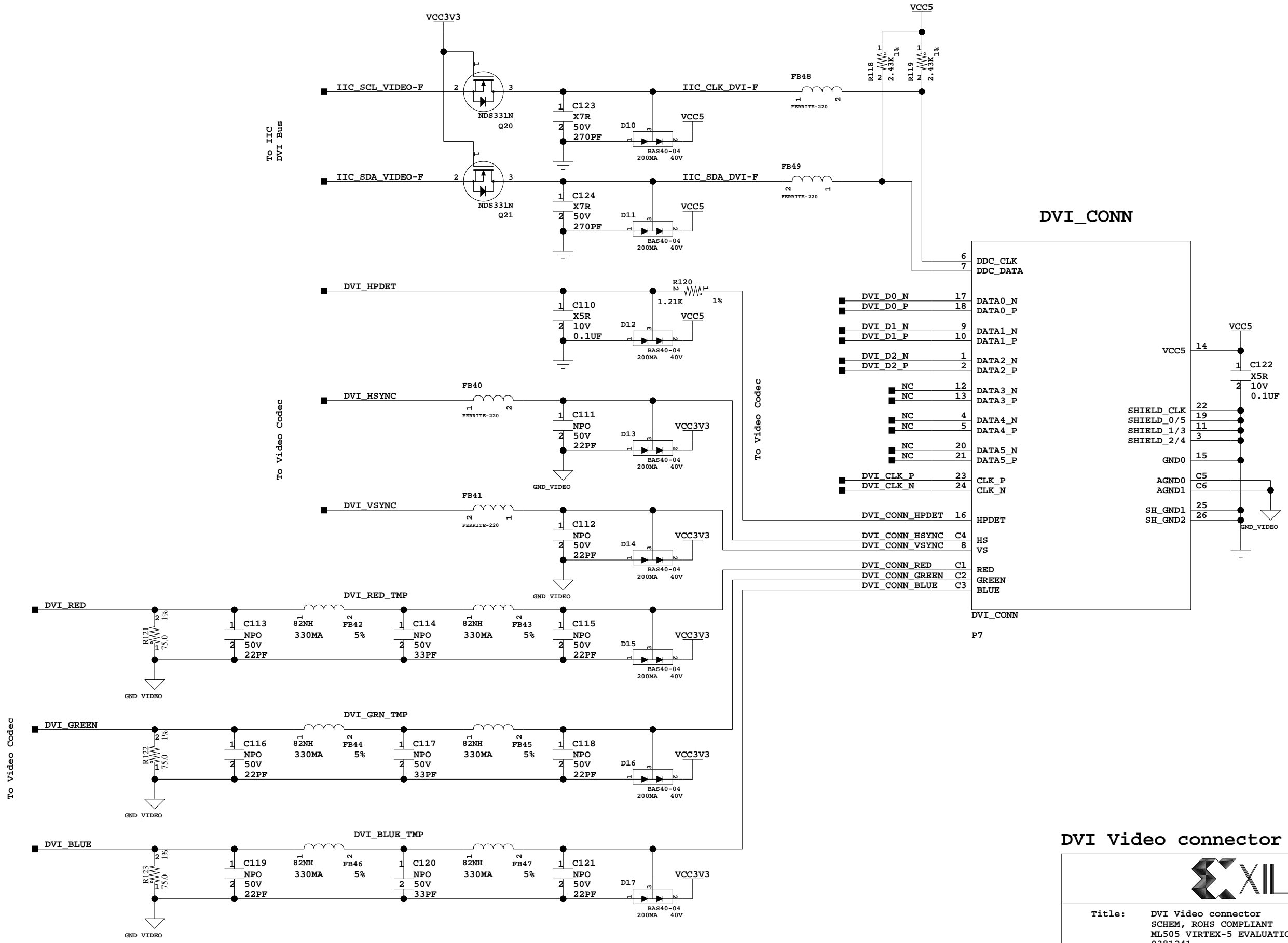
Misc - LCD, PS2, UART, Fan Controller



Title: LCD, PS2, UART, IIC EEPROM, IIC Fan Controller
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

Date:	12-5-2006_10:49	Ver:	02
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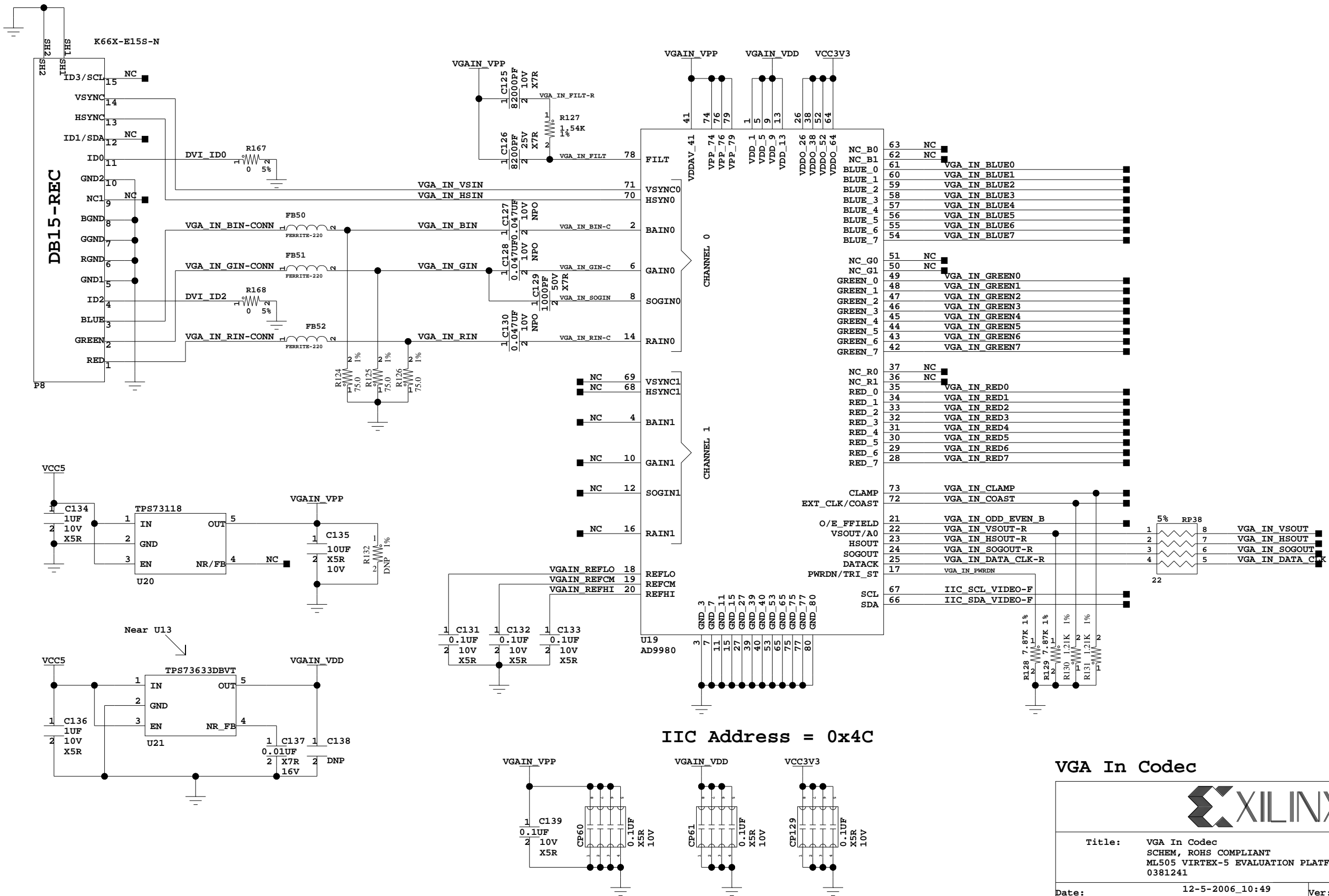


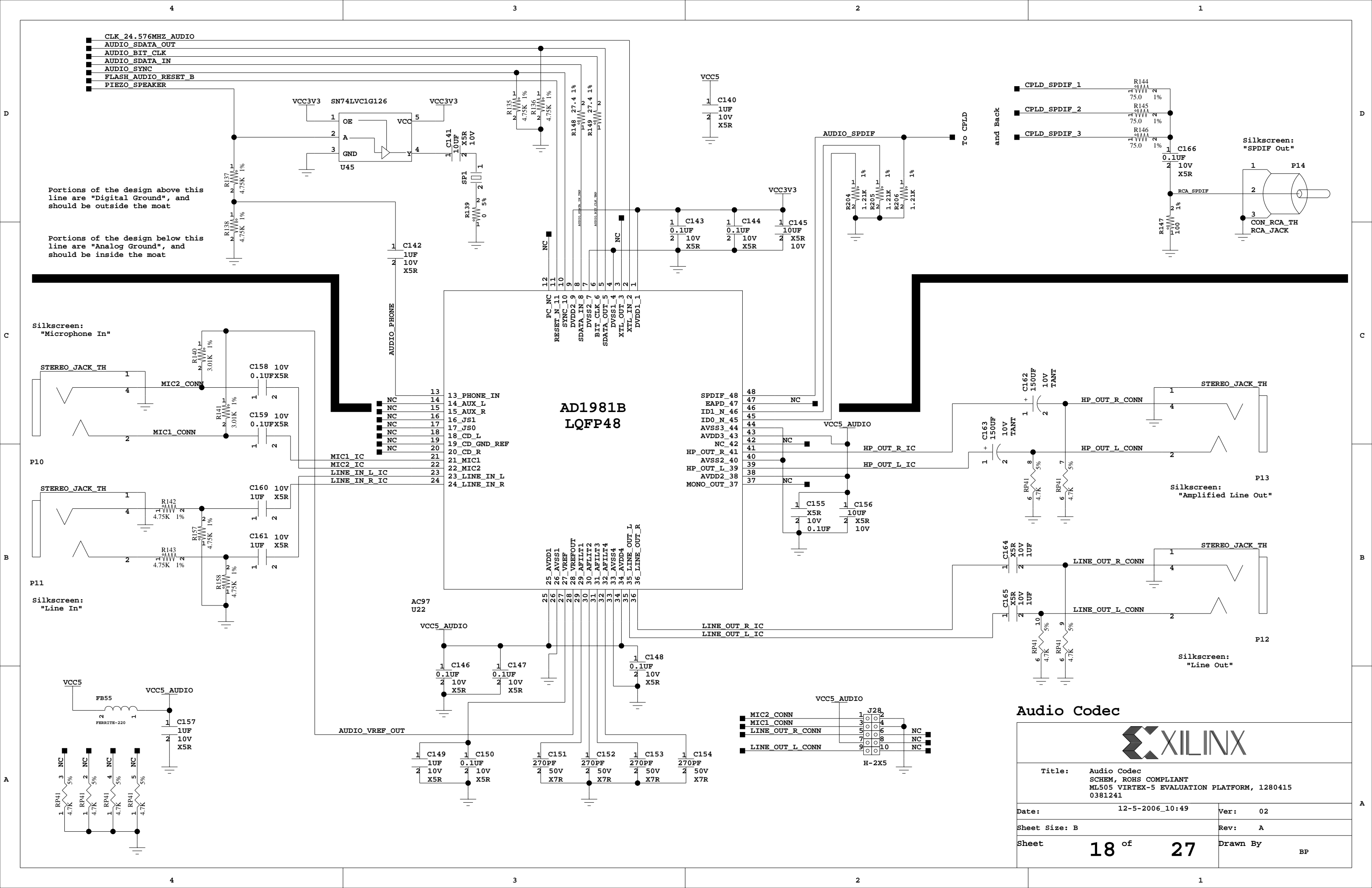


DVI Video connector

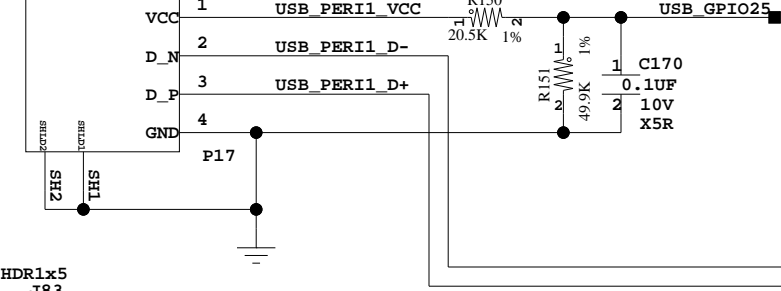


Title: DVI Video connector SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 12-5-2006_10:49	Ver: 02	
Sheet Size: B	Rev: A	
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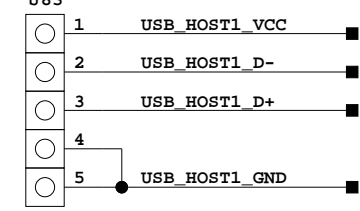




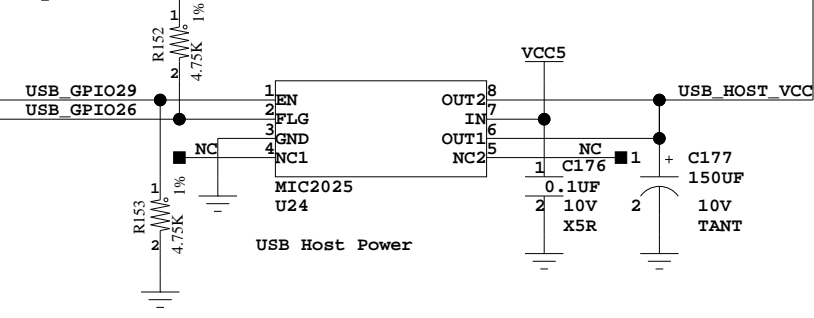
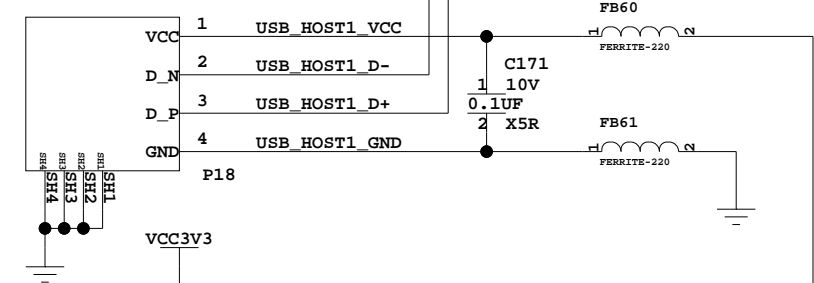
Silkscreen:
"USB Peripheral 1"
USB_B_PERI_SMT



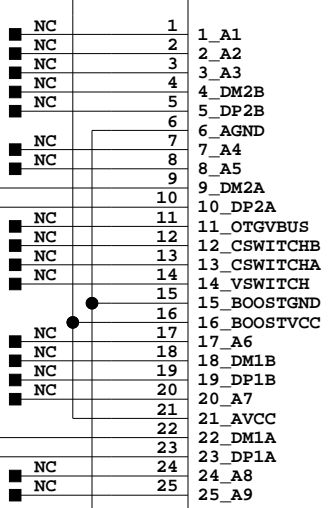
HDR1x5
J83



Silkscreen:
"USB Host"



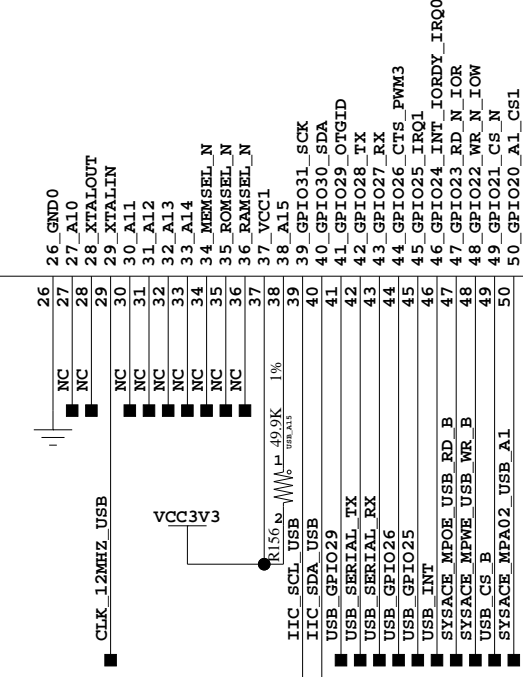
VCC3V3



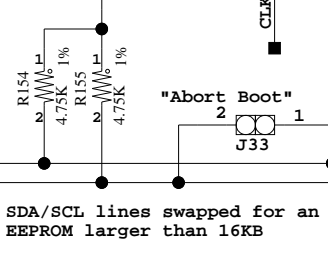
CY7C67300-100AI

(DIE UP)

U23
CYP_USB_HOST

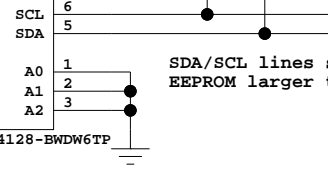


VCC3V3

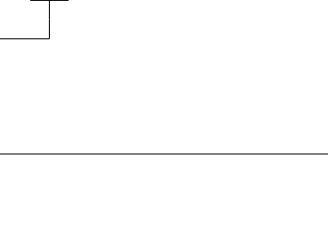


SDA/SCL lines swapped for an EEPROM larger than 16KB

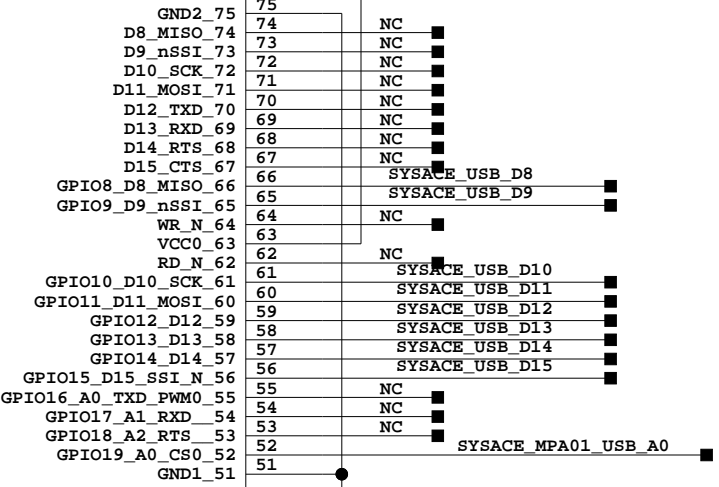
VCC3V3



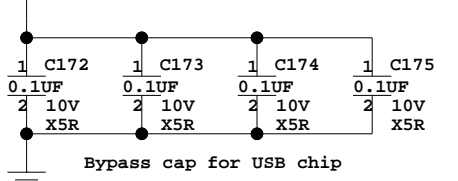
VCC3V3



VCC3V3



VCC3V3



Bypass cap for USB chip

USB Controller



Title: USB Controller
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

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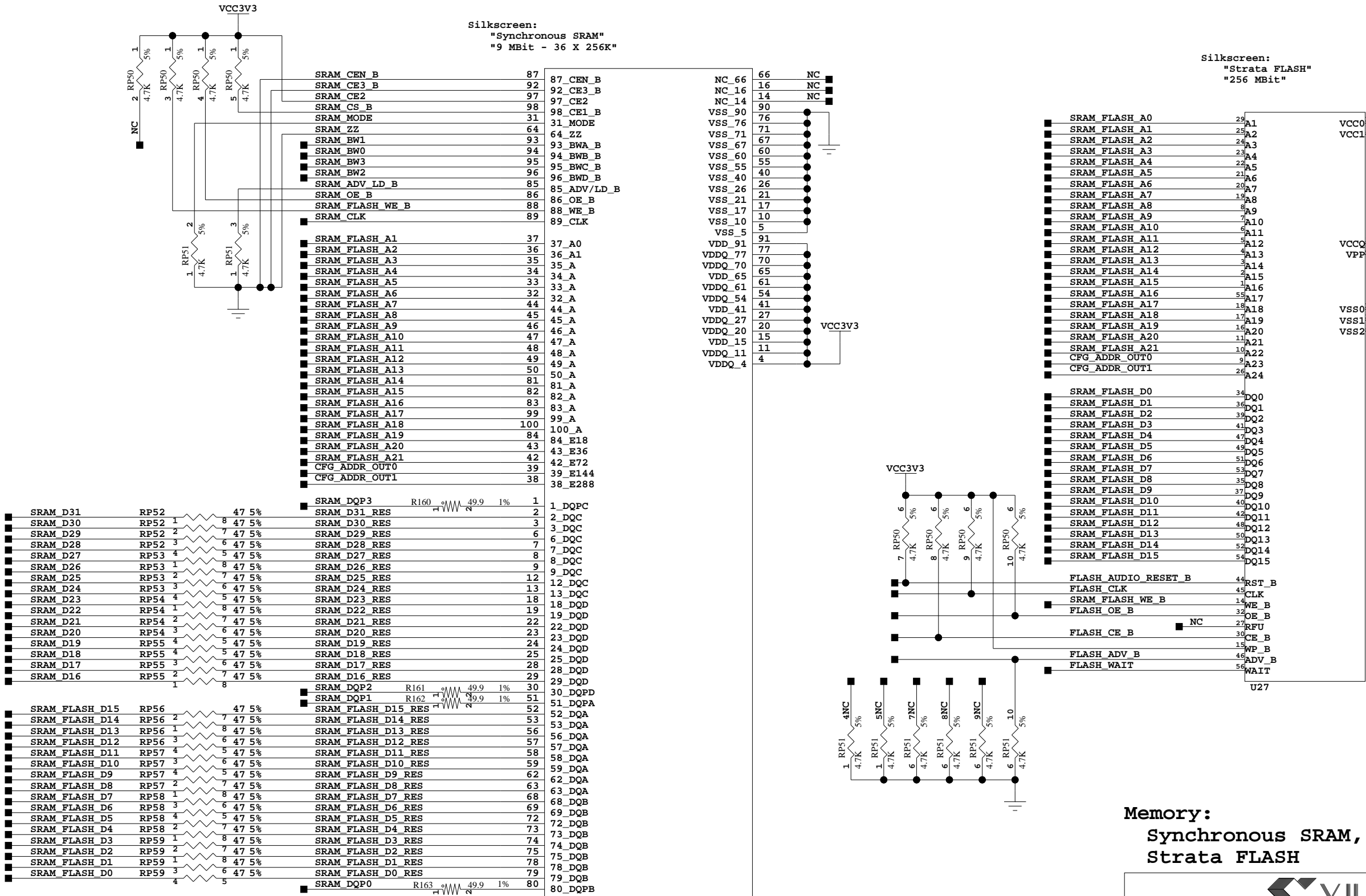
Sheet Size: B Rev: A

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The burst order mode of the SRAM is set to "Linear" by default

Silkscreen:
"Synchronous SRAM"
"9 MBit - 36 X 256K"

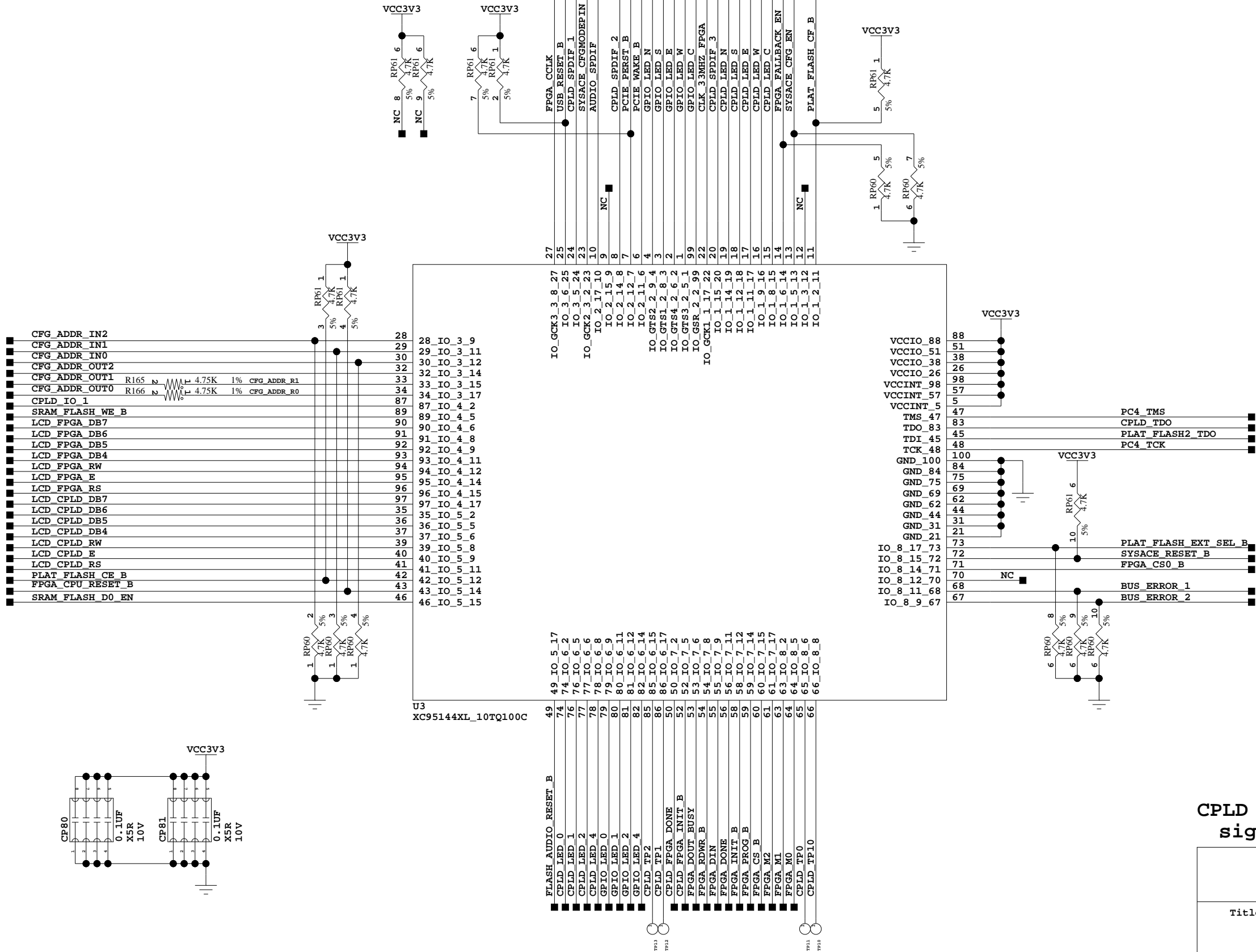
Silkscreen:
"Strata FLASH"
"256 MBit"



Memory:
Synchronous SRAM,
Strata FLASH



Title: Sync. SRAM, FLASH SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 12-5-2006_10:49	Ver: 02
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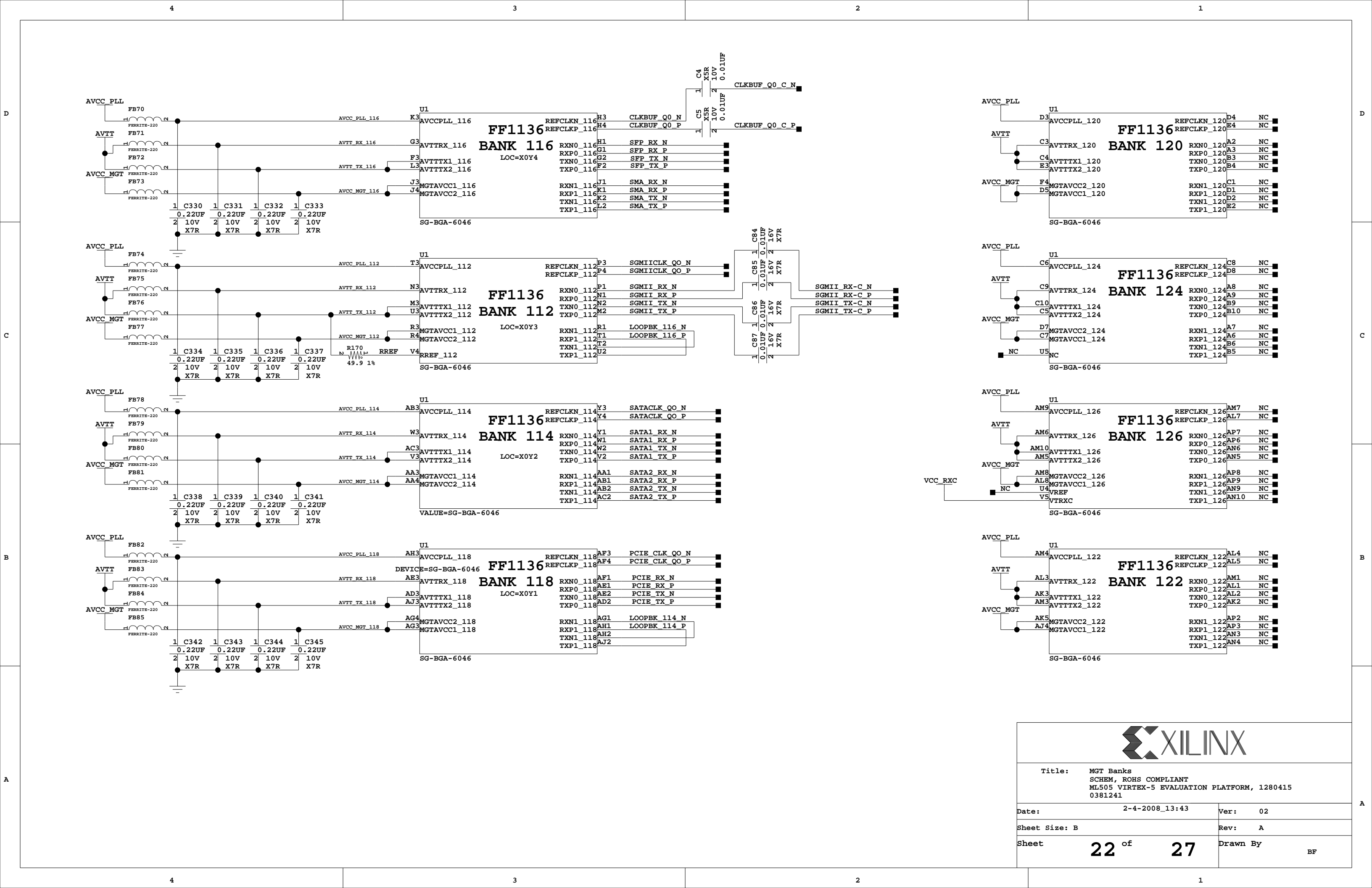


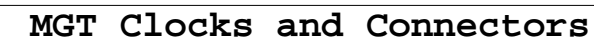
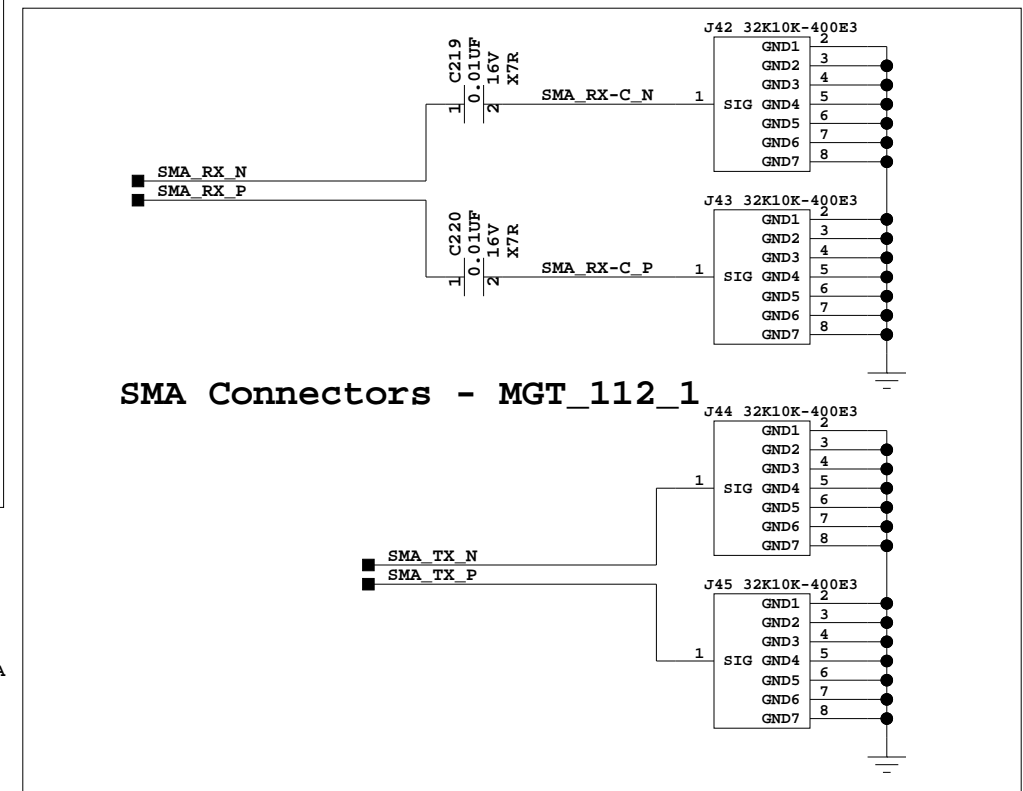
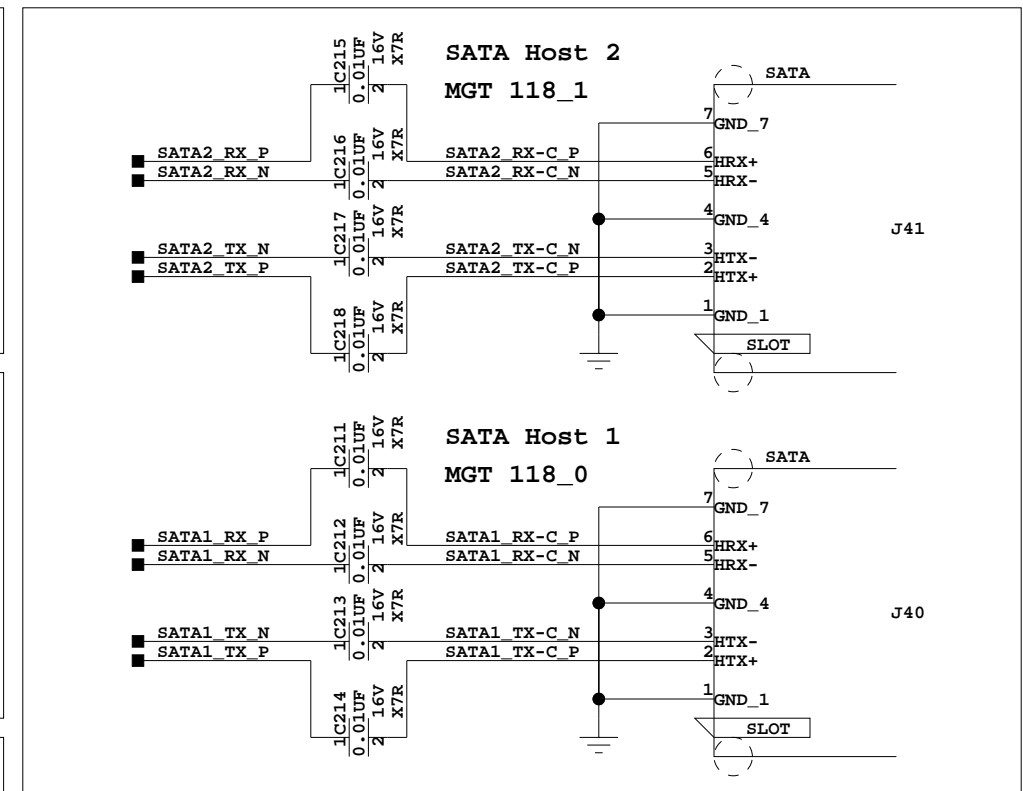
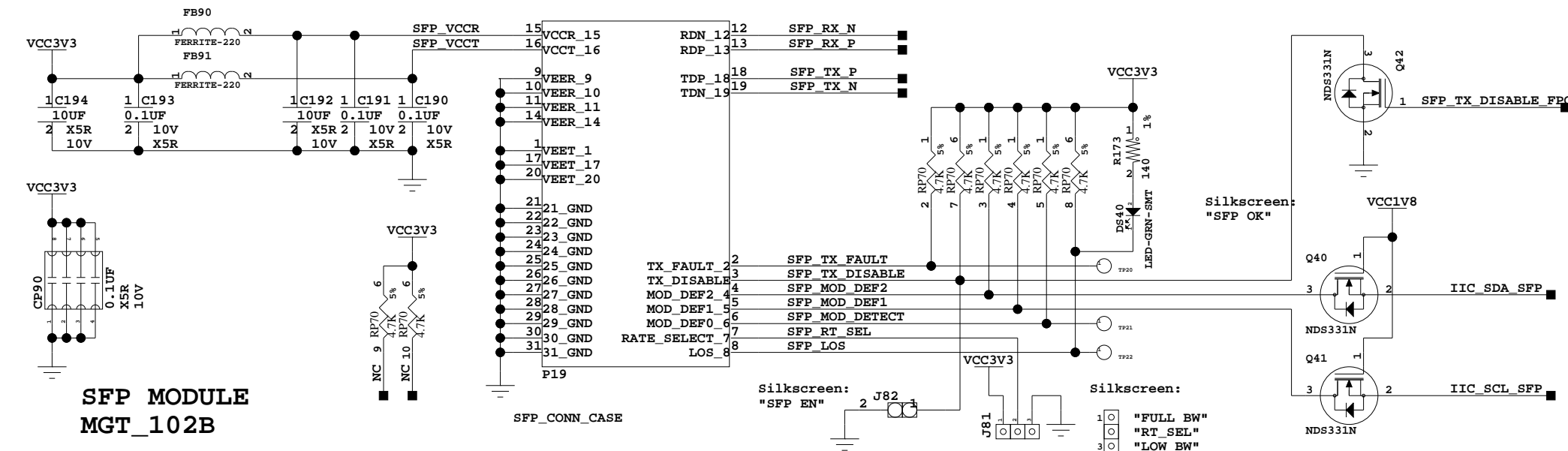
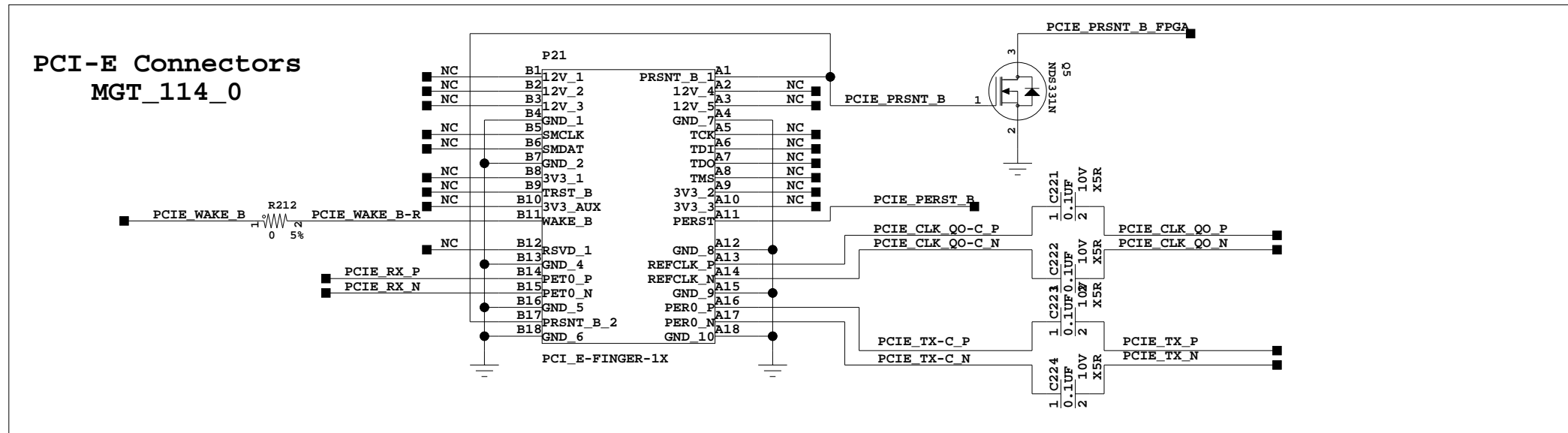
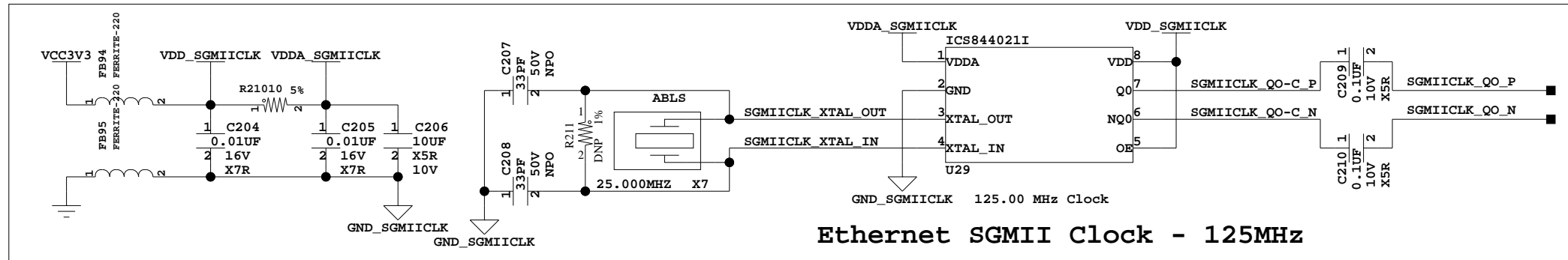
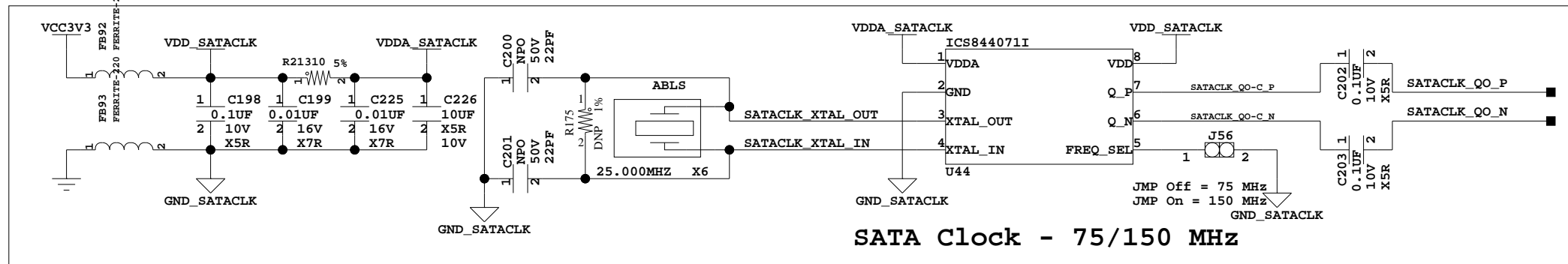
CPLD - Misc signal control



Title: CPLD - Misc signal control
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

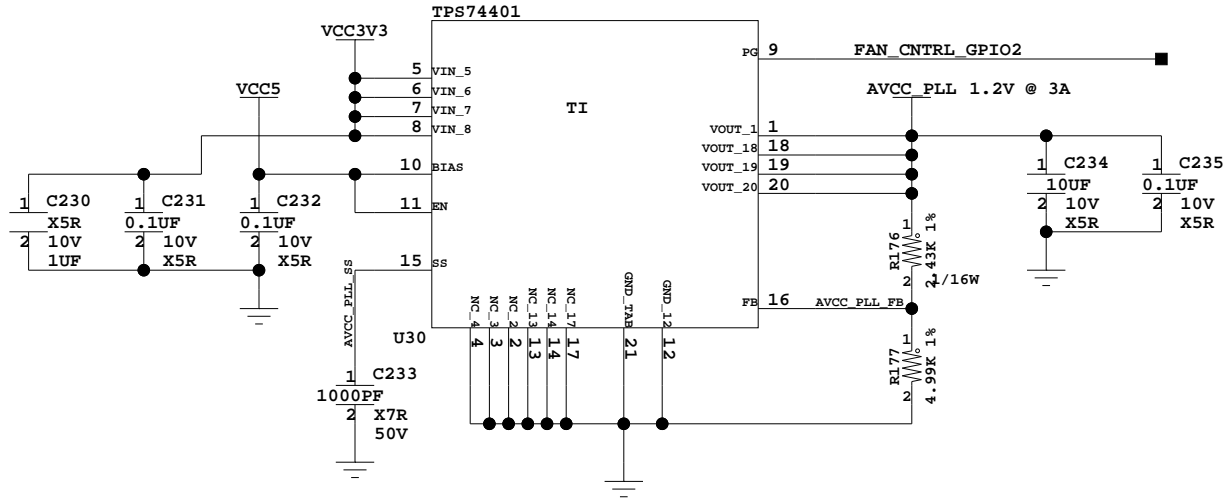
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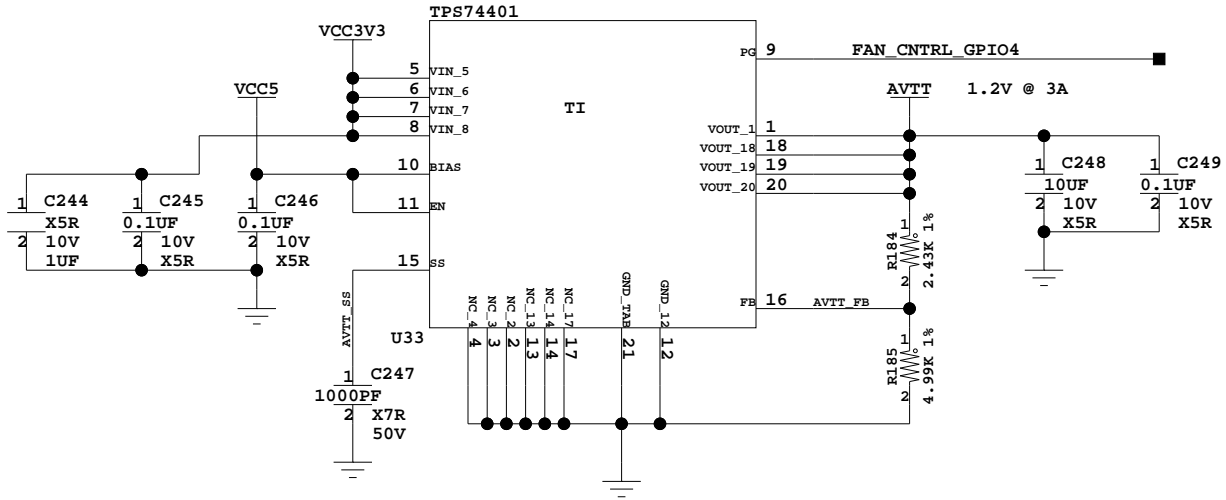


Title: MGT Connectors SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 12-5-2006_10:49	Ver: 02
Sheet Size: B	Rev: A
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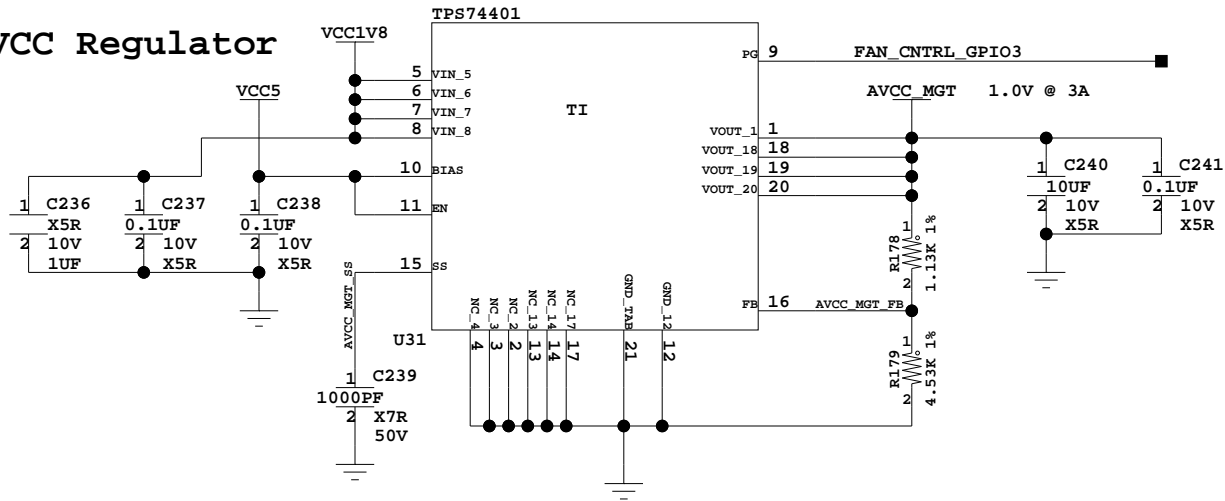
MGT PLL Regulator



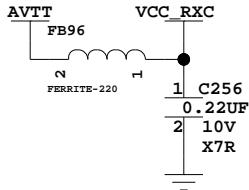
MGT VTT Regulator



MGT AVCC Regulator



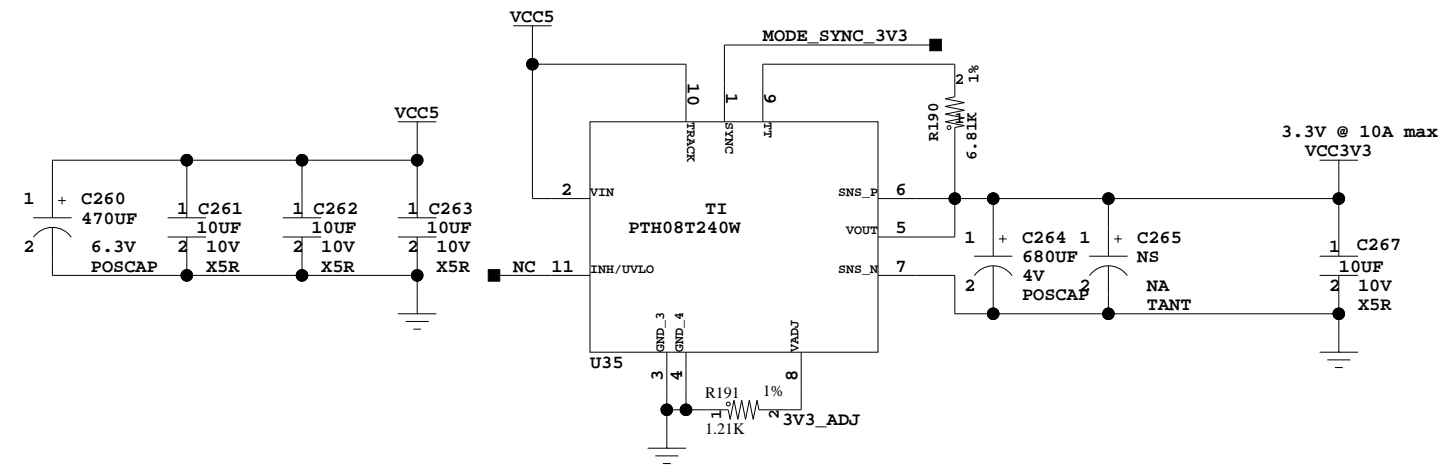
MGT RXC Regulator



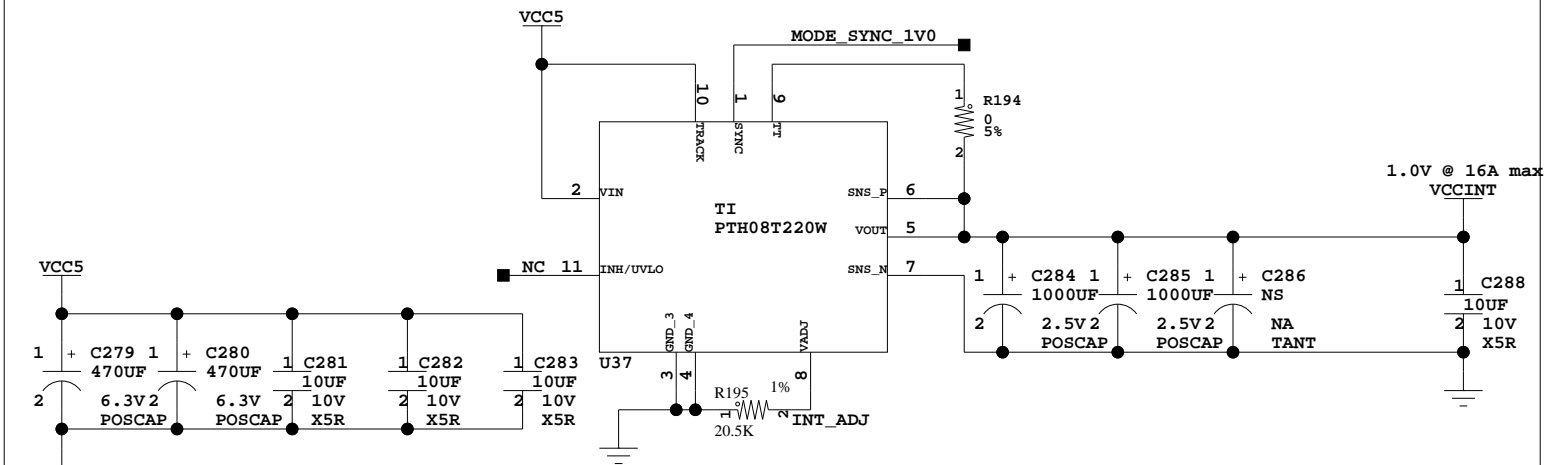
MGT Power Supplies

Title: MGT Power Supplies SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 12-5-2006_10:49	Ver: 02	
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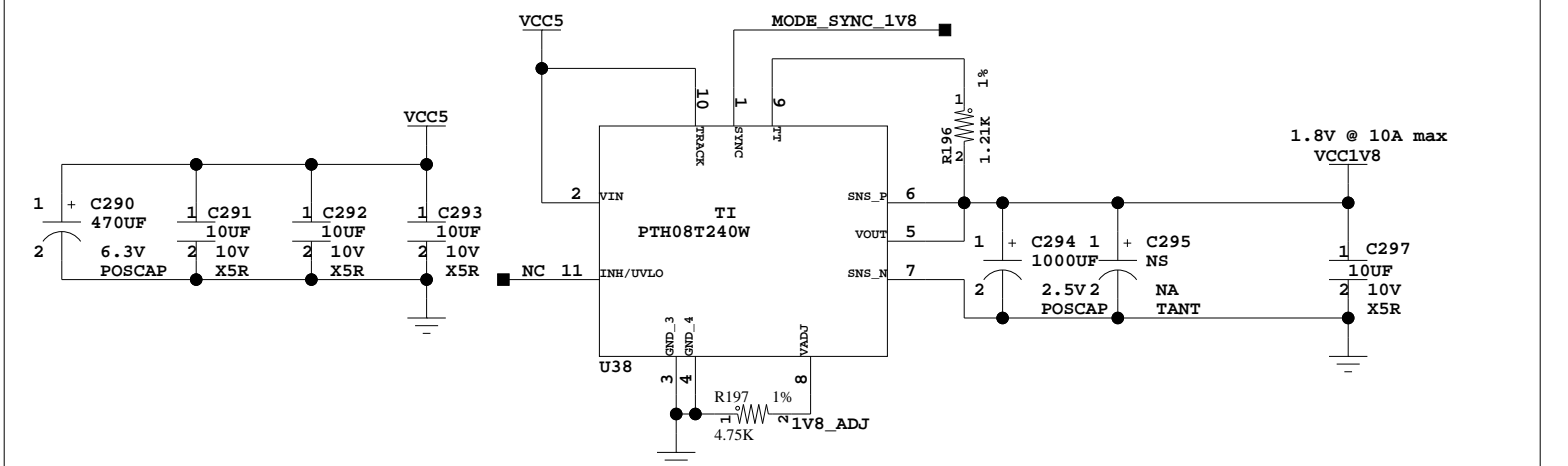
5v to 3.3V Regulator



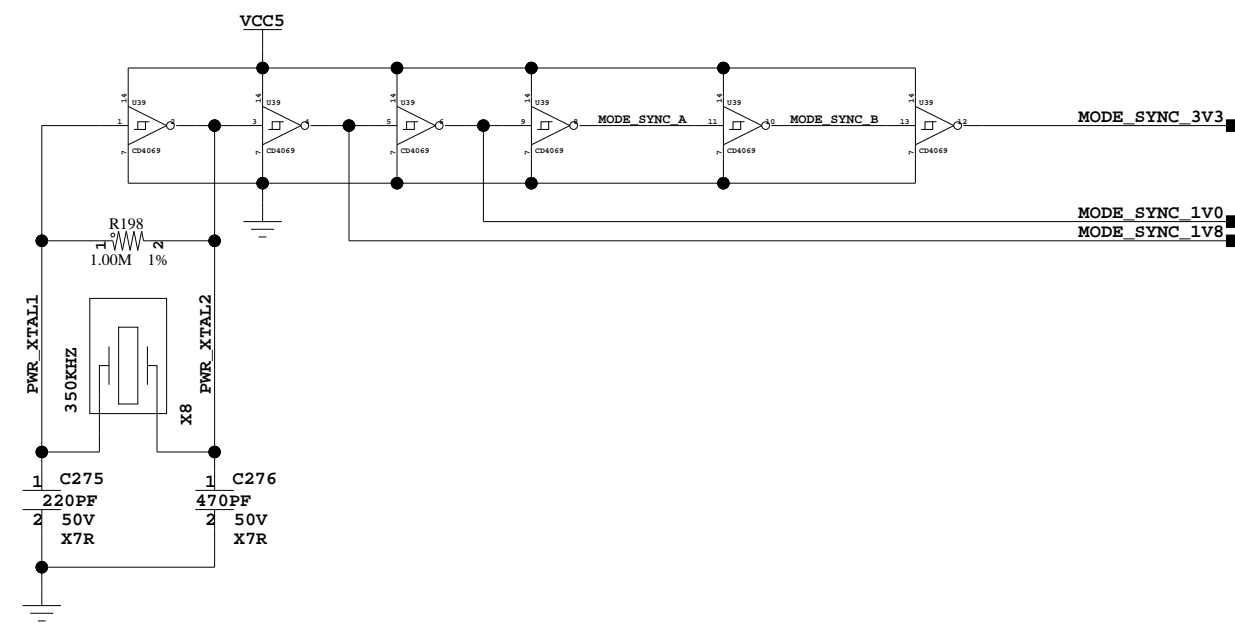
5v to 1.0V Regulator



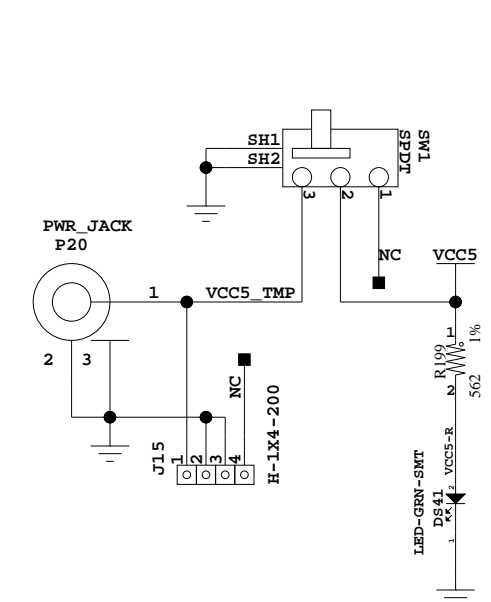
5v to 1.8V Regulator



5V Power Synchronizing Circuit



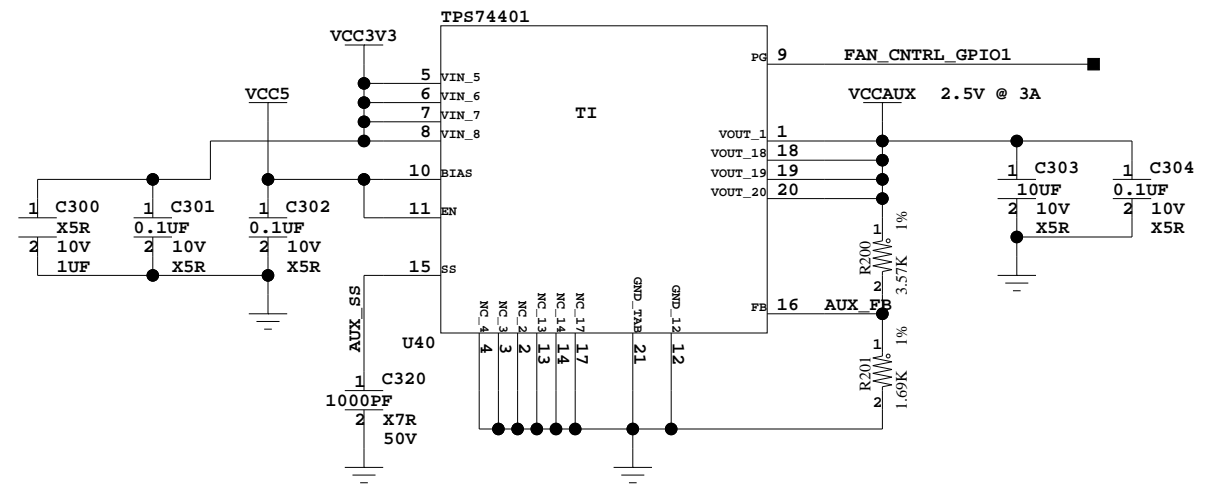
5V Power - Jack, Switch and LED



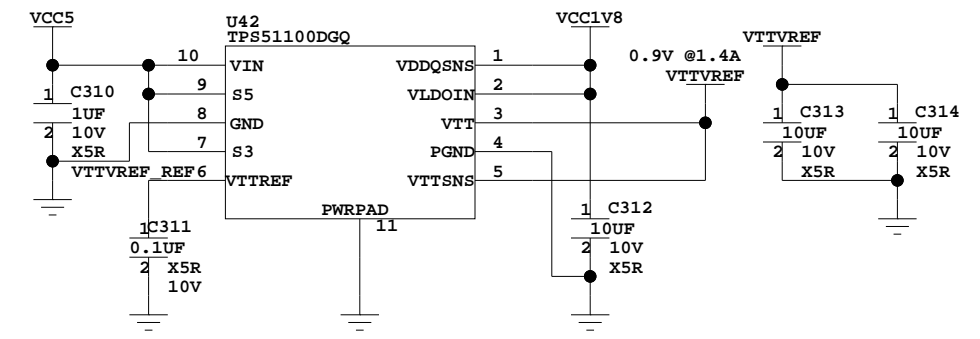
5V Power Supplies

Title: Power Supplies SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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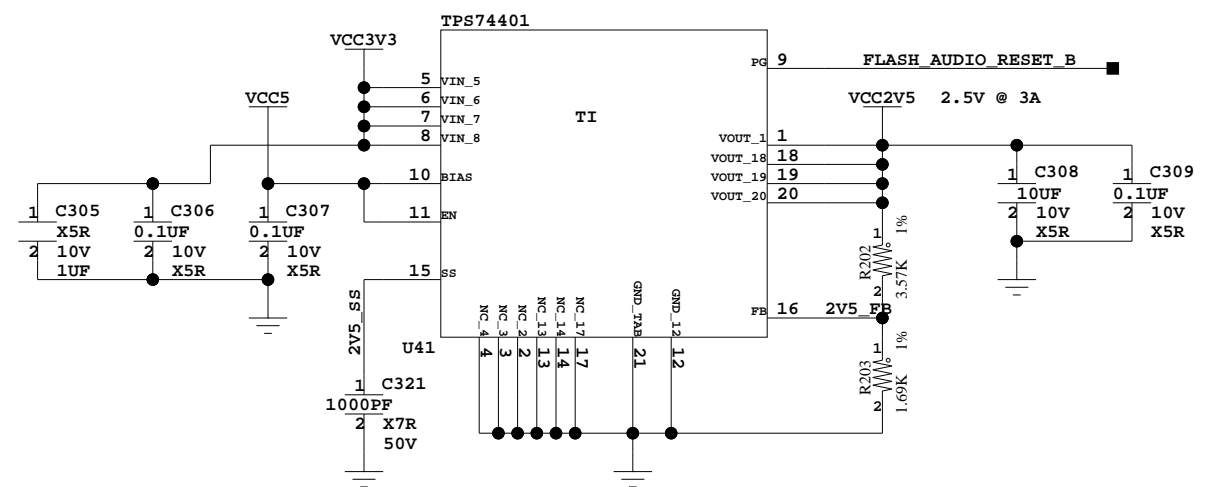
3.3v to 2.5V (VCC AUX) Regulator



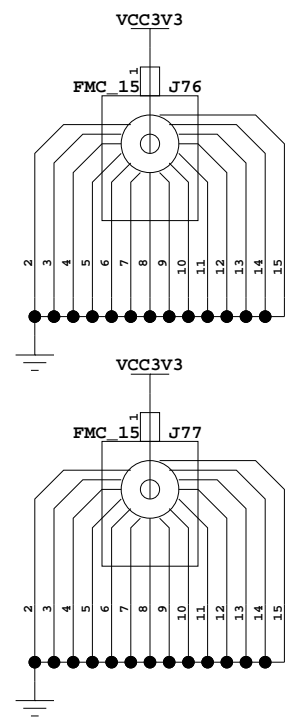
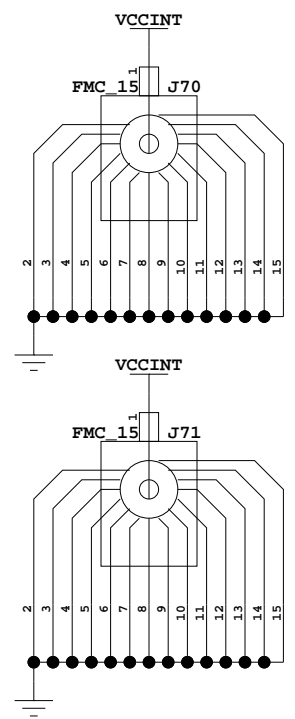
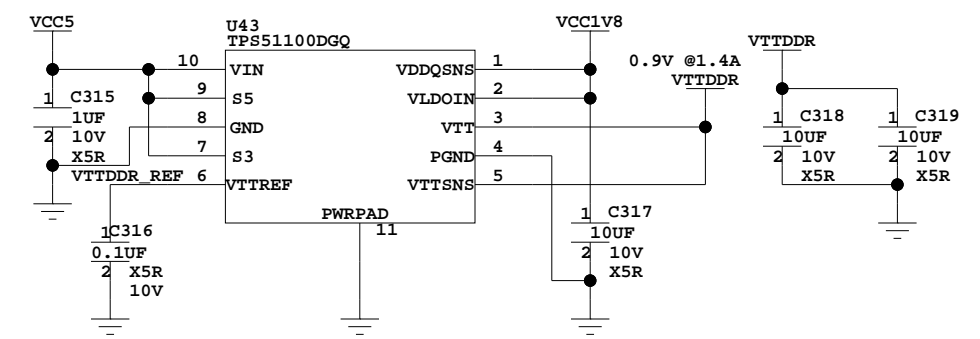
5V to 0.9V (DDR VTT VREF) Regulator



3.3v to 2.5V Regulator



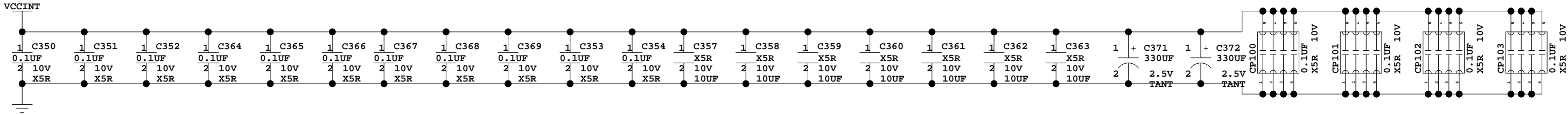
5V to 0.9V (DDR2 VTT DDR) Regulator



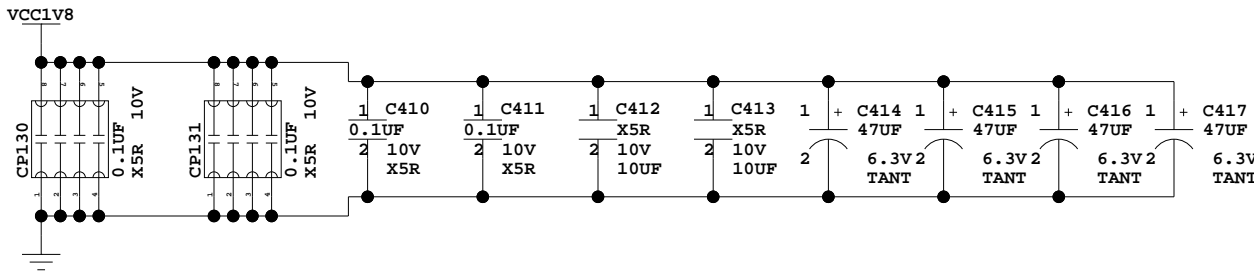
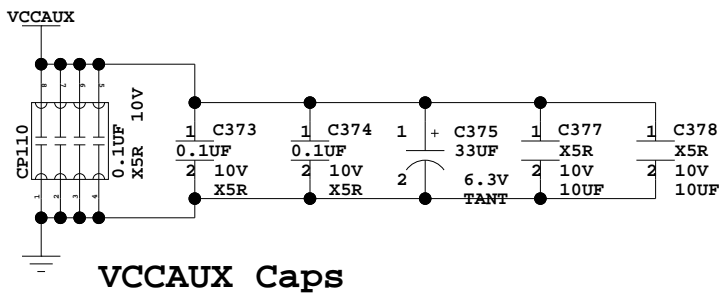
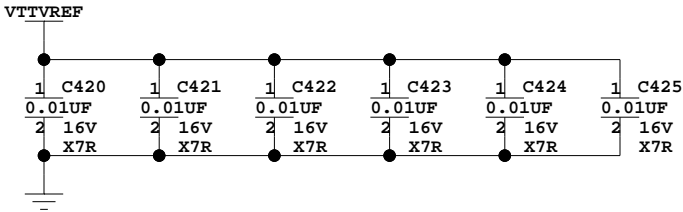
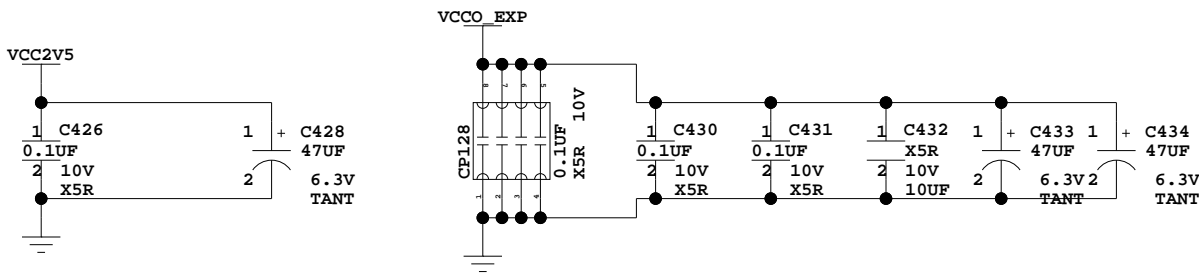
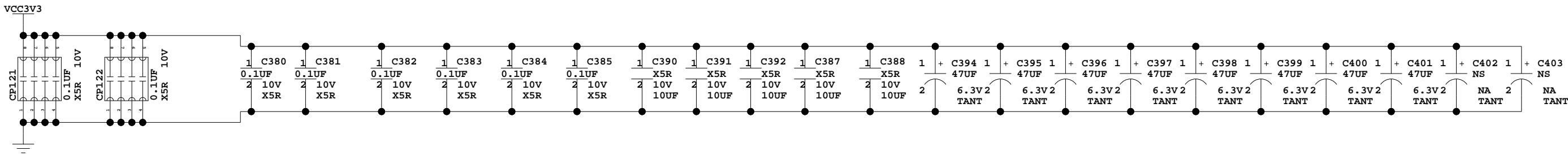
5V and 3.3V Power Supplies

Title: Power Supplies SCHEM, ROHS COMPLIANT ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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VCCINT Caps



VCCO Caps



Title: FPGA Decoupling
SCHEM, ROHS COMPLIANT
ML505 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241

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