SP601 Built-In Self Test Flash Application

March 2012
## Revision History

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<tr>
<td>07/23/10</td>
<td>12.2</td>
<td>Up-rev 12.1 BIST Design to 12.2. Set RZQ and ZIO pins in MPMC core GUI. See MPMC 6.01.a Product Specification for more details. Added <a href="#">AR36291</a> – MCB Data errors on initial programming of FPGA. Updated SI Labs USB UART Drivers URL</td>
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Overview

- Xilinx SP601 Board
- Software Requirements
- SP601 Setup
- SP601 BIST (Built-In Self Test)
- Compile SP601 BIST Design
- Program SP601 with BIST Design
- Program SP601 BPI
- References

Note: This presentation applies to the SP601
Description

- The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

Reference Design IP

- EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_iic, xps_mch_emc, xps_spi, util_io_mux, util_bus_split, xps_ethernetlite
  - Embedded System Tools Reference Guide (UG111)

Reference Design Source

- rdf0045.zip
- Available through http://www.xilinx.com/sp601

Note: Presentation applies to the SP601
Embedded Processor Design

- **The provided embedded reference design is supported “as is”**
  - Please refer to the click through license agreement

- **Embedded reference design has been verified on the SP601 Evaluation Kit**
  - Design consists of Early Access IP
  - Design may change in subsequent releases

- **The reference design will allow users to:**
  - Re-build and verify functionality on the SP601 evaluation kit

**Note:** Presentation applies to the SP601
Xilinx SP601 Board

Note: Presentation applies to the SP601
The SP601 MicroBlaze design hardware includes:

- DDR2 Interface (128 MB)
- BRAM
- External Memory Controller (EMC)
  - Flash Memory
- Networking
- UART
- Interrupt Controller
- GPIO (IIC, LEDs and LCD)
- Timer
- SPI
- PLB v46 Bus
ISE Software Requirement

- Xilinx ISE 13.4 software

Note: Presentation applies to the SP601
EDK Software Requirement

- Xilinx EDK 13.4 software
EDK Software Requirement

- Xilinx SDK 13.4 software

Note: Presentation applies to the SP601
SP601 Setup

- Power on the SP601 board for UART Driver Install

- Connect a USB Mini-B Cable to the USB UART connector on the SP601 board
  - Connect this cable to your PC
SP601 Setup

- **Install USB UART Drivers**
  - CP210x VCP Win XP S2K3 Vista 7.exe

*Note: Presentation applies to the SP601*
SP601 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager

Note: Presentation applies to the SP601
SP601 Setup

- **Expand the Ports Hardware**
  - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select Properties
SP601 Setup

- Under Port Settings tab
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4

Note: Presentation applies to the SP601
SP601 Setup

- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to 9600

Note: Tera Term may need to be restarted if board power is cycled
Set the mode pins for BPI Flash

- \( M0 = 0 \)
- \( M1 = 0 \)
**SP601 BIST**

- Press PROG and view initial BIST screen
  - Type “1” to start the UART Test

**Note:** As per [AR36291](http://www.example.com/AR36291), hold the PROG button for an extra second or two if seeing errors.
**SP601 BIST**

- **UART Test completed**
  - Press **PROG** and type **2** to begin LED Test

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**Note:** Presentation applies to the SP601
SP601 BIST

- LED Test completed
  - Press PROG and type 3 to begin Timer Test
- Timer Test completed
  - Press PROG and type 4 to begin Flash test

**Note:** Do not press PROG until this test completes
**SP601 BIST**

- **Flash Test completed**
  - Press **PROG** and type **5** to begin IIC EEPROM Test

*Note: Presentation applies to the SP601*
SP601 BIST

- IIC EEPROM Test completed
  - Press PROG and type 6 to begin Ethernetlite Test

Note: Presentation applies to the SP601
SP601 BIST

- Ethernetlite Test completed
  - Press **PROG** and type 7 to begin GPIO Switch Test

*Note*: Presentation applies to the SP601
**SP601 BIST**

- **GPIO Switch Test completed**
  - Press **PROG** and type **8** to begin External Memory Test

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**Note:** Presentation applies to the SP601
SP601 BIST

- External Memory Test running with caches on

Note: Presentation applies to the SP601
Second part of External Memory test (caches off)

```
Pass B> ICache: Off, DCache: Off
TEST0: Write all memory to 0x00000000 and check
  Writing...
  Reading...
  Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
  Writing...
  Reading...
  Test Complete Status = SUCCESS
TEST2: Testing for stuck together bank/row/col bits
  Clearing memory to zeros...
  Writing and Reading...
  Test Complete Status = SUCCESS
TEST3: Testing for maximum ba/row/col noise
  This test performs 16 word writes followed by 16 word reads
  Each 64 bytes inverts the ba/row/col address
  Initializing Memory to 0xA5A5A5A5...
  Writing and Reading...
  Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
  Writing...
  Reading...
  Test Complete Status = SUCCESS

Number of errors in this pass = 0

MPMC memory test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
Press the 'PROG' button to continue.
```
Compile SP601 BIST Design
Compile SP601 BIST Design

- Unzip the rdf0045.zip file
  - Available through http://www.xilinx.com/sp601
  - Includes AR32713 – Recommended constraints for the XPS_LL_TEMAC systems

Note: Presentation applies to the SP601
Compile SP601 BIST Design

- If desired, FPGA compile can be skipped by opening SDK directly:
  Start → All Programs → Xilinx ISE Design Suite 13.4 → EDK → Xilinx Software Development Kit

- Select the workspace: `<design files>\SDK\SDK_Workspace_35`

- Go to **SDK Software Compile**
Compile SP601 BIST Design

- Open XPS project `<project directory>\system.xmp`
- Create the hardware design, `system.bit`, located in `<project directory>\implementation`
  - Click the Generate Bitstream button (1)
  - Or from the menu, select Hardware → Generate Bitstream

Note: Presentation applies to the SP601
Compile SP601 BIST Design

- **Open SDK**
  - Click the **Export Design** button (1)
  - Click **Export & Launch SDK** (2)

**Note:** Presentation applies to the SP601
Compile SP601 BIST Design

- **SDK Software Compile**
  - Build ELF files in SDK
  - Select **Project → Build All** (1)
  - **Note:** If by-passing the FPGA compile, the ELF files are already built; if desired, the ELF files can be re-built by selecting **Clean...** followed by **Build All**
Program SP601 with BIST Design
Program SP601 with BIST Design

- Add a second USB Type-A to Mini-B cable to the USB JTAG connector on the SP601 board
  - Connect this cable to your PC
Program SP601 with BIST Design

- Init memory with the Bootloop ELF
  - Update the bitstream (download.bit) with the Bootloop ELF
  - Select Xilinx Tools → Program FPGA (1)
Program SP601 with BIST Design

- Init memory with the Bootloader Application ELF
  - Select bootloop (1)
  - Click Program

Note: Verify the Bitstream and BMM File paths match your design path
Program SP601 with BIST Design

- **Launch XMD**
  - Select *Xilinx Tools → XMD Console* (1)
Program SP601 with BIST Design

- **Connect XMD to the MicroBlaze:**
  
  ```
  cd C:/sp601_bist/SDK/SDK_Workspace_35
  connect mb mdm
  ```
Program SP601 with BIST Design

- Download the bootloader with xmd:
  
dow bootloader/Debug/bootloader.elf
Program SP601 with BIST Design

- Download the bootloader with xmd:
  
  `con`
Program SP601 with BIST Design

- Bootloader runs in the terminal window

** Note: Presentation applies to the SP601 **
Program SP601 with BIST Design

- **Init memory with the Bootloader ELF**
  - Update the bitstream (download.bit) with the *Bootloader* ELF
  - Select *Xilinx Tools* → *Program FPGA* (1)
Program SP601 with BIST Design

- Init memory with the Bootloader Application ELF
  - Select `<Design Files>\SDK\SDK_Workspace_35\bootloader\Debug\bootloader.elf`
  - Click Program

**Note:** Always reselect the desired ELF file at this step.
Program SP601 with BIST Design

- Bootloader runs in the terminal window

**Note:** Presentation applies to the SP601
Program SP601 BPI
Program SP601 BPI

- The bitstream must be converted to hex format (.bin) prior to programming into flash
  - Select Xilinx Tools → Launch Shell (1)
Program SP601 BPI

- Generate a BIN file from the bitstream

```bash
promgen -w -p bin -c FF -o hw_platform_0/download.bin -u 0 hw_platform_0/download.bit
```

Note: Presentation applies to the SP601
Program SP601 BPI

- **Program the bitstream and ELF files into BPI Flash**
  - Select Xilinx Tools → Program Flash Memory (1)
  - FPGA must contain the BIST bitstream at this point
Program SP601 BPI

- Program the BPI Flash with the bitstream bin file
  - Bitstream `hw_platform_0/download.bin`
  - Offset: `0x00000000`
  - Working Memory: `DDR2_SDRAM`

Note: Click Program after the data is entered
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: hello_uart/Debug/hello_uart.elf
  - Select Auto-convert to SREC
  - Offset: 0x00120000
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: hello_gpio/
    Debug/hello_gpio.elf
  - Select Auto-convert to SREC
  - Offset: 0x00140000
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: hello_timer/Debug/hello_timer.elf
  - Select Auto-convert to SREC
  - Offset: 0x00160000
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program the BPI Flash with an SREC file:
- ELF: hello_flash/Debug/hello_flash.elf
- Select Auto-convert to SREC
- Offset: 0x00180000
- Working Memory: DDR2_SDRAM
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: hello_iic/
    Debug/hello_iic.elf
  - Select Auto-convert to SREC
  - Offset: 0x001a0000
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: hello_emac/Debug/hello_emac.elf
  - Select Auto-convert to SREC
  - Offset: 0x001c0000
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: hello_switch/Debug/hello_switch.elf
  - Select Auto-convert to SREC
  - Offset: 0x001e0000
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program SP601 BPI

- Program the BPI Flash with an SREC file:
  - ELF: `hello_mem/Debug/hello_mem.elf`
  - Select Auto-convert to SREC
  - Offset: `0x00200000`
  - Working Memory: DDR2_SDRAM

Note: Presentation applies to the SP601
Program SP601 BPI

- Press PROG and view initial BIST screen
  - Type “1” to start the UART Test
References

- **EDK Documentation**
  - Embedded System Tools Reference Guide

- **Spartan-6 Configuration**
  - Spartan-6 FPGA Configuration User Guide
Documentation

- **Spartan-6**
  - Spartan-6 FPGA Family

- **SP601 Documentation**
  - Spartan-6 FPGA SP601 Evaluation Kit
  - SP601 Getting Started Guide
  - SP601 Hardware User Guide
  - SP601 Reference Design User Guide