

# ML510 Reference Design

## *User Guide*

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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/25/08	1.0	Initial Xilinx release.
08/29/08	1.0.1	Minor typographical edit.
10/17/08	1.1	Updated <a href="#">Table 1, page 11</a> . Added " <a href="#">Memory Interface Generator (MIG) Design</a> ." Minor typographical edits throughout.
06/23/09	1.2	Updated <a href="#">Table 1, page 11</a> and content to match published files for 11.1. Fixed links and references.

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## About This Guide

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This user guide introduces several designs that demonstrate Virtex®-5 FPGA features using the ML510 (FXT) Embedded Development Platform. The provided designs include processing systems based on the embedded PowerPC® 440 processor block, the MicroBlaze™ soft processor, the integrated Tri-mode Ethernet MAC, and the RocketIO™ GTX transceiver.

### Additional Documentation

The following documents are also available for download at <http://www.xilinx.com/virtex5>.

- Virtex-5 Family Overview  
The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics  
This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.
- Virtex-5 FPGA User Guide  
Chapters in this user guide cover the following topics:
  - ◆ Clocking Resources
  - ◆ Clock Management Technology (CMT)
  - ◆ Phase-Locked Loops (PLLs)
  - ◆ Block RAM
  - ◆ Configurable Logic Blocks (CLBs)
  - ◆ SelectIO™ Resources
  - ◆ SelectIO Logic Resources
  - ◆ Advanced SelectIO Logic Resources
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide  
This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.
- Embedded Processor Block in Virtex-5 FPGAs Reference Guide  
This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.

- **Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller**  
This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.
- **Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs**  
This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.
- **XtremeDSP Design Considerations**  
This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.
- **Virtex-5 FPGA Configuration Guide**  
This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- **Virtex-5 FPGA Packaging and Pinout Specifications**  
This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- **Virtex-5 PCB Designer's Guide**  
This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

## Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at:  
<http://www.xilinx.com/support>.

## Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
<i>Italic font</i>	References to other documents	See the Virtex-5 <i>FPGA Configuration Guide</i> for more information.
	Emphasis in text	The address (F) is asserted <i>after</i> clock event 2.
<u>Underlined Text</u>	Indicates a link to a web page.	<a href="http://www.xilinx.com/virtex5">http://www.xilinx.com/virtex5</a>

## Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “ <a href="#">Additional Documentation</a> ” for details. Refer to “ <a href="#">System Monitor Primitive</a> ” for details.
Red text	Cross-reference link to a location in another document	See <a href="#">Figure 2</a> in the <i>Virtex-5 Data Sheet</i>
<a href="#">Blue, underlined text</a>	Hyperlink to a website (URL)	Go to <a href="http://www.xilinx.com">http://www.xilinx.com</a> for the latest documentation.



# ML510 Reference Design

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## Introduction

The Virtex®-5 FPGA family [Ref 1] offers designers multiple platforms with an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing resources. All members of the Virtex-5 FPGA family are built using the second generation Advanced Silicon Modular Block (ASMBL™) technology and a state-of-the-art 65 nm copper process to produce the industry's highest performance FPGAs. In addition to the embedded PowerPC™ 440 processor block, integrated system-level hard-IP blocks for PCI Express® (PCIe®), Tri-mode Ethernet, and advanced high-speed RocketIO™ GTP and GTX serial transceivers are also provided through the Virtex-5 FPGA family.

Along with capabilities offered directly through an integrated IP block implemented in silicon, the Xilinx [LogiCORE IP](#) catalog and the [embedded processing IP](#) catalog are available to system level designers. For designers utilizing the RocketIO GTX transceivers, the [Chipscope™ Pro Serial I/O Toolkit](#) offers the fastest way to setup and begin using the high-speed serial I/O channels. A design using the Xilinx Memory Interface Generator (MIG) tool is also provided to show an easy way to design, implement, and verify external memory interfaces. [Ref 19]

As an embedded development board, the ML510 is useful for exercising the new architectural features of the Virtex-5 FPGA and as a platform to create user designs. The ML510 is populated with an XC5VFX130T device.

Users can obtain a quick understanding of the features offered by the ML510 board by running the demonstration content provided on the CompactFlash (CF) card included with the board.

## Reference Designs

### EDK Design

The ML510 platform utilizes the Embedded Development Kit (EDK) and the Base System Builder (BSB) wizard to create an embedded processing system. The BSB wizard helps designers quickly create a working embedded system using a point-and-click graphical user interface (GUI) to select a Xilinx processor and an associated set of peripherals. Processing systems using either the MicroBlaze soft processor or the embedded PowerPC 440 block can be generated by BSB. BSB designs can be further customized within the Xilinx Platform Studio (XPS) environment by leveraging the extensive set of peripherals offered through the EDK IP catalog.

BSB-generated designs for the ML510 are available at:

- [www.xilinx.com/products/boards/ml510/reference\\_designs.htm#bsb\\_design](http://www.xilinx.com/products/boards/ml510/reference_designs.htm#bsb_design)

Older revisions of the designs can be found by clicking on “Previous Revisions” on the ML510 Reference Designs Web page.

## PowerPC 440 Processor

The ML510 platform supports a set of software applications and hardware designs that utilize the integrated PPC440 hard processor block. The BSB design Web page lists multiple PowerPC 440 reference designs along with documentation on how to create these designs using the BSB wizard and XPS. Designs that use the Virtex-5 FXT integrated PowerPC 440 processor block are labeled with the *\_ppc440* suffix in their names. The BSB1 set of designs utilize the DDR2 DIMM0 memory, whereas the BSB2 set of designs use the second provided DDR2 DIMM1.

The strategy of beginning with a known good BSB design and deriving new designs with additional capabilities offers a quick way to generate a variety of designs and the ability to debug designs using incremental changes.

- EDK BSB base design
  - ◆ ml510\_bsb1\_design\_ppc440.zip
  - ◆ ml510\_bsb2\_design\_ppc440.zip

The base design is an out-of-the-box BSB design that demonstrates many of the features offered on the board. BSB1 designs utilize DIMM0; BSB2 designs utilize DIMM1.

- EDK BSB design with standard IP (STD IP) addition
  - ◆ ml510\_bsb1\_std\_ip\_ppc440.zip
  - ◆ ml510\_bsb2\_std\_ip\_ppc440.zip

This design is derived from the base design by using XPS to add or modify standard supported EDK peripherals. The standard IP addition is identical to the BSB base design with one exception: for the BSB1 STD IP design, the Ethernet PHY interface is modified from MII to RGMII; for the BSB2 STD IP design, the MII interface is modified to SGMII.

- EDK standard IP design with pcores addition
  - ◆ ml510\_bsb1\_pcores\_ppc440.zip

This design adds a frame-buffer-based video output port to the base design. The PLB v4.6 DVI/VGA pcore that drives the video port was created by using EDK’s Create and Import Peripheral wizard as a template.

An application demonstrating the EDK port of the open source Lightweight IP (lwIP) networking library is also provided. The Xilinx Ethernet xps\_ll\_temac MAC is used to demonstrate RGMII and SGMII PHY interfaces with lwIP’s *sockets* mode Application Program Interface (API). The EDK *OS and Libraries Document Collection* provides additional details on using the lwIP networking library. [Ref 15]

## MicroBlaze Processor

In addition to supporting PowerPC 440 processor designs, the ML510 supports MicroBlaze soft processor designs. Two sets of BSB-generated designs are provided. The first set is located in the BSB1 section of the BSB designs page and targets the DDR2 DIMM0 memory. The second set is available in the BSB2 section that uses the DDR2 DIMM1 along with a smaller subset of peripherals than the BSB1 design. A common set of PLBv46 peripherals from the EDK IP catalog are used across the MicroBlaze and PowerPC processor designs.

- EDK BSB1 designs
  - ◆ ml510\_bsb1\_design.zip
- EDK BSB2 designs
  - ◆ ml510\_bsb2\_design.zip

## Stand-Alone Software Applications

Stand-alone software applications (Table 1) are provided to verify board functionality. These applications can be compiled within EDK and downloaded to the ML510 over a JTAG download cable. Pre-built bitstreams, ELF and ACE files, and readme .txt files that explain how to run the applications for the ML510 are available at:

- [www.xilinx.com/products/boards/ml510/ml510\\_11.1\\_1/standalone\\_apps\\_ppc440.htm](http://www.xilinx.com/products/boards/ml510/ml510_11.1_1/standalone_apps_ppc440.htm)
- [www.xilinx.com/products/boards/ml510/ml510\\_11.1\\_1/standalone\\_apps.htm](http://www.xilinx.com/products/boards/ml510/ml510_11.1_1/standalone_apps.htm)

Table 1: Software Applications (PPC440 Processor)

ML510 Designs	Feature Tested / Description
ml510_standalone_apps_ppc440_bit_elf_ace.zip	Complete collection of stand-alone applications and board test BIT, ELF, and ACE files.  To run each application individually, select one of the ACE files below and replace the my_ace.ace in configuration address 6 of the production ML510 CF card.
<b>BSB1 + STD IP Designs</b>	
ml510_bsb1_std_ip_ppc440_bootloop.bit ml510_bsb1_ppc440_testapp_mem.elf ml510_bsb1_ppc440_testapp_mem.ace testapp_memory_readme.txt	Tests DIMM0 DDR2 memory.
ml510_bsb1_ppc440_bootloop.bit ml510_bsb1_ppc440_testapp_periph.elf ml510_bsb1_ppc440_testapp_periph.ace testapp_peripheral_readme.txt	Tests the following peripherals: <ul style="list-style-type: none"> <li>• DDR2_SDRAM_DIMM0</li> <li>• FLASH</li> <li>• Hard_Ethernet_MAC</li> <li>• IIC_EEPROM</li> <li>• LCD_OPTIONAL</li> <li>• LEDs_4Bit</li> <li>• RS232_Uart_1</li> <li>• SPI_EEPROM</li> <li>• SysACE_CompactFlash</li> <li>• plb_v46</li> <li>• xps_intc</li> </ul>

Table 1: Software Applications (PPC440 Processor) (Cont'd)

ML510 Designs	Feature Tested / Description
<b>BSB 1 + STD IP Design</b>	
ml510_bsb1_std_ip_ppc440_bootloop.bit ace_loader.elf ace_loader.ace ace_loader_readme.txt	Main menu to load and launch ACE file demonstrations.
ml510_bsb1_std_ip_ppc440_bootloop.bit ddr_mem_test.elf ddr_mem_test.ace ddr_mem_test_readme.txt	DIMM0 memory test.
ml510_bsb1_std_ip_ppc440_bootloop.bit hello.elf hello.ace hello_readme.txt	Exercises serial port output and input functionality using libc routines.
ml510_bsb1_std_ip_ppc440_bootloop.bit hello_dip.elf hello_dip.ace hello_dip_readme.txt	Verifies functionality of GPIO DIP switches, GPIO LEDs.
ml510_bsb1_std_ip_ppc440_bootloop.bit hello_lcd.elf hello_lcd.ace hello_lcd_readme.txt	Verifies functionality of LCD display.
ml510_bsb1_std_ip_ppc440_bootloop.bit hello_spi.elf hello_spi.ace hello_spi_readme.txt	Placeholder application for a user-generated SPI Flash design. Loaded from SPI Flash.
ml510_bsb1_std_ip_ppc440_bootloop.bit hello_uart.elf hello_uart.ace hello_uart_readme.txt	Exercises serial port output and input functionality using low-level UART driver routines on UART #1.
ml510_bsb1_std_ip_ppc440_bootloop.bit iic_ddr2_dimm0.elf iic_ddr2_dimm0.ace iic_ddr2_dimm0_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access DIMM0.
ml510_bsb1_std_ip_ppc440_bootloop.bit iic_ddr2_dimm1.elf iic_ddr2_dimm1.ace iic_ddr2_dimm1_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access DIMM1.
ml510_bsb1_std_ip_ppc440_bootloop.bit iic_eeprom.elf iic_eeprom.ace iic_eeprom_readme.txt	IIC dynamic mode EEPROM access example.
ml510_bsb1_std_ip_ppc440_bootloop.bit iic_fan.elf iic_fan.ace iic_fan_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the fan controller.

**Table 1: Software Applications (PPC440 Processor) (Cont'd)**

<b>ML510 Designs</b>	<b>Feature Tested / Description</b>
ml510_bsb1_std_ip_ppc440_bootloop.bit iic_pcie.elf iic_pcie.ace iic_pcie_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the PCIe slot power controller chip.
ml510_bsb1_std_ip_ppc440_bootloop.bit iic_temp_voltage.elf iic_temp_voltage.ace iic_temp_voltage_readme.txt	Uses the Xilinx IIC peripheral in dynamic mode along with its low-level driver to access the temperature and voltage monitor chip.
ml510_bsb1_std_ip_ppc440_bootloop.bit lwipdemo_rgmii.elf lwipdemo_rgmii.ace lwipdemo_rgmii_readme.txt	Uses LWIP in sockets mode for a Web server.
ml510_bsb1_std_ip_ppc440_bootloop.bit real_time_clock.elf real_time_clock.ace real_time_clock_readme.txt	User-selectable loading of ACE files utilizing the System ACE CF controller.
ml510_bsb1_std_ip_ppc440_bootloop.bit set_eeprom.elf set_eeprom.ace set_eeprom_readme.txt	Tests the EEPROM chip.
ml510_bsb1_std_ip_ppc440_bootloop.bit slideshow.elf slideshow.ace slides.zip slideshow_readme.txt	A self-running audio and video presentation highlighting features of the ML510 and the Virtex-5 FPGA.
ml510_bsb1_std_ip_ppc440_bootloop.bit testfatfs.elf testfatfs.ace testfatfs.zip testfatfs_readme.txt	Performs write and read tests of the FAT file system on the CompactFlash card.
ml510_bsb1_std_ip_ppc440_bootloop.bit xflash.elf xflash.ace xflash_readme.txt	Tests linear flash memory.
<b>BSB 1 + STD IP + PCOREs Design</b>	
ml510_bsb1_pcores_ppc440_bootloop.bit hello_pci.elf hello_pci.ace hello_pci_readme.txt	Scans PCI bus.
<b>BSB2 (DIMM1) Design</b>	
ml510_bsb2_ppc440_bootloop.bit ml510_bsb2_ppc440_testapp_mem.elf ml510_bsb2_ppc440_testapp_mem.ace testapp_memory_readme.txt	Tests DIMM1 DDR2 memory.

Table 1: Software Applications (PPC440 Processor) (Cont'd)

ML510 Designs	Feature Tested / Description
ml510_bsb2_ppc440_bootloop.bit ml510_bsb2_ppc440_testapp_periph.elf ml510_bsb2_ppc440_testapp_periph.ace testapp_peripheral_readme.txt	Tests the following peripherals: <ul style="list-style-type: none"> <li>• DDR2_SDRAM_DIMM1</li> <li>• Hard_Ethernet_MAC</li> <li>• RS232_Uart_2</li> <li>• SysACE_CompactFlash</li> <li>• plb_v46</li> <li>• xps_intc</li> </ul>
<b>BSB2 + Standard IP Design</b>	
ml510_bsb2_std_ip_ppc440_bootloop.bit lwipdemo_sgmi.elf lwipdemo_sgmi.ace lwipdemo_sgmi_readme.txt	Uses LWIP in sockets mode for a Web server.
<b>Dual Processor Design (BSB1 + BSB2)</b>	
ml510_dual_ppc440_bootloop.bit ml510_dual_ppc440_testapp_mem_0.elf ml510_dual_ppc440_testapp_mem_1.elf ml510_dual_ppc440_testapp_mem.ace testapp_memory_readme.txt	Tests DIMM0 and DIMM1 DDR2 memory.
ml510_dual_ppc440_bootloop.bit ml510_dual_ppc440_testapp_periph_0.elf ml510_dual_ppc440_testapp_periph_1.elf ml510_dual_ppc440_testapp_periph.ace testapp_peripheral_readme.txt	Tests the following peripherals for DDR2_SDRAM_DIMM0: <ul style="list-style-type: none"> <li>• FLASH</li> <li>• Hard_Ethernet_MAC</li> <li>• IIC_EEPROM</li> <li>• LCD_OPTIONAL</li> <li>• LEDs_4Bit</li> <li>• RS232_Uart_1</li> <li>• SPI_EEPROM</li> <li>• SysACE_CompactFlash</li> <li>• plb_v46</li> <li>• xps_intc</li> </ul> Tests the following peripherals for DDR2_SDRAM_DIMM1: <ul style="list-style-type: none"> <li>• Hard_Ethernet_MAC</li> <li>• RS232_Uart_2</li> <li>• plb_v46</li> <li>• xps_intc</li> </ul>

## ChipScope Pro Serial I/O Toolkit IBERT Design

The ChipScope Pro Serial I/O Toolkit [Ref 17] provides the ability to generate a hardware design to exercise the Virtex-5 FPGA RocketIO GTX transceivers [Ref 5]. After querying the user for the device part and package, the location of a system clock pin, the dedicated RocketIO GTX clock pins, and the expected transceiver line rates, the ChipScope Pro software generates a bitstream that implements an Integrated Bit Error Ratio Tester

(IBERT). The IBERT design is easily scalable to user board designs. A pre-built IBERT design and tutorial is available for the ML510 at:

- [www.xilinx.com/products/boards/ml510/reference\\_designs.htm#ibert\\_design](http://www.xilinx.com/products/boards/ml510/reference_designs.htm#ibert_design)

Figure 1 shows an overview of the IBERT core in an ML510 system.

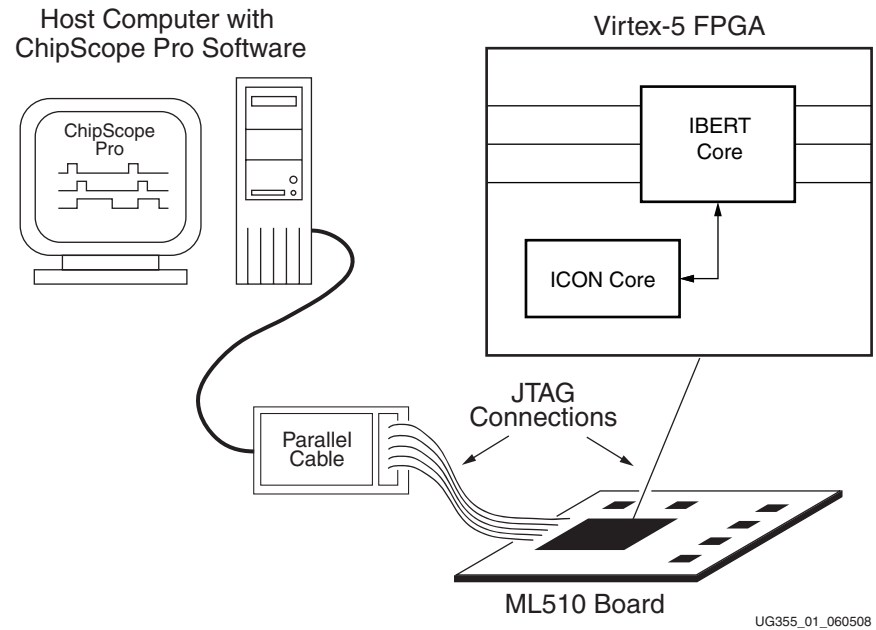


Figure 1: IBERT Core Generated Using ChipScope Pro Software

The IBERT design (ml510\_ibert\_2gtxs\_design.zip) (Figure 2) verifies loopback connections over the following interfaces that use the GTX transceivers:

- SATA
- Ethernet SGMII

Refer to the posted tutorials for a description of equipment and cables available from third-party vendors to test these interfaces.

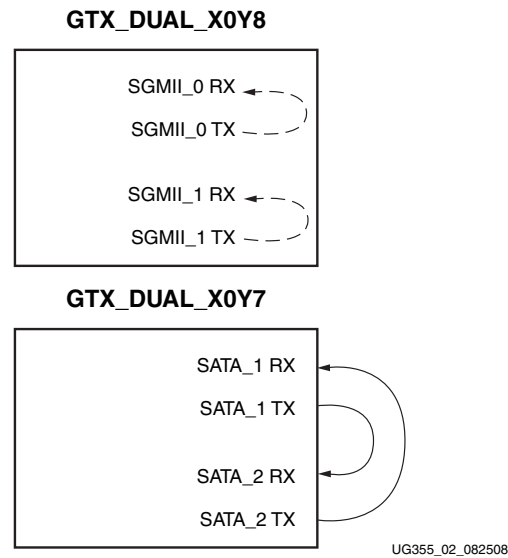


Figure 2: IBERT Design

**Note:** An internal GTX loopback is used with the SGMII interface.

## Memory Interface Generator (MIG) Design

The MIG tool can generate DDR SDRAM, DDR2 SDRAM, and QDR II SRAM interfaces for Virtex-5 FPGAs. The tool takes inputs such as the memory interface type, FPGA family, FPGA devices, frequencies, data width, memory mode register values, and so forth, from the user through a GUI. The tool generates RTL, SDC, UCF, and document files as output. RTL or EDIF (EDIF is created after running a script file, where the script file is a tool output) files can be integrated with other design files.

Refer to the *Xilinx Memory Interface Generator User Guide* [Ref 19] for information on how to download the tool, how to use the tool, and how to implement the memory controllers. The user guide also contains information on recommended pin constraints, PCB trace matching, terminations schemes, clock capable I/O rules, bank recommendations, DCI and ODT suggestions, loopback trace signals, and more. Consult this guide before implementing a PCB with an external memory interface.

The Web page for the ML510 MIG design is located at:

- [www.xilinx.com/products/boards/ml510/reference\\_designs.htm#mig\\_design](http://www.xilinx.com/products/boards/ml510/reference_designs.htm#mig_design)

Figure 3 shows an example view of the MIG user interface. See the “References” section for additional MIG resources.

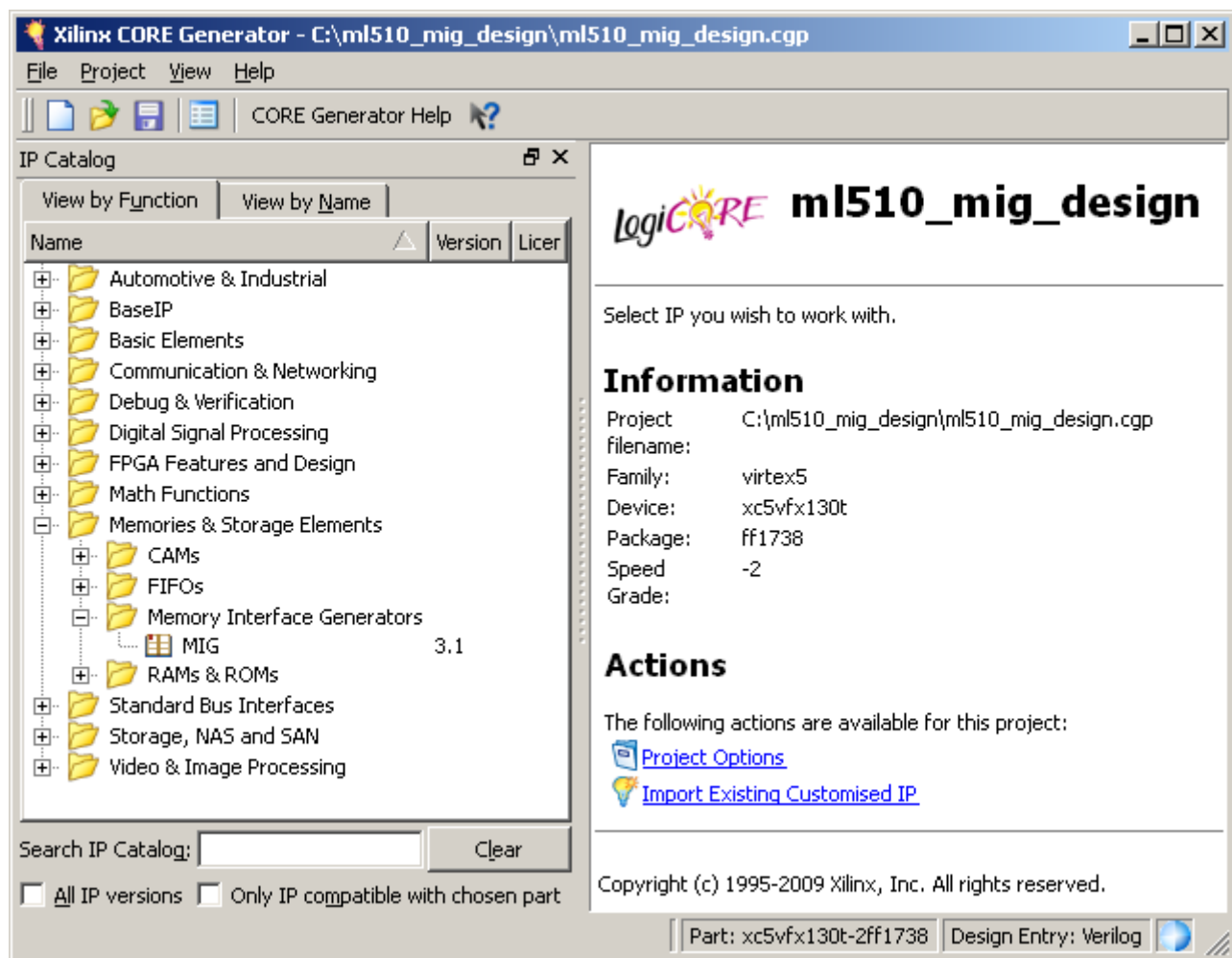


Figure 3: Memory Interface Generator

## System Monitor

Every member of the Virtex-5 FPGA family contains a single System Monitor (Figure 4), which is located in the center of every die. The System Monitor function is built around a 10-bit, 200-kSPS (kilosamples per second) Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the ADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 user-selectable analog inputs, known as auxiliary analog inputs ( $V_{AUXP}[15:0]$ ,  $V_{AUXN}[15:0]$ ). The external analog inputs allow the ADC to monitor the physical environment of the board or enclosure. System Monitor is fully functional on power up, and measurement data can be accessed via the JTAG port pre-configuration.

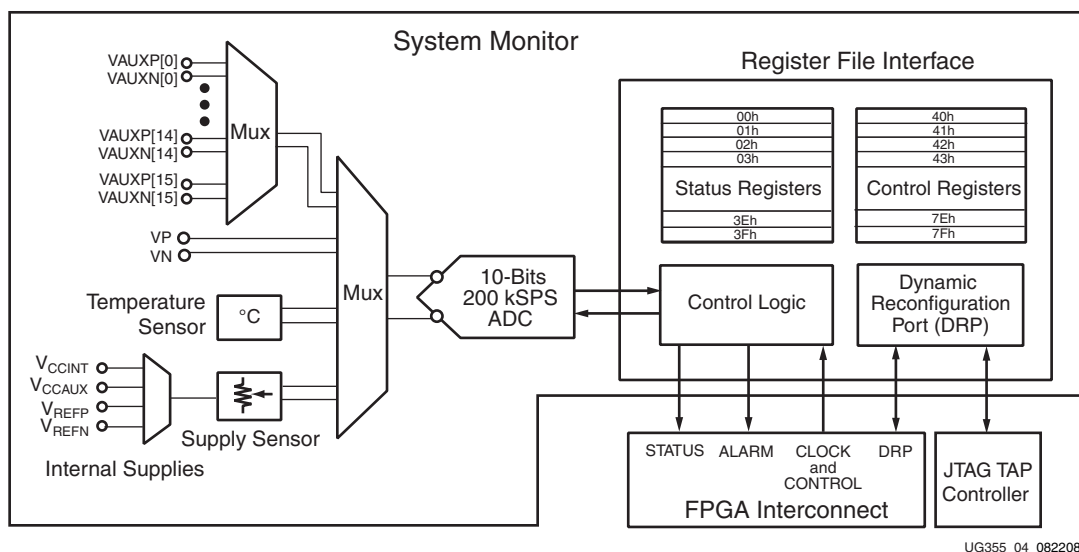


Figure 4: System Monitor Block Diagram

A useful feature of the System Monitor is the ability to access measurement information over a JTAG connection prior to configuring the FPGA. Figure 5 and Figure 6, page 19 show the ChipScope Pro System Monitor console reporting the ML510 temperature and an onboard voltage.

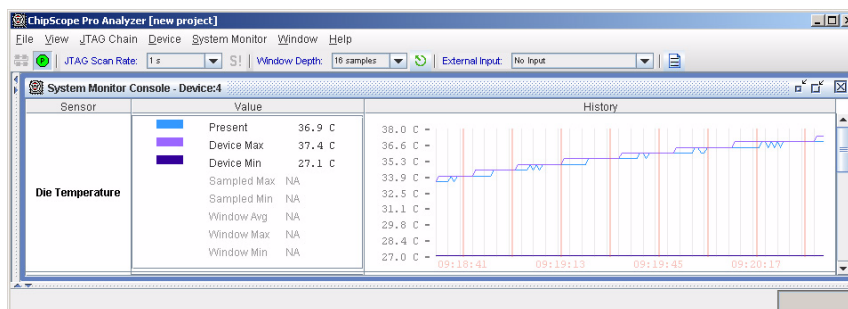


Figure 5: System Monitor Die Temperature Sensor

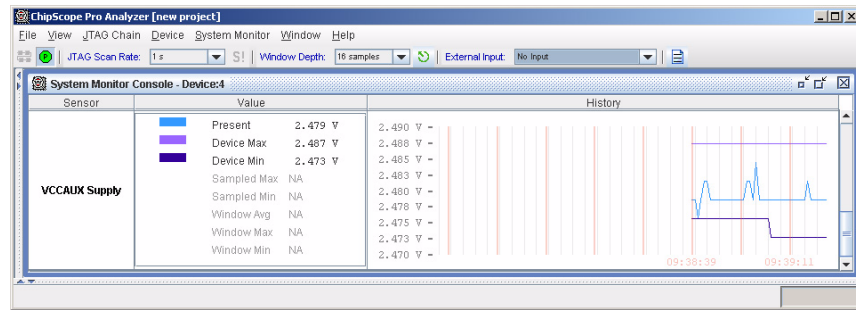


Figure 6: System Monitor VCCAUX Supply Sensor

For more information about the Virtex-5 FPGA System Monitor, see <http://www.xilinx.com/systemmonitor> and [Ref 10] *Virtex-5 FPGA System Monitor User Guide*.

## References

This section provides references to documentation supporting Virtex-5 devices, tools, and IP. For additional information, see [www.xilinx.com/support/documentation/index.htm](http://www.xilinx.com/support/documentation/index.htm).

Documents supporting Virtex-5 FPGAs:

1. [DS100](#), *Virtex-5 FPGA Family Overview*.
2. [DS202](#), *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics*.
3. [UG190](#), *Virtex-5 FPGA User Guide*.
4. [UG200](#), *Embedded Processor Block in Virtex-5 FPGAs Reference Guide*.
5. [UG198](#), *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.
6. [UG194](#), *Virtex-5 FPGA Embedded Tri-Mode Ethernet Media Access Controller User Guide*.
7. [UG197](#), *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide*.
8. [UG193](#), *Virtex-5 FPGA XtremeDSP Design Considerations*.
9. [UG191](#), *Virtex-5 FPGA Configuration User Guide*.
10. [UG192](#), *Virtex-5 FPGA System Monitor User Guide*.
11. [UG195](#), *Virtex-5 FPGA Packaging and Pinout Specification*.

Documents supporting [Xilinx Platform Studio \(XPS\)](#):

12. [UG111](#), *Embedded System Tools Reference Manual*
13. [UG683](#), *EDK Concepts, Tools, and Techniques*.
14. [UG081](#), *MicroBlaze Processor Reference Guide*.
15. [UG643](#), OS and Libraries Document Collection

Documents specific to the ML510 Evaluation Platform:

16. [UG356](#), *ML510 Evaluation Platform User Guide*.

Documents supporting IBERT:

17. [UG029](#), *ChipScope Pro Software and Cores User Guide*.

The Xilinx [Memory Solutions Web page](#) offers the following material supporting the Memory Interface Generator (MIG) tool:

18. [WP260](#), *Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator*.
19. [UG086](#), *Xilinx Memory Interface Generator (MIG) User Guide* (for registered users).
20. [Demos on Demand](#), *Memory Interface Solutions with Xilinx FPGAs*.
21. [Xilinx Support - Memory Interface Resources](#) (for registered users).

Documents supporting the LogiCORE Endpoint block for PCIe solutions:

22. [DS551](#), *LogiCORE Endpoint Block Plus for PCI Express Data Sheet*.
23. [UG341](#), *LogiCORE Endpoint Block Plus for PCI Express User Guide*.
24. [UG343](#), *LogiCORE Endpoint Block Plus for PCI Express Getting Started Guide*.

Documents supporting the LogiCORE SGMII solution:

25. [DS550](#), *Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet*.
26. [UG340](#), *Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide*.

The Xilinx [DSP Resources Web page](#) includes documents supporting the System Generator for DSP:

27. [UG639](#), *System Generator for DSP Getting Started Guide*
28. [UG640](#), *System Generator for DSP User Guide*
29. [UG638](#), *System Generator for DSP Reference Guide*

Documents supporting additional embedded processor and LogiCORE IP cores:

30. [DS537](#), *XPS\_LL\_TEMAC (v2.00a) Data Sheet*.
  - ◆ [XAPP1026](#), *LightWeight IP (lwIP) Application Examples Application Note*.
31. [DS581](#), *XPS External Peripheral Controller (EPC) (v1.01a) Data Sheet*.
  - ◆ [XAPP925](#), *Reference System: Using the OPB EPC with the Cypress CY7C67300 USB Controller Application Note*.
32. [DS531](#), *Processor Local Bus (PLB) v4.6 (v1.00a) Data Sheet*.
33. [DS643](#), *Multi-Port Memory Controller (MPMC) (v4.02a) Data Sheet*.
34. [DS575](#), *XPS Multi-Channel External Memory Controller (XPS MCH EMC) (v3.00a) Data Sheet*.
35. [DS568](#), *XPS\_LL\_FIFO (v1.00a) Data Sheet*.
36. [DS606](#), *XPS IIC Bus Interface (v2.00a) Data Sheet*.
37. [DS583](#), *XPS System ACE Interface Controller (v1.00a) Data Sheet*.
38. [DS573](#), *XPS Timer/Counter (v1.00a) Data Sheet*.
39. [DS572](#), *XPS Interrupt Controller (v2.00a) Data Sheet*.
  - ◆ [XAPP778](#), *Using and Creating Interrupt-Based Systems Application Note*.
40. [DS569](#), *XPS General Purpose Input/Output (GPIO) (v1.00a) Data Sheet*.
41. [DS577](#), *XPS 16550 UART (v1.00a) Data Sheet*.
42. [DS695](#), *XPS Thin Film Transistor (TFT) Controller (v1.00a) Data Sheet*.
43. [DS707](#), *XPS PS2 Controller (v1.01a) Data Sheet*.
44. [DS596](#), *XPS Block RAM (BRAM) Interface Controller (v1.00a) Data Sheet*.
45. [DS403](#), *PLBV46 to OPB Bridge (v1.00a) Data Sheet*.
46. [DS401](#), *On-Chip Peripheral Bus V2.0 with OPB Arbiter (v1.10c) Data Sheet*.
47. [DS444](#), *Block RAM Block (v1.00a) Data Sheet*.
48. [DS641](#), *Microprocessor Debug Module (MDM) (v1.00a) Data Sheet*.
49. [DS445](#), *Local Memory Bus (LMB) v1.0 (v1.00a) Data Sheet*.

50. [DS452](#), *LMB Block RAM Interface Controller (v2.10b) Data Sheet*.
51. [DS298](#), *JTAGPPC Controller (v2.01c) Data Sheet*.
52. [DS406](#), *Processor System Reset Module (v2.00a) Data Sheet*.
53. [DS614](#), *Clock Generator (v2.00a) Data Sheet*.
54. [DS481](#), *Util Vector Logic Data Sheet*.
55. [DS484](#), *Util Bus Split Operation (v1.00a) Data Sheet*.
56. [DS694](#), *Utility IO Multiplexer (v1.00a) Data Sheet*.
57. [DS616](#), *PLBV46 PCI Full Bridge (v1.00a) Data Sheet*.