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Chapter 1

Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit

Introduction

This document describes how to use the materials provided in the VC707 Evaluation Kit to set up the VC707 board and a host computer to run two reference designs, which test and demonstrate some of the key features of the XC7VX485T FPGA and the VC707 board:

- Built-in self test (BIST)
- Analog mixed signal (AMS) card demonstration

Note: These design summaries are for use as a quick start method for users who are familiar with Xilinx tools, technology, and reference designs. Additional instructions and background information are available from the VC707 Evaluation Kit website.

VC707 Evaluation Kit Contents

The VC707 Evaluation Kit includes:

- VC707 board with the Virtex®-7 XC7VX485T FPGA
- ISE® Design Suite: Logic Edition (full seat, node-locked, device-locked to the XC7VX485T FPGA)
- Vivado® Design Suite Installation DVD
- Printed entitlement voucher: provides entitlement of the Vivado Design Suite Logic Edition, node-locked, and device-locked to the XC7VX485T FPGA. Follow the printed instructions on the voucher to redeem your software entitlement.
- AMS101 evaluation card
- USB cable, standard-A plug to mini-B plug
- USB cable, standard-A plug to micro-B plug
- HDMI™ cable, type-A plug to type-A plug
- Power Supply: 100 VAC–240 VAC input, 12 VDC 5.0A output
- Power cords to support three main plug types
- Getting Started Guide
Host Computer Requirements

The example designs described in this document require an Intel processor based computer running Windows 7 or Windows XP operating system. The computer must have two USB ports and an Ethernet interface.

*Note:* The Windows 7 operating system is used in the setup instructions and examples.

Preliminary Setup

Complete the tasks in this section before running the reference designs.

Install ISE Software

Install the latest version of the Xilinx ISE® Design Suite on the host computer.

Install the USB UART Drivers

Download and install the Silicon Laboratories CP210x VCP drivers on the host computer. The drivers are available for download at no cost from Silicon Labs.

Configure the Host Computer COM Port

The BIST design uses a terminal program to communicate between the host computer and the VC707 board. To configure the host computer COM port for this purpose:

1. Connect the VC707 board to the host computer and power supply as shown in Figure 1-1.

2. Turn Board power on (SW12).

![Figure 1-1: Host Computer COM Port Configuration](image)
3. Open the host computer Device Manager (Figure 1-2). In the Windows task bar, Click **Start**, click **Control Panel**, and then click **Device Manager**.

![Device Manager](image1.png)

*Figure 1-2: Device Manager*

4. Open UART properties. Expand **Ports (COM & LPT)**, right-click **Silicon Labs CP210x USB to UART Bridge**, and then click **Properties**.

5. In the properties window, select the **Port Settings** tab, verify the settings match the values shown in Figure 1-3 and then click **Advanced**.

![Port Settings](image2.png)

*Figure 1-3: Port Settings*
6. Select an unused COM Port Number and then click **OK**. Figure 1-4 shows **COM1** as the selected COM port number.

![Select an unused COM port](image)

**Figure 1-4: Advanced Settings**

7. Click **OK** in the properties window (Figure 1-3, page 7), and then close the Device Manager and the Control Panel.

**Install the Terminal Program**

Download and install the Tera Term Pro terminal program on the host computer. Tera Term is available for download at no cost from the LogMeIT download page.

To communicate with the VC707 board, configure the New Connection and Serial Port settings as shown in Figure 1-5. These settings must match the host computer COM port settings shown in Figure 1-3, page 7 and Figure 1-4.

![TeraTerm Pro Settings](image)

**Figure 1-5: TeraTerm Pro Settings**

Preliminary setup is complete and the reference designs can now be run.
Verify Jumpers are in Default Positions

Verify the jumpers on the VC707 board are positioned as shown in Table 1-1. See Figure 1-6 for the location of the jumpers.

### Table 1-1: Default Jumper Settings

<table>
<thead>
<tr>
<th>Callout</th>
<th>Jumper</th>
<th>Function</th>
<th>Default Jumper Position</th>
<th>Schematic 0381418 Page Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>J6</td>
<td>SFP Enable</td>
<td>None</td>
<td>31</td>
</tr>
<tr>
<td>2</td>
<td>J9</td>
<td>XADC GND ferrite filter bypass jumper</td>
<td>None</td>
<td>40</td>
</tr>
<tr>
<td>3</td>
<td>J10</td>
<td>XADC GND-to-XADC_AGND jumper</td>
<td>1–2</td>
<td>40</td>
</tr>
<tr>
<td>4</td>
<td>J11</td>
<td>TI Controller U42 Addr 52 Reset jumper</td>
<td>None</td>
<td>46</td>
</tr>
<tr>
<td>5</td>
<td>J12</td>
<td>TI Controller U43 Addr 53 Reset jumper</td>
<td>None</td>
<td>50</td>
</tr>
<tr>
<td>6</td>
<td>J13</td>
<td>USB Mini-B Connector J2 VBUS</td>
<td>None</td>
<td>44</td>
</tr>
<tr>
<td>7</td>
<td>J14</td>
<td>USB SMBC U8 CLKOUT selector</td>
<td>None</td>
<td>44</td>
</tr>
<tr>
<td>8</td>
<td>J38</td>
<td>SFP RX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate</td>
<td>1–2</td>
<td>31</td>
</tr>
<tr>
<td>9</td>
<td>J39</td>
<td>SFP TX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate</td>
<td>1–2</td>
<td>31</td>
</tr>
<tr>
<td>10</td>
<td>J42</td>
<td>XADC external 1.2V or internal VREFP selector</td>
<td>1–2</td>
<td>40</td>
</tr>
<tr>
<td>11</td>
<td>J43</td>
<td>XADC VCC Select Header</td>
<td>2–3</td>
<td>40</td>
</tr>
<tr>
<td>12</td>
<td>J44</td>
<td>USB Mini-B Connector J2 GND jumper</td>
<td>None</td>
<td>44</td>
</tr>
<tr>
<td>13</td>
<td>J45</td>
<td>USB SMBC U8 VBUS</td>
<td>1–2</td>
<td>44</td>
</tr>
<tr>
<td>14</td>
<td>J49</td>
<td>PCIe Bus Width Select Header</td>
<td>1-2</td>
<td>30</td>
</tr>
<tr>
<td>15</td>
<td>J50</td>
<td>TI Controller U64 Addr 54 Reset jumper</td>
<td>None</td>
<td>53</td>
</tr>
<tr>
<td>16</td>
<td>J51</td>
<td>FMC_VADJ_ON_B jumper</td>
<td>1–2</td>
<td>46</td>
</tr>
<tr>
<td>17</td>
<td>J53</td>
<td>XADC VCC5V0-to-XADC_VCC5V0 jumper</td>
<td>1–2</td>
<td>40</td>
</tr>
<tr>
<td>18</td>
<td>J54</td>
<td>XADC REF3012 U35 V_IN Select</td>
<td>1–2</td>
<td>40</td>
</tr>
</tbody>
</table>
Built-In Self Test

The BIST tests several XC7VX485T FPGA and VC707 board features. The BIST interface is a menu of tests displayed by a terminal program running on the host computer.

Project Files

The BIST design is available for download from the VC707 Evaluation Kit website on the Docs & Designs tab.

The BIST is pre-loaded in the device and the project files are not required to run this demonstration.
Run BIST

2. Connect the VC707 board to the host computer and power supply as shown in Figure 1-7.
3. Turn board power on (SW12).
4. Set DIP switch SW11 as shown in Figure 1-8.

Figure 1-7: BIST Board Connections

Figure 1-8: SW11 BIST Settings
5. Press and release the Program button SW9 (Figure 1-7). The BIST bitstream configures the FPGA and then runs BIST. The terminal program displays the BIST menu shown in Figure 1-9.

![BIST Menu](UG848_c1_08_062112)

**Figure 1-9: BIST Menu**

6. To run a test, type the test number, and press the Enter key. Press any key to end the test and return to the menu.

### AMS 101 Card Demonstration

The XC7VX485T FPGA features dual one Mega-sample per second (MS/s), 12-bit, analog-to-digital converters (XADC) built into the FPGA. The AMS card demonstration uses the AMS 101 card (Figure 1-11, page 14) to generate an analog signal and the AMS evaluator tool (Figure 1-13, page 15) to view and control the signal.

### Install the AMS Evaluator Tool

Download the AMS Evaluator installer files:

1. Go to [AMS101 Evaluation Card](#).
2. Click [AMS101 Evaluation Card Targeted Reference Designs](#).
4. Extract the AMS101 AMS Evaluator Installer Vxx to your hard drive.
5. Click the setup.exe file to install the National Instruments LabVIEW Engine needed to host the AMS Evaluator tool.

The GUI was developed with National Instruments LabVIEW 2011 software. To enable use of the GUI without a LabVIEW license, Xilinx bundled the LabVIEW run-time engine with the GUI installer. During the installation process, the run-time engine is installed on the PC.
Extract the AMS Design Files

1. Go to the VC707 Evaluation Kit website and navigate to the Docs & Designs tab.
2. Click Virtex-7 FPGA VC707 Evaluation Kit.
3. Navigate to the software version that you are using, click + to expand the document type list, and click Targeted Reference Designs.
5. After downloading the design files, open the xadc_eval_design_vc707_vxx folder and unzip the files to a working directory on the host computer.
6. Open the ChipScope™ Pro Analyzer in the ISE design tools.
7. Click Open_cable.
8. Select Device, choose Configure, and click Select New File.
9. Open the AMS design in the xadc_eval_design_vc707_vxx folder by opening the ready_to_test folder and selecting the xadc_eval_design.bit file.

Set Up the Hardware

2. On the AMS101 card (Figure 1-11), place jumpers across pins 1-2 on J3 and J5.

![Figure 1-10: AMS101 Evaluation Card](image-url)
3. Turn off the VC707 board power (SW12) before installing the AMS 101 card on the VC707 board XADC header J35.

4. Plug the AMS 101 Card into the XADC header J35 on the VC707 board as shown in Figure 1-11.

5. Connect the VC707 board to the host computer and power supply as shown in Figure 1-11.

6. Turn board power on (SW12).

Examine Analog Mixed Signal Features

The AMS evaluator tool (Figure 1-13) is useful for examining analog signals in the time and frequency domains, displaying linearity, viewing the XADC register settings, and monitoring the internal FPGA temperature sensor and supply voltages. The AMS evaluator tool also provides user-controllable decimation on the XADC output data to enhance the signal-to-noise ratio (SNR) performance.

Table 1-2: AMS101 Evaluation Card Jumper and Component Notes

<table>
<thead>
<tr>
<th>Callout</th>
<th>Reference Designator</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>J2</td>
<td>External signal source input to $V_P$ positive analog input.</td>
</tr>
<tr>
<td>2</td>
<td>J3</td>
<td>Jumper on pins 1–2 selects DAC signal source. Jumper on pins 2–3 selects external input source on J2.</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>20-pin connector to XADC header J35 on the VC707 board.</td>
</tr>
<tr>
<td>5</td>
<td>J6</td>
<td>External signal source to $V_N$ negative analog input.</td>
</tr>
<tr>
<td>6</td>
<td>U3</td>
<td>16-bit DAC. Sets analog test voltage.</td>
</tr>
<tr>
<td>7</td>
<td>U2</td>
<td>Reference buffer for DAC.</td>
</tr>
</tbody>
</table>
After the AMS Evaluator installer files are installed, a red Xilinx logo (“X”) is displayed on the host PC desktop. Click the “X” to open the AMS Evaluator tool (Figure 1-12).

Figure 1-12: AMS Icon

To run the AMS evaluator tool executable file:

1. Open the AMS_Eval_Demo_Files_<ISE_Version> directory and double-click AMS101 Evaluator GUI V1.0.exe. See Figure 1-13.

Figure 1-13: AMS101 Evaluator Tool

For an extensive explanation of the AMS101 evaluation card see the AMS101 Evaluation Card User Guide (UG886) [Ref 1].
Next Steps

1. Download the VC707 Evaluation Board for the Virtex-7 FPGA User Guide (UG885) [Ref 2].
2. Review and run the reference designs available at the VC707 Evaluation Kit website from the Docs & Designs tab.

Additional Information

VC707 board reference design files, user guides, schematics, and bill of materials, can be downloaded from the VC707 Evaluation Kit website.

Other documents associated with Xilinx devices, design tools, intellectual property, boards, and kits are available at the Xilinx documentation website.

Instructions for restoring the BPI flash memory with the factory-loaded reference designs are provided in VC707 Restoring Flash Contents (XTP145) [Ref 3].

For an extensive explanation of the AMS101 evaluation card, see the AMS101 Evaluation Card User Guide (UG886) [Ref 1].
Appendix A

VC707 Board Components

The VC707 board block diagram is shown in Figure A-1. The VC707 board schematics are available for download from the VC707 Evaluation Kit product page on the Docs & Designs tab at the VC707 Evaluation Kit website.

Caution! The VC707 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Figure A-1: VC707 Board Block Diagram
Appendix A: VC707 Board Components

Feature Descriptions

Figure A-2 shows the VC707 board.

Note: The image in Figure A-2 is for reference only and might not reflect the current revision of the board.

Table A-1: VC707 Board Component Descriptions

<table>
<thead>
<tr>
<th>Callout</th>
<th>Reference Designator</th>
<th>Component Description</th>
<th>Notes</th>
<th>Schematic Page Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1</td>
<td>Virtex-7 FPGA with cooling fan</td>
<td>XC7VX485T-2FFG1761C</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>J1</td>
<td>DDR3 SODIMM memory (1 GB)</td>
<td>Micron MT8JTF12864HZ-1G6G1</td>
<td>21</td>
</tr>
<tr>
<td>3</td>
<td>U3</td>
<td>BPI parallel NOR flash memory (1 Gb)</td>
<td>Micron PC28F00AG18FE</td>
<td>35</td>
</tr>
<tr>
<td>4</td>
<td>U8, J2</td>
<td>USB ULPI transceiver, USB mini-B connector</td>
<td>SMSC USB3320-EZK</td>
<td>44</td>
</tr>
<tr>
<td>5</td>
<td>U29</td>
<td>SD card interface connector</td>
<td>Molex 67840-8001</td>
<td>37</td>
</tr>
<tr>
<td>6</td>
<td>U26</td>
<td>USB JTAG interface, USB micro-B connector</td>
<td>Digilent USB JTAG module</td>
<td>20</td>
</tr>
<tr>
<td>7</td>
<td>U51</td>
<td>System clock, 200 MHz, LVDS (back side of board)</td>
<td>SiTime SIT9102-243N25E200.0000</td>
<td>32</td>
</tr>
<tr>
<td>8</td>
<td>U34</td>
<td>I²C programmable user clock LVDS, 156.250 MHz default frequency (back side of board)</td>
<td>Silicon Labs SI570BAB0000544DG</td>
<td>32</td>
</tr>
<tr>
<td>9</td>
<td>J31, J32</td>
<td>User SMA clock</td>
<td>Rosenberger 32K10K-400L5</td>
<td>32</td>
</tr>
<tr>
<td>10</td>
<td>J25, J26</td>
<td>GTX transceiver SMA reference clock</td>
<td>Rosenberger 32K10K-400L5</td>
<td>32</td>
</tr>
</tbody>
</table>
### Table A-1: VC707 Board Component Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Callout</th>
<th>Reference Designator</th>
<th>Component Description</th>
<th>Notes</th>
<th>Schematic Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>U24</td>
<td>Jitter attenuated clock (back side of board)</td>
<td>Silicon Labs SI5324C-C-GM</td>
<td>33</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>GTX transceiver Quad 111 – Quad 119</td>
<td>Embedded within FPGA U1</td>
<td>12 – 15</td>
</tr>
<tr>
<td>13</td>
<td>P1</td>
<td>PCI Express connector</td>
<td>8-lane card edge connector</td>
<td>30</td>
</tr>
<tr>
<td>14</td>
<td>P3</td>
<td>SFP/SFP+ module connector</td>
<td>Molex 74441-0010</td>
<td>31</td>
</tr>
<tr>
<td>15</td>
<td>U50</td>
<td>10/100/1000 Mb/s Ethernet PHY</td>
<td>Marvell M88E1111-BAB1C000</td>
<td>34</td>
</tr>
<tr>
<td>16</td>
<td>U2</td>
<td>SGMII GTX transceiver clock generator</td>
<td>ICS ICS84402IACI-01LF</td>
<td>32</td>
</tr>
<tr>
<td>17</td>
<td>U44</td>
<td>USB-to-UART bridge</td>
<td>Silicon Labs CP2103GM</td>
<td>36</td>
</tr>
<tr>
<td>18</td>
<td>P2, U48</td>
<td>HDMI video connector, HDMI controller</td>
<td>Molex 500254-1927, AD ADV7511KSTZ-P</td>
<td>43, 42</td>
</tr>
<tr>
<td>19</td>
<td>J23</td>
<td>LCD character display and connector</td>
<td>2 x 7 0.1 inch male header</td>
<td>39</td>
</tr>
<tr>
<td>20</td>
<td>U52</td>
<td>I²C Bus Switch (back side of board)</td>
<td>TI PCA9548ARGгер</td>
<td>41</td>
</tr>
<tr>
<td>21</td>
<td>DS11–DS13</td>
<td>Ethernet status LEDs</td>
<td>EPHY status LED, dual green</td>
<td>34</td>
</tr>
<tr>
<td>22</td>
<td>DS2–DS9</td>
<td>User LEDs</td>
<td>GPIO LEDs, green 0603</td>
<td>38</td>
</tr>
<tr>
<td>23</td>
<td>SW3–SW7</td>
<td>User pushbuttons, active-High</td>
<td>E-Switch TL3301EP100QG</td>
<td>38</td>
</tr>
<tr>
<td>24</td>
<td>SW2</td>
<td>User DIP Switch</td>
<td>8-pole C and K SDA08H15BD</td>
<td>38</td>
</tr>
<tr>
<td>25</td>
<td>SW10</td>
<td>User rotary switch (under LCD assembly)</td>
<td>Panasonic EVQ-WK4001</td>
<td>38</td>
</tr>
<tr>
<td>26</td>
<td>J33, J34</td>
<td>User SMA GPIO</td>
<td>Rosenberger 32K10K-400L5</td>
<td>32</td>
</tr>
<tr>
<td>27</td>
<td>SW12</td>
<td>Power on/off switch</td>
<td>C&amp;K 1201M253AQE2</td>
<td>45</td>
</tr>
<tr>
<td>28</td>
<td>SW9</td>
<td>FPGA PROG pushbutton</td>
<td>E-Switch TL3301EP100QG</td>
<td>38</td>
</tr>
<tr>
<td>29</td>
<td>SW11</td>
<td>Config mode/upper linear flash address dip switch</td>
<td>5-pole C&amp;K SDA05H11BD</td>
<td>36</td>
</tr>
<tr>
<td>30</td>
<td>J35</td>
<td>FMC HPC1 connector (J35)</td>
<td>Samtec ASP_134486_01</td>
<td>22–25</td>
</tr>
<tr>
<td>31</td>
<td>J37</td>
<td>FMC HPC2 connector (J37)</td>
<td>Samtec ASP_134486_01</td>
<td>26–29</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td>Power management system (front and back side of board)</td>
<td>TI UCD9248PFC in conjunction with various regulators</td>
<td>45–55</td>
</tr>
<tr>
<td>33</td>
<td>J19</td>
<td>Xilinx XADC header</td>
<td>2 x 10 0.1inch male header</td>
<td>40</td>
</tr>
<tr>
<td>34</td>
<td>J27, J28</td>
<td>GTX receiver SMA (RX)</td>
<td>Rosenberger 32K10K-400L5</td>
<td>32</td>
</tr>
<tr>
<td>35</td>
<td>J29/J30</td>
<td>GTX transmitter SMA (TX)</td>
<td>Rosenberger 32K10K-400L5</td>
<td>32</td>
</tr>
<tr>
<td>36</td>
<td>J5</td>
<td>2 x 5 shrouded PMBus connector</td>
<td>Assmann HW10G-0202</td>
<td>46</td>
</tr>
<tr>
<td>37</td>
<td>J18</td>
<td>12V power input 2 x 3 connector</td>
<td>Molex 39-30-1060</td>
<td>46</td>
</tr>
</tbody>
</table>
Appendix B

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC707 board and its documentation is available on these websites:

- Virtex-7 VC707 Evaluation Kit
- Virtex-7 VC707 Evaluation Kit documentation
- Virtex-7 VC707 Evaluation Kit Master Answer Record (AR 45382)

These documents and sites provide supplemental material useful with this guide:

1. AMS101 Evaluation Card User Guide (UG886)
2. VC707 Evaluation Board for the Virtex-7 FPGA User Guide (UG885)
3. VC707 Restoring Flash Contents (XTP145)
4. Silicon Labs
5. LogMeTT
Appendix C

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx (“Development Systems”). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:

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