Virtex-7 XT VC709 Connectivity Kit (Vivado Design Suite 2013.2) Getting Started Guide

UG966 (v2.0) July 29, 2013
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Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
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<tr>
<td>02/08/13</td>
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<td>Changed XPN number on title page to 0402950-01.</td>
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<tr>
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<td>1.1</td>
<td>Revised DDR3 description in the first paragraph of the Introduction, page 13. Revised DDR3 transfer rate on page 13. Added ISE design suite to list on page 14. Added step 6 through step 9 on page 17. Updated screen captures in Figure 2-12, Figure 2-15, and Figure 2-19. Updated links in Further Resources, page 35.</td>
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<td>2.0</td>
<td>Revised all references to the FPGA part number from commercial engineering sample (CES) to commercial (C). Replaced direct links in the text with indirect links referenced in Appendix A. Revised the list under Requirements, page 14 to indicate a board programmed with the BIST and TRD is required. Added note on page 14 referring to UG962 for programming instructions. Removed programming instructions from VC709 Board Setup, page 15. Added ZIP file download instructions under Driver Installation and Modes of Operation, page 18.</td>
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Introduction

Overview

The VC709 evaluation kit is based on the XC7VX690T-2FFG1761C FPGA. For additional information, see the Virtex®-7 family FPGA Product Table [Ref 7]. A built-in self-test (BIST) and a Connectivity Targeted Reference Design (TRD) are provided with the VC709 evaluation kit. The BIST provides a convenient way to test many of the features of the board on power-up and upon reconfiguration. This guide describes how to run the BIST and the Connectivity TRD. For more designs targeting the VC709 board, and the most up to date information on the tutorial or documentation, visit the VC709 product page [Ref 8].

Figure 1-1 is a photograph of the VC709 evaluation kit.

VC709 Evaluation Kit Contents

The VC709 evaluation kit includes:

- VC709 evaluation board featuring the XC7VX690T-2FFG1761C FPGA with cooling fan
- Vivado™ Design Suite DVD and License Voucher
- Device-locked to the Virtex-7 690T FPGA
Virtex-7 FPGA Base Platform Built-In Self-Test

The built-in self-test (BIST) of the Virtex-7 FPGA tests many of the features offered by the Virtex-7 FPGA VC709 evaluation kit. The test is an available reference design for the VC709 evaluation kit and can be programmed into the FPGA by way of JTAG.

Figure 1-2 provides an overview of the board features utilized by the BIST.

Note: For a diagram of all the features on the VC709, see the VC709 Evaluation Board for the Virtex-7 FPGA User Guide (UG887).
Prerequisites

The prerequisites include:

- VC709 evaluation board with Virtex-7 FPGA
- USB-to-Mini-B cable (for UART)
- USB-to-Micro-B cable (for JTAG)
- 12V AC power adapter
- Tera Term Pro (terminal emulation program)
- Silicon Labs USB-UART driver
- A PC and display monitor (not included with kit)

Hardware Setup

This section details the hardware setup and use of the terminal program for running the BIST application. Also included are step-by-step instructions for board bring-up.

VC709 Board Setup

Set the SW1 switch as shown in Figure 1-3 to set up the VC709 evaluation board.

![SW1 Switch Settings for JTAG Programming Mode](UG966_c1_03_122112)

**Figure 1-3: SW1 Switch Settings for JTAG Programming Mode**

*Note:* For this application, set the board up as a standalone system powered with the AC power adapter provided with the VC709 evaluation kit.

Hardware Bring-Up

**Figure 1-2** is a photograph of the setup for the VC709 board.

To prepare the VC709 board for hardware bring-up:

1. With the VC709 board switched off, connect a USB-to-Mini-B cable to the UART port of the VC709 board and to the host PC (USB-UART in Figure 1-2).
2. Connect the 12V_AC adapter cable to the VC709 board (12V Power in Figure 1-2).
3. Connect the Digilent JTAG cable to the VC709 board (USB-JTAG in Figure 1-2).
4. Switch on the power to the VC709 board.

Install Silicon Labs UART Device Driver

The UART device driver is required for UART-USB communications with the host computer.

*Note:* The steps described here refer to a host PC running Windows XP or Windows 7.
To install the UART device driver and set the COM port:

1. Download and run the executable file for the Silicon Labs UART-USB driver [Ref 9]. Figure 1-4 shows the Silicon Labs InstallShield Wizard.

2. On the host PC, right-click on My Computer and select Properties.

3. Click on the Hardware tab.

4. Click the Device Manager button.

5. Locate the Silicon Labs device, right-click on it and select Properties (see Figure 1-5).
Prerequisites

6. Click on the Port Settings tab.
7. Click the Advanced button.
8. Select an open COM port between COM1 and COM4.
9. Click OK.

Run the BIST Application

To run the BIST application:

1. Download the VC709 BIST PDF file and VC709 BIST design files (RDF0230) from the VC709 product page [Ref 8].
2. Unzip the design files to the C:\ directory.
3. Start the installed terminal program.
4. Under Setup > Serial Port . . . ensure that the settings match Figure 1-6:
   - Port: COM2 (the COM port set in the Install Silicon Labs UART Device Driver, page 7 section)
   - Baud Rate: 9600
   - Data: 8-bit
   - Parity: none
   - Stop: 1-bit
   - Flow control: None

   Figure 1-6 shows the serial port setup window.

   ![Image of Serial Port Setup Window]

5. Open an ISE® Design Suite command prompt and enter:

   ```
cd C:\vc709_bist\ready_for_download
vc709_bist.bat
```
6. Select the desired tests to run (see Figure 1-7) and observe the results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard non-volatile storage, see the VC709 product page [Ref 8].
Chapter 2

Connectivity System Setup with Targeted Reference Design

Introduction

The Virtex®-7 XT Targeted Reference Design (TRD) targets a VC709 evaluation board containing a Xilinx XC7VX690T-2FFG1761C device (see Figure 2-1). The intent of this design is to demonstrate a high performance data transfer system using x8 PCIe Gen3 endpoint with a high performance scatter gather DMA. Two DDR3 SODIMM memories are used as a packet buffer. Data is transferred over Quad 10G BASE-R links.

The TRD demonstrates high speed data transfers between the host system memory and the FPGA card. The software driver (the data source) generates packets in the user space for performance demo and also connects to the TCP/IP stack for networking application demo.

Features of the TRD include:

- PCIe Gen3 Endpoint operating at 8 Gb/s, per lane, per direction
  - PCIe transaction interface utilization engine
  - MSI and Legacy interrupt support
- Bus mastering Scatter-gather DMA
  - Multi-channel DMA
  - AXI4 streaming interface for data
  - AXI4 interface for register space access
  - DMA performance engine
  - Full duplex operation
  - Independent transmit and receive channels
- Two DDR3 SODIMMs each operating 64-bits at 1,866 MT/s
  - Use of AXI stream interconnect and AXI Virtual FIFO controller IP to make DDR3 a packet FIFO
- 10 Gigabit Ethernet MAC with 10GBASE-R PHY
  - Address filtering
  - Inter-frame gap control
  - Jumbo frame support up to 16,383 bytes
  - Ethernet statistics engine
  - Management interface for physical interface configuration (MDIO)
Chapter 2: Connectivity System Setup with Targeted Reference Design

- PicoBlaze™ processor-based PVT monitoring
- Engine in hardware to monitor power consumption by reading the TI UCD9248 Power controller devices on the VC709 board
- Engine in hardware to monitor die temperature and voltage rails using Xilinx Analog-to-Digital Converter (XADC)

PicoBlaze processor-based I2C programming of SI5324 clock multiplier or a jitter attenuator device on the VC709 board

Requirements

The VC709 evaluation kit for TRD testing requires the user to provide a host PC with PCIe v3.0 slot and a monitor connected.

Requirements for testing the design in hardware include:

- VC709 evaluation board with XC7VX690T-2FFG1761C FPGA programmed with the XT Connectivity TRD.

**Note:** The VC709 evaluation board is delivered pre-programmed with the XT Connectivity TRD and a BIST. Programming instructions for the XT Connectivity TRD are provided in *Virtex-7 FPGA XT Connectivity Targeted Reference Design for the VC709 Board User Guide* (UG962).

- Vivado® Design Suite: Design Edition
- ISE® Lab tools (or a full installation of ISE Design Suite)

*Figure 2-1: Virtex-7 XT TRD Block Diagram*
**Note:** ISE software version 14.6 or later is specifically required to program the flash memory on the VC709 board.

- USB cable, standard-A plug to micro-B plug
- Four Avago SFP+ connector modules with two fiber optic cables
- ATX power supply adapter cable (4-pin to 6-pin adapter)
- Fedora 16 LiveDVD
- USB Memory device for transferring TRD drivers and GUI files to PCIe host PC (not included in kit)

**Note:** Due to the presence of four SFP+ cages on the side of VC709 evaluation board, a full-sized chassis is needed to test the TRD in its entirety because a rack-sized chassis makes two of the four SFP+ cages inaccessible.

For a list of all known issues, refer to the Virtex-7 XT Connectivity TRD release notes and the known issues master answer record [Ref 10]. The same information is available in the readme.txt file included with the design files.

**Hardware Test Setup**

This section describes hardware bring-up, software bring-up, and use of the application GUI.

All procedures listed in the following sections require Linux super user permissions for access. When using Fedora 16 LiveDVD provided with the kit, super user access is granted by default due to the way the kernel image is built. If not using LiveCD, contact your system administrator for super user access.

**VC709 Board Setup**

To set up the VC709 evaluation board:

1. With the host PC powered off, insert the VC709 board into the PCIe slot.
2. Insert SFP+ connectors into the SFP+ cage positions as shown in Figure 2-2.

**Note:** The cage connector P2 is connected to P3 and P4 to P5 (cage P2 is the bottom one nearer to PCIe finger) to provide loopback capability. The photos in Figure 2-2 show the board outside of the PC chassis for clarity.
Chapter 2: Connectivity System Setup with Targeted Reference Design

The setup with fiber optic cables installed in the PC chassis is as shown in Figure 2-3.

**Figure 2-2: SFP+ Connector Positions on VC709 Board (Left) and Cables Showing Loopback Configuration (Right)**

The setup with fiber optic cables installed in the PC chassis is as shown in Figure 2-3.

**Figure 2-3: Fiber Optic Cable Setup**

3. Connect the 6-pin side of the 12V ATX power supply adapter cable to the board at connector J18, and the 4-pin side of the adapter cable to the ATX power supply.
Note: Because the 4-pin ATX supply cannot be connected directly to the VC709 board, the ATX power supply adapter cable is needed (see Figure 2-4).

Figure 2-4: ATX Power Supply Adapter Cable

4. Ensure that the connections are secure.
5. On SW11, set the mode pins and the BPI upper address pins to configure the FPGA (see the settings in Figure 2-5). A25 and A24 are set to 00 and the mode pins are set to 010.

Figure 2-5: SW11 Switch Settings for Mode Pins and BPI Upper Addresses

6. Power on the system.

The LED indicators on the VC709 board provide the indications listed in Table 2-1. LED positions are marked on the board starting from 7 on the left to 0 on the right.

Table 2-1: LED Indicators on VC709 Evaluation Board

<table>
<thead>
<tr>
<th>LED</th>
<th>Description</th>
<th>Proper Behavior</th>
<th>If Something Wrong</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PCIe link up</td>
<td>On (after a few seconds)</td>
<td>Off after BIOS loads (no link)</td>
</tr>
<tr>
<td>1</td>
<td>PCIe 250 MHz clock heart beat</td>
<td>Blinks slowly</td>
<td>Off (no clock)</td>
</tr>
<tr>
<td>2</td>
<td>PCIe linked at x8</td>
<td>On</td>
<td>Blinking fast (not x8)</td>
</tr>
<tr>
<td>3</td>
<td>PCIe linked at Gen3</td>
<td>On</td>
<td>Blinking fast (not Gen3)</td>
</tr>
<tr>
<td>4</td>
<td>Ethernet 156.25 clock heart beats</td>
<td>Blinks slowly</td>
<td>Off (no clock)</td>
</tr>
<tr>
<td>5</td>
<td>10GBASE-R links ready (for all four links)</td>
<td>On</td>
<td>Off (one or more links down)</td>
</tr>
<tr>
<td>6</td>
<td>DDR3 calibration done (both SODIMMs)</td>
<td>On</td>
<td>Off (calibration failed on at least one SODIMM)</td>
</tr>
<tr>
<td>7</td>
<td>unused</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LED positions are shown in Figure 2-6. If the LEDs are not exhibiting the proper behavior, refer to the Virtex-7 XT Connectivity TRD release notes and known issues master answer record (www.xilinx.com/support/answers/51901.htm).
Chapter 2: Connectivity System Setup with Targeted Reference Design

Chapter 2: Connectivity System Setup with Targeted Reference Design

Driver Installation and Modes of Operation

The following steps describe the installation of the device drivers for the Virtex-7 XT Connectivity TRD after hardware set up. The steps that follow demonstrate all modes of test operation by installing and uninstalling various drivers.

Note: If Fedora 16 is currently installed on the hard disk of the host PC, reboot the PC as a user with root privileges. After reboot, proceed to step 2.

1. Place the Fedora 16 LiveDVD in the CD-ROM drive of the host PC. The PC should boot automatically from the CD-ROM drive.

The Fedora 16 LiveDVD Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. The PC boots from the CD-ROM drive and logs into a live user account. This account has kernel development root privileges required to install and remove device driver modules.

Note: Users might have to adjust BIOS boot order settings to ensure that the CD-ROM drive is the first drive in the boot order. To enter the BIOS menu to set the boot order, press the Delete or F2 key when the system is powered on. Set the boot order and save the changes.

The screen images shown in Figure 2-7 are displayed on the monitor during boot-up.
2. Browse to the Virtex-7 FPGA VC709 Connectivity Kit webpage.

3. Under the Documentation heading, expand by clicking Virtex-7 FPGA VC709 Connectivity Kit - (<Software Version>) where Software Version equals the appropriate design suite software version.


5. Click Virtex-7 FPGA VC709 Connectivity Kit Targeted Reference Design and save vc709-connectivity-trd-rdf0285.zip to a working directory on the host computer.

6. Use a USB Flash memory to copy v7_xt_conn_trd.tar.gz from the vc709-connectivity-trd-rdf0285.zip to the Home directory on the host computer (Figure 2-8).

Figure 2-7: Screen Images of Fedora 16 LiveDVD Boot Sequence

First Screen

Last Boot Screen

Booted

X-Ref Target - Figure 2-7

Figure 2-7: Screen Images of Fedora 16 LiveDVD Boot Sequence
7. Right click v7_xt_conn_trd.tar.gz and select Extract Here. Double-click the v7_xt_conn_trd folder. Figure 2-9 shows the contents of the v7_xt_conn_trd folder.
8. Double-click the quickstart.sh file. This script sets the proper permissions and a pop-up window is displayed to control the running of the script (see Figure 2-10).

![Figure 2-9: Contents of v7_xt_conn_trd Folder](image)

8*BFBB

**Figure 2-9:** Contents of v7_xt_conn_trd Folder

9. Click **Run in Terminal**. The TRD Setup window is displayed as shown in Figure 2-11.

![Figure 2-10: Running QuickStart Script](image)

**Figure 2-10:** Running QuickStart Script

9. **Run in Terminal**. The TRD Setup window is displayed as shown in Figure 2-11.
As described in the following sections, this window is used to install the drivers for testing the different modes of operation. Hovering the mouse pointer over the choices brings up a short description. The available tests are:

- **GEN/CHK**—Selects PCIe-DMA driver with Generator and Checker in hardware or Loopback for maximum PCIe-DMA performance
- **Raw Ethernet**—Selects the Raw Ethernet drivers exercising the Quad 10G links in hardware for maximum Ethernet performance
- **Application**—Selects the Application mode drivers that connect to the networking (TCP/IP) stack for demonstrating a real networking application.

These modes are further explained in the following sections.

**GEN/CHK Performance Mode**

With the TRD Setup window displayed:

1. In the Driver Mode Selection area select **GEN/CHK** (Figure 2-11).
2. Click the **Install** button.

After installation of the GEN/CHK performance mode driver is complete, the Virtex-7 XT Connectivity TRD Control and Monitoring Interface is displayed (Figure 2-12). This interface includes control parameters such as test mode (loopback, generator, or checker) and packet length. The **System Monitor** tab displays system power consumption and die temperature.
**Hardware Test Setup**

**3.** In the Data Path-0 field, with **Loopback** selected by default, click **Start**.

The Virtex-7 XT Connectivity TRD Control and Monitoring Interface is updated.

**4.** Click the **Performance Plots** tab.

The **Performance Plots** tab (Figure 2-13) shows the system-to-card and card-to-system performance numbers for a specific packet size. The user can vary packet size and view performance variations accordingly.

**Figure 2-12:** GEN/CHK Performance Mode

**Note:** This interface also provides LED indicators for DDR3 memory calibration and 10G PHY link status.

**Note:** Only Data Path-0 is enabled in Performance mode GEN/CHK flow.
5. Stop the Gen/Chk test by clicking Stop for Data Path 0.

6. Click the Block Diagram tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode. See Figure 2-14.

Figure 2-13: GEN/CHK Performance Mode Plots
7. Close the Virtex-7 XT Connectivity TRD Control and Monitoring Interface by clicking X in the upper right corner. Closing the interface stops any running test, uninstalls the driver, and returns to the TRD Setup window.

Raw Ethernet Performance Mode

With the TRD Setup window displayed:

1. In the Driver Mode Selection area select **Raw Ethernet** (Figure 2-15).
2. Click the **Install** button. The Virtex-7 XT Connectivity TRD Control and Monitoring Interface starts with **Performance Mode (Raw Ethernet)** displayed by default (**Figure 2-16**). The user can configure packet size in this mode. The **System Monitor** tab monitors system power consumption and die temperature.

3. Click **Start All** to start tests on all channels at once or **Start** for each data path to start each channel separately.

---

**Figure 2-15:** **Raw Ethernet Driver Installation**
4. Click the **Plots** tab to see performance on system-to-card and card-to-system (Figure 2-17).
5. Stop the raw ethernet test by clicking **Stop All** or stop an individual datapath by clicking **Stop** associated with the individual datapath.

6. Click the **Block Diagram** tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode (Figure 2-18).

**Figure 2-17:** Raw Ethernet Driver Interface
7. Close the Virtex-7 XT Connectivity TRD Control and Monitoring Interface by clicking X in the upper right corner. Closing the interface stops any running test, uninstalls the driver, and returns to the TRD Setup window.

**Application Mode**

With the TRD Setup window displayed:

1. In the Driver Mode Selection area select **Application** (Figure 2-19).

**Note:** Do not select the Peer-to-Peer option if a peer machine is not available with 10G NIC or an identical VC709 setup.
2. Click **Install**. After installing the application mode driver the Virtex-7 XT Connectivity TRD Control and Monitoring Interface starts (see Figure 2-20). However, in application mode the user cannot start or stop a test because the traffic is generated by the networking stack.

![Application Mode Driver Installation](image)
3. Open a command prompt on the host PC and ping the four network interfaces by entering:

   % ping 10.60.0.1
   % ping 10.60.1.1
   % ping 10.60.2.1
   % ping 10.60.3.1

The results should be similar to the output shown in Figure 2-21.

**Figure 2-20: Application Driver Interface**
4. Click the **Block Diagram** tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode. See Figure 2-22.

![Figure 2-21: System Output from Ping of Network Interfaces]

---

**Figure 2-21:** System Output from Ping of Network Interfaces
---

4. Click the **Block Diagram** tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode. See Figure 2-22.
Conclusion

5. Close the Virtex-7 XT Connectivity TRD Control and Monitoring Interface by clicking X in the upper right corner. Closing the interface stops any running test, uninstalls the driver, and returns to the TRD setup window.

This completes the demonstration of the three modes of operation provided by the design. Refer to the Virtex-7 XT Connectivity Targeted Reference Design User Guide (UG962) for testing application mode when connecting to a peer machine.

By completing the steps in this getting started guide the user carries out a simple hardware bring-up of the Virtex-7 XT Connectivity TRD in three different modes and obtains initial hands-on experience with the connectivity kit.
Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support

For continual updates, add the Answer Record to your myAlerts:

www.xilinx.com/support/myalerts

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the VC709 board and its documentation is available on the following websites.

The Virtex®-7 VC709 Evaluation Kit Product Page:

www.xilinx.com/vc709

The Virtex-7 VC709 Evaluation Kit Master Answer Record:

www.xilinx.com/support/answers/51901.htm

These Xilinx documents provide supplemental material useful with this guide:

UG887, VC709 Evaluation Board for the Virtex-7 FPGA User Guide

UG962, Virtex-7 FPGA XT Connectivity Targeted Reference Design for the VC709 Board User Guide

PG023, Virtex-7 FPGA Gen3 Integrated Block for PCI Express

WP350, Understanding Performance of PCI Express Systems

PG035, LogiCORE IP AXI Stream Interconnect

PG038, LogiCORE IP AXI Virtual FIFO Controller: Product guide for Vivado Design Suite
Appendix A: Additional Resources

**UG586**, Xilinx Memory Interface Generator User Guide

**UG476**, 7 Series FPGAs GTX/GTH Transceivers User Guide

**PG072**, LogiCORE IP 10-Gigabit Ethernet MAC Product Guide


**UG129**, PicoBlaze 8-bit Embedded Microcontroller User Guide

## References

The following websites provide supplemental material useful with this guide:

1. Northwest Logic DMA Backend core
   [nwlogic.com/products/docs/DMA_Back-End_Core.pdf](nwlogic.com/products/docs/DMA_Back-End_Core.pdf)

2. Fedora project
   [fedoraproject.org](fedoraproject.org)
   Fedora is a Linux-based operating system used in the development of this TRD.

3. 10G MMF SFP+ SR Optical Transceivers: Avago AFBR-703SDZ

4. LC to LC OM3 10G fiber optic patch cable:
   Amphenol Cables on Demand™ (ACD) FO-10GGBLCX20-001
   [http://www.cablesondemand.com/category/FO10GGBMM/URvars/Catalog/Library/InfoManage/10-GIGABIT_MULTI MODE_CABLES ...htm](http://www.cablesondemand.com/category/FO10GGBMM/URvars/Catalog/Library/InfoManage/10-GIGABIT_MULTI MODE_CABLES ...htm)

5. Tera Term home page

6. Silicon Labs USB-UART drivers:
   [www.silabs.com/Support%20Documents/Software/CP210x_VCP_Windows.zip](www.silabs.com/Support%20Documents/Software/CP210x_VCP_Windows.zip)

7. Virtex-7 family FPGA Product Table:
   [www.xilinx.com/publications/prod_mktg/Virtex7-Product-Table.pdf](www.xilinx.com/publications/prod_mktg/Virtex7-Product-Table.pdf)

8. VC709 product page:

9. Silicon Labs CP210x USB to UART Bridge VCP Drivers:
   [http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx](http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx)

10. Master Answer Record:
    [www.xilinx.com/support/answers/51901.htm](www.xilinx.com/support/answers/51901.htm)
Warranty

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