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## ***Spartan-6 FPGA SP605 Evaluation Kit FAQ***

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### Overview

This document answers the most frequently asked questions about the Spartan®-6 FPGA SP605 Evaluation Kit.

**Question 1:** *Where can I purchase a kit?*

You can purchase your SP605 Evaluation Kit online at:

<http://www.xilinx.com/products/devkits/EK-S6-SP605-G.htm>

Or contact your local distributor or representative at:

[http://www.xilinx.com/company/sales/ww\\_disti.htm](http://www.xilinx.com/company/sales/ww_disti.htm)

**Question 2:** *When will I get my kit?*

Lead times vary based on inventory and availability. For more information, go to:

[http://www.xilinx.com/onlinestore/s6\\_boards.htm](http://www.xilinx.com/onlinestore/s6_boards.htm)

Or contact your local distributor at:

[http://www.xilinx.com/company/sales/ww\\_disti.htm](http://www.xilinx.com/company/sales/ww_disti.htm)

The software is available for you to download immediately upon purchasing the kit. When you place your order, you are sent an e-mail with instructions to help you to register and generate a software license. See [Question 11: How do I register and install my software?](#) for instructions.

**Question 3:** *What is included in the Spartan-6 FPGA SP605 Evaluation Kit?*

The kit includes these items:

- SP605 Base Board  
Includes the XC6SLX45T-FGG484-3CES FPGA.
- Welcome Letter
- FPGA Design Software

A DVD containing Xilinx® ISE® Design Suite: Logic Edition. The version included with the SP605 Evaluation Kit is locked to the XC6SLX45T device (see [Software-Related Questions](#)).

- Reference Designs

Available online on the SP605 Evaluation Kit product page.

- Base Reference Design – Demonstrates board functionality and provides a reference design and tutorial demonstrating how to download, modify, and customize a design.

- Memory Controller Design – Demonstrates how to connect and design with the Memory Controller in the Spartan-6 FPGA.
- MultiBoot Configuration Design – Demonstrates how to implement the MultiBoot functionality and how to configure with one design and then automatically configure with another.
- Reference Design for x1 PCIe® – Basic memory transfer reference design for PCIe.
- iBERT Transceiver Reference Design – Basic design to test a GTP transceiver as a loopback channel
- Documentation
  - Hardware Setup Guide – Step-by-step guide for connecting cables, setting switches and jumpers, and powering on for the first time.
  - Getting Started Guide – Step-by-step guide to running the diagnostic demonstration, running the base reference design, and installing the software.
  - Hardware User Guide – Detailed description of the SP605 Board features, jumper settings, options, and pin location tables.
  - Reference Design User Guide – Step-by-step guide describing, implementing, modifying, and customizing the SP605 reference designs.
  - Board Design Files – Schematics, Gerber files, and the bill of materials.
- Cables and Power Supply
  - 12V universal power adapter
  - Two USB A/MiniB cables (for download and debug)
  - Ethernet Cable
  - DVI to VGA Adaptor

## SP605 Board Questions

**Question 4:** *What is the speed grade of the Spartan-6 LX45T FPGA on the board?*

The board is populated with a -3CES speed grade Spartan-6 XC6SLX45T FGG FPGA.

**Question 5:** *What is the return policy for boards and software?*

To return a board or cable purchased through normal distribution channels, contact the authorized distributor who sold you the product. More information is available at: <http://www.xilinx.com/products/quality/rma.htm>

**Question 6:** *Why are there two USB connectors on the SP605 board?*

The USB port labeled USB/JTAG is specifically used for downloading a configuration bitstream and programming the flash memory. This port can be used as a debug port, using JTAG and the ChipScope™ logic analyzer, but cannot be used as a standard USB device port. The other USB port (labeled USB UART) is a USB-to-UART bridge that can be used as a serial communication channel.

**Question 7:** *What expansion ports are available on the SP605 board?*

The SP605 board has two expansion ports. One is the FPGA Mezzanine Card (FMC) connector (see [Question 8](#)). The other expansion port provides for I/Os configured as one row of  $V_{CC}$ , GND, and four I/Os. A number of small peripheral cards called

Peripheral Modules (Pmods) are available at:

<http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9>

**Question 8:** *What is the FMC expansion connector and what can I connect to it?*

The FMC is an expansion card interface format developed by a consortium of companies, including FPGA vendors and end users. The interface provides a standard mezzanine card form factor, connectors, and modular interface to an FPGA located on a base board. Decoupling the I/O interfaces from the FPGA in this manner simplifies the design of the I/O interfacing modules while maximizing board reuse. More information is available at:

<http://www.xilinx.com/fmc/>

**Question 9:** *How do I get a copy of the FMC specification?*

FPGA Mezzanine (FMC) Card is a VITA specification available on VITA's website at:

<https://www.vita.com/online-store.html>

## Software-Related Questions

**Question 10:** *What is ISE Design Suite: Logic Edition?*

ISE Design Suite: Logic Edition is the industry's fully featured FPGA design solution for Linux, Windows XP, and Windows Vista. This is a full-feature software build; however, the version provided with the SP605 Evaluation Kit only targets the Spartan-6 XCS6LX45T device. To target other Xilinx devices, you need to buy an ISE software Logic Edition license. This software is the ideal downloadable solution for FPGA and CPLD designs offering HDL synthesis and simulation, implementation, device fitting, and JTAG programming. The ISE Design Suite: Logic Edition delivers a complete, front-to-back design flow providing instant access to the ISE software features and functionality at no cost. Xilinx has created a solution that allows convenient productivity by providing a design solution that is always up to date with error-free downloading and single file installation. Download this tool from:

<http://www.xilinx.com/support/download/index.htm>

**Question 11:** *How do I register and install my software?*

After you order the Spartan-6 FPGA SP605 Evaluation Kit, you are sent an e-mail with instructions to download and entitle the ISE Design Suite: Logic Edition software. You can also follow the instructions found here:

<http://www.xilinx.com/support/download/index.htm>

If you log in with the e-mail address that was provided with the purchase order, an account is created for you. If not, you need to register a new account.

The evaluation kit comes with "entitlement" to a seat of the ISE Design Suite: Logic Edition software and all associated updates for a one-year period, or as specified in your purchase order, if different.

To get started, visit the Xilinx software registration and entitlement site:

<http://www.xilinx.com/getproduct>

Generate a License:

Select the "Create New License" tab. Select the check box of the software you want to license and install. Select the check box for the "ISE Design Suite: WebPACK Edition, Node Locked."

**Note:** Laptop users might want to select your Hard Disk ID or Wireless Ethernet card HostID. If you are going to select an Ethernet adaptor, it is best to select your wireless card. If you select your Docking Station HostID, you are only licensed when you are docked. Also, many direct RJ45 Ethernet connections on laptop computers are powered down when not plugged into the network. So if you are not connected with a cable, you may also find that you are not licensed.

After you have selected a HostID, click the **Generate Node Locked License** button. This generates your license in the **Manage Licenses** tab and e-mails you a copy of the license. Use this license later as part of the software installation process. More installation and licensing information is available in [UG631, ISE Design Suite Installation, Licensing, and Release Notes](#).

#### Installing the Software:

Select the **Download Software** tab. You have the option to run a Web Install client, or download the ISE Design Suite: Logic Edition image. If you are on a fast network, Xilinx recommends downloading the *Individual Files ISE Design Suite: Logic Edition* image. If not, the *Web Install Client* is a good option. In both cases, select the ISE Design Suite: Logic Edition and follow these steps:

1. Download Web Install Client or Full DVD Image.
2. Extract the contents of archive.
3. Run `xsetup.exe`.

### Question 12: *What other software would be helpful and why?*

While ISE Design Suite: Logic Edition software supports all the features of the SP605 board, there are some additional software tools that can be helpful. These are found in the ISE Design Suite: Embedded Edition, ISE Design Suite: DSP Edition, or ISE Design Suite: System Edition software. See:

<http://www.xilinx.com/tools/designtools.htm>

- ChipScope Pro Analyzer (included with SP605)

An FPGA debug and verification tool. Using the CORE Generator™ or Core Inserter tool in the ChipScope Pro software, put ChipScope software specific logic into your design, called a ChipScope tool core. Then, you can connect to ChipScope tool cores later using the ChipScope analyzer to debug or validate your design.

- The Embedded Development Kit (EDK) tools.

The ISE Design Suite: Embedded Edition includes all of the features and technologies found in the ISE Design Suite: Logic Edition plus additional tools and IP required for Xilinx FPGA designs with embedded PowerPC® processor cores and/or MicroBlaze™ soft processor cores.

- The AccelDSP™ Synthesis Tool

A product that allows you to transform a MATLAB® software floating-point design into a hardware module that can be implemented in a Xilinx FPGA. The AccelDSP synthesis tool features an easy-to-use graphical user interface that controls an integrated environment with other design tools, such as MATLAB software, ISE software tools, and other industry-standard HDL simulators and logic synthesizers.

- System Generator

A DSP design tool from Xilinx that enables the use of The Mathworks model-based design environment Simulink® software for FPGA design. Designs are captured

in the DSP-friendly Simulink software modeling environment, using a Xilinx specific block set. All of the downstream FPGA implementation steps, including synthesis and place and route, are automatically performed to generate an FPGA programming file.

- PlanAhead™ Software (included with the SP605 Evaluation Kit)

A design and analysis software product used to design large FPGA devices. The core technology includes a hierarchical floorplanning tool that can partition the physical design into smaller, more manageable pieces, thus reducing the time to understand, design, verify, and implement the FPGA.

## Getting More Information

### *Question 13: Where do I get more information?*

Check the SP605 product page for the latest information:

<http://www.xilinx.com/products/devkits/EK-S6-SP605-G.htm>

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/08/10	1.0	Initial Xilinx release.

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