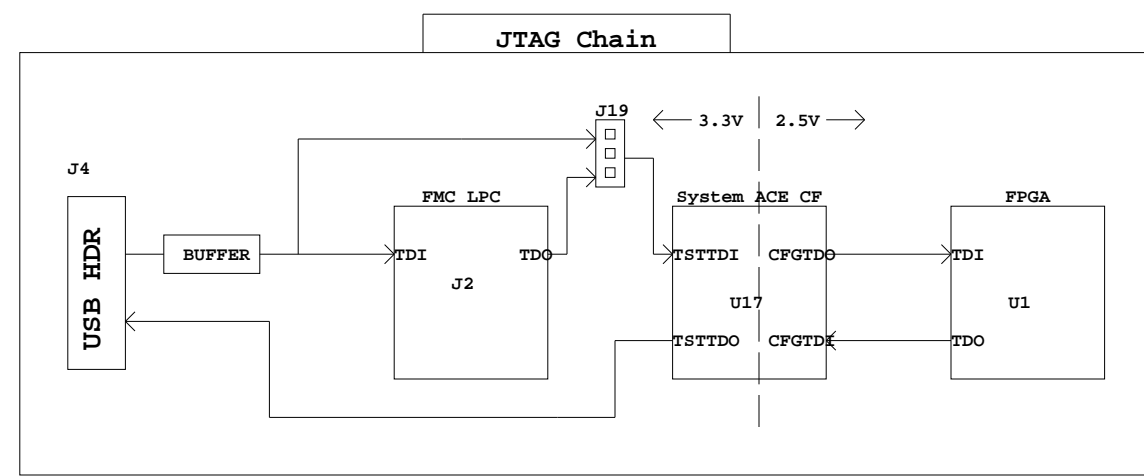
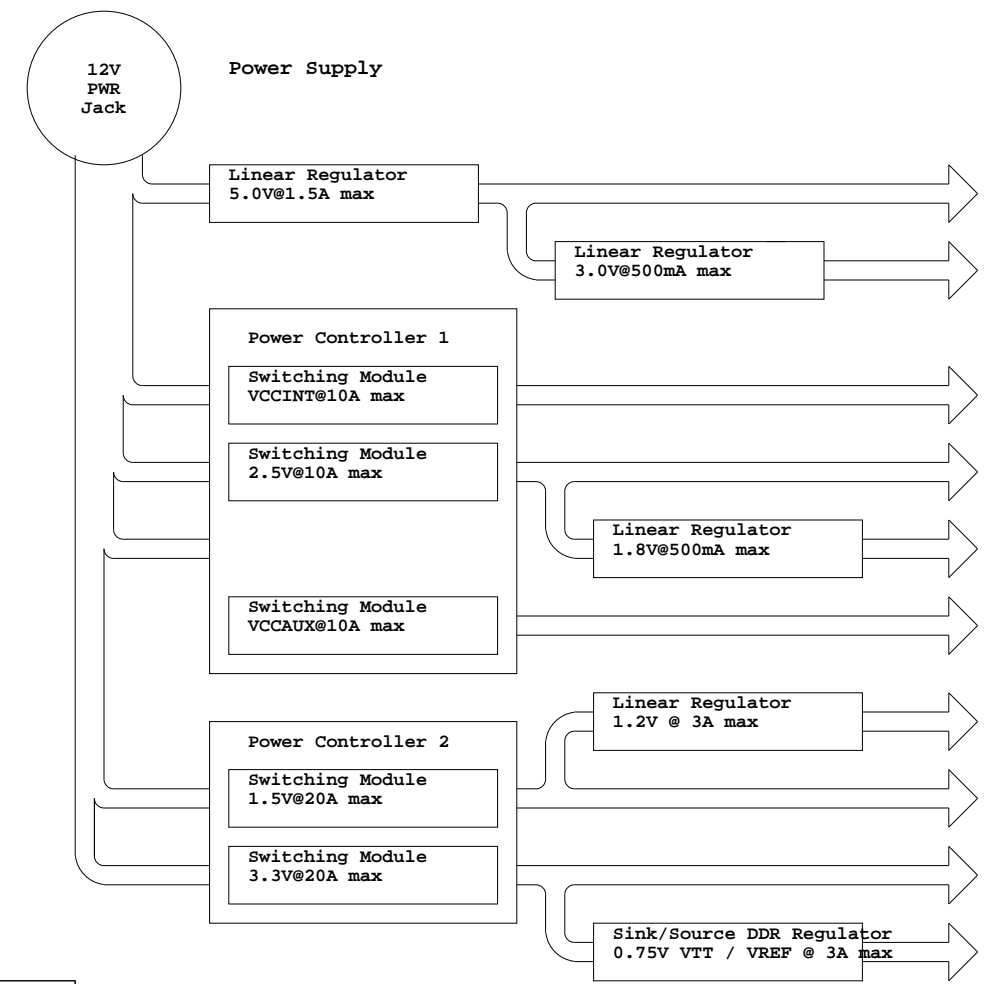
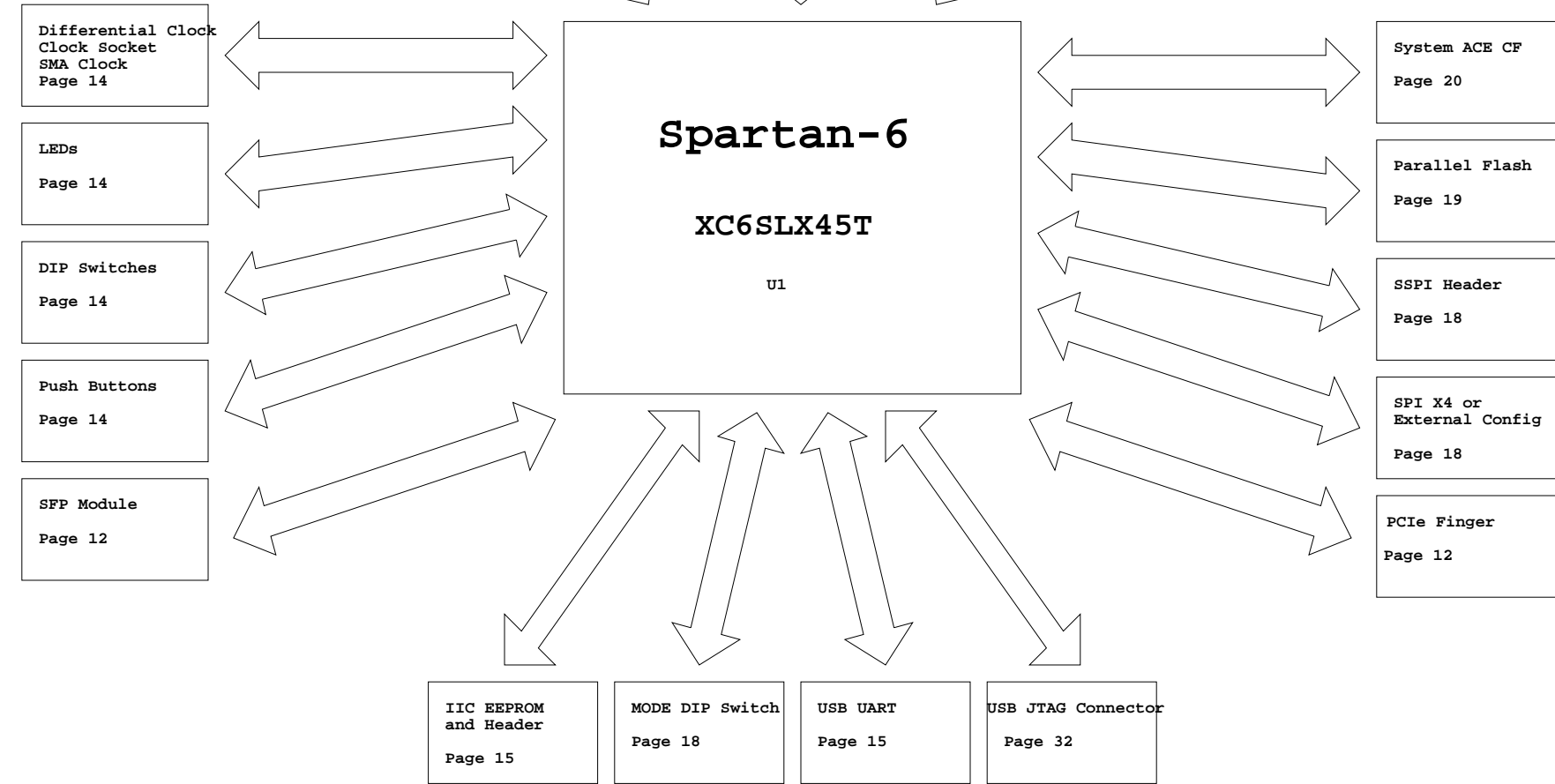


DDR3
Page 9

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Page 10

10/100/1000 Ethernet
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IIC Addressing	
U4	0b1010100
J2	EEPROM: 0b1010010 Other Devices: 0bXXXXX10

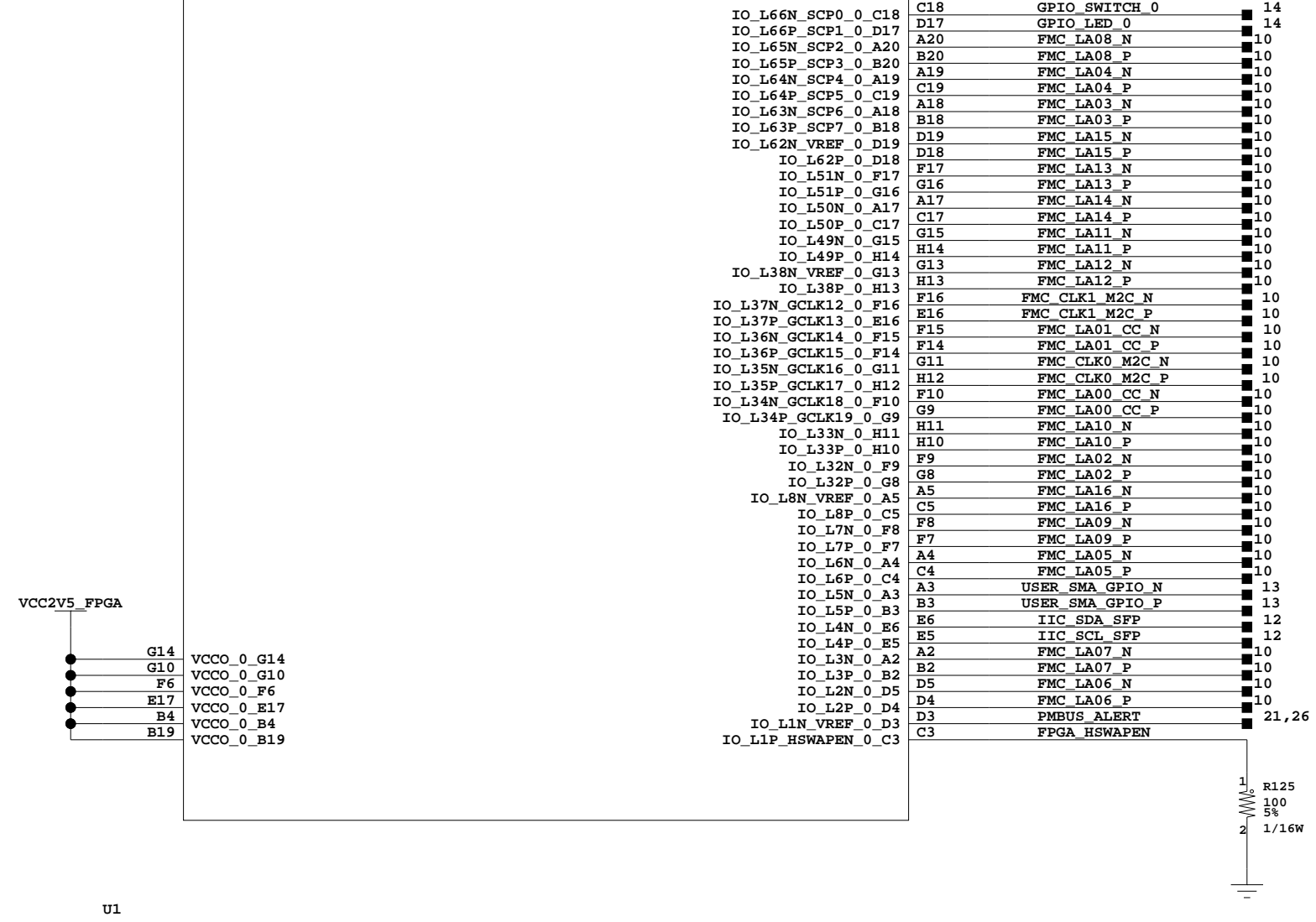
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Title: SP605 Block Diagram SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM

PCB P/N: 0431534
SCH P/N: 0381305
Test P/N: TSS0123
ART P/N: 1280473

Date: 9-25-2009_10:32 Ver: D
Sheet Size: B Rev: 04
Sheet **1** of **35** Drawn By BF

DUT
BANK 0
6slx45tfg484



FPGA Bank 0



Title: FPGA Bank 0
SCHEM, ROHS COMPLIANT
SP605 EVALUATION PLATFORM

Pcb P/N: 0431534
SCH P/N: 0381305
Test P/N: TSS0123
ART P/N: 1280473

Date: 9-18-2009_15:04 Ver: D

Sheet Size: B Rev: 04

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DUT
BANK 1
6slx45tfg484

IO_L74N_DOUT_BUSY_1_V20	V20	PHY_MDIO	11
IO_L74P_AWAKE_1_V19	V19	FPGA_AWAKE	18
IO_L73N_1_T18	T18	FLASH_WAIT	19
IO_L73P_1_T19	T19	FLASH_ADV_B	19
IO_L72N_1_T17	T17	SFP_LOS	12
IO_L72P_1_R17	R17	DVI_D11	17
IO_L71N_1_P18	P18	DVI_D10	17
IO_L71P_1_P17	P17	DVI_D9	17
IO_L70N_1_R16	R16	DVI_D8	17
IO_L70P_1_R15	R15	DVI_D7	17
IO_L61N_1_M18	M18	DVI_D6	17
IO_L61P_1_M17	M17	DVI_D5	17
IO_L60N_1_P16	P16	DVI_D4	17
IO_L60P_1_N16	N16	DVI_D3	17
IO_L59N_1_T20	T20	DVI_D2	17
IO_L59P_1_U19	U19	DVI_D1	17
IO_L58N_1_N15	N15	PHY_CRD	11
IO_L58P_1_M16	M16	PHY_COL	11
IO_L53N_VREF_1_R19	R19	PHY_MDC	11
IO_L53P_1_P19	P19	PHY_RXD0	11
IO_L52N_M1DQ15_1_Y22	Y22	PHY_RXD1	11
IO_L52P_M1DQ14_1_Y21	Y21	PHY_RXD2	11
IO_L51N_M1DQ13_1_W22	W22	PHY_RXD3	11
IO_L51P_M1DQ12_1_W20	W20	PHY_RXD4	11
IO_L50N_M1UDQS_1_V22	V22	PHY_RXD5	11
IO_L50P_M1UDQS_1_V21	V21	PHY_RXD6	11
IO_L49N_M1DQ11_1_U22	U22	PHY_RXD7	11
IO_L49P_M1DQ10_1_U20	U20	PHY_RXER	11
IO_L48N_M1DQ9_1_T22	T22	PHY_RXCTL_RXDV	11
IO_L48P_HDC_M1DQ8_1_T21	T21	IIC_SCL_MAIN	10,15
IO_L47N_LDC_M1DQ1_1_R22	R22	IIC_SDA_MAIN	10,15
IO_L47P_FWE_B_M1DQ0_1_R20	R20	FLASH_WE_B	19
IO_L46N_FOE_B_M1DQ3_1_P22	P22	FLASH_OE_B	19
IO_L46P_FCS_B_M1DQ2_1_P21	P21	FLASH_CE_B	19
IO_L45N_A0_M1DQSN_1_N22	N22	FLASH_A0	19
IO_L45P_A1_M1DQS_1_N20	N20	FLASH_A1	19
IO_L44N_A2_M1DQ7_1_M22	M22	FLASH_A2	19
IO_L44P_A3_M1DQ6_1_M21	M21	FLASH_A3	19
IO_L43N_GCLK4_M1DQ5_1_L22	L22	NC	
IO_L43P_GCLK5_M1DQ4_1_L20	L20	PHY_TXCLK	11
IO_L42N_GCLK6_M1LDM_1_N19	N19	CLK_33MHZ_SYSACE	20
IO_L42P_GCLK7_M1UDM_1_P20	P20	PHY_RXCLK	11
IO_L41N_GCLK8_M1CASN_1_K22	K22	SYSCLK_N	14
IO_L41P_GCLK9_M1RASN_1_K21	K21	SYSCLK_P	14
IO_L40N_GCLK10_M1A6_1_M19	M19	USER_SMA_CLOCK_N	13
IO_L40P_GCLK11_M1A5_1_M20	M20	USER_SMA_CLOCK_P	13
IO_L39N_M1ODT_1_J22	J22	PHY_RESET	11
IO_L39P_M1A3_1_J20	J20	PHY_INT	11
IO_L38N_A4_M1CLKN_1_L19	L19	FLASH_A4	19
IO_L38P_A5_M1CLK_1_K20	K20	FLASH_A5	19
IO_L37N_A6_M1A1_1_H22	H22	FLASH_A6	19
IO_L37P_A7_M1A0_1_H21	H21	FLASH_A7	19
IO_L36N_A8_M1BA1_1_L17	L17	FLASH_A8	19
IO_L36P_A9_M1BA0_1_K17	K17	FLASH_A9	19
IO_L35N_A10_M1A2_1_G22	G22	FLASH_A10	19
IO_L35P_A11_M1A7_1_G20	G20	FLASH_A11	19
IO_L34N_A12_M1BA2_1_K18	K18	FLASH_A12	19
IO_L34P_A13_M1WE_1_K19	K19	FLASH_A13	19
IO_L33N_A14_M1A4_1_H20	H20	FLASH_A14	19
IO_L33P_A15_M1A10_1_J19	J19	FLASH_A15	19
IO_L32N_A16_M1A9_1_E22	E22	FLASH_A16	19
IO_L32P_A17_M1A8_1_E20	E20	FLASH_A17	19
IO_L31N_A18_M1A12_1_F22	F22	FLASH_A18	19
IO_L31P_A19_M1CKE_1_F21	F21	FLASH_A19	19
IO_L30N_A20_M1A11_1_H19	H19	FLASH_A20	19
IO_L30P_A21_M1RESET_1_H18	H18	FLASH_A21	19
IO_L29N_A22_M1A14_1_F20	F20	FLASH_A22	19
IO_L29P_A23_M1A13_1_G19	G19	FLASH_A23	19
IO_L28N_VREF_1_D22	D22	DVI_GPI01	17
IO_L28P_1_D21	D21	GPIO_LED_2	14
IO_L21N_1_K16	K16	DVI_D0	17
IO_L21P_1_L15	L15	DVI_RESET_B	17
IO_L20N_1_C22	C22	DVI_XCLK_N	17
IO_L20P_1_C20	C20	DVI_XCLK_P	17
IO_L19N_1_J17	J17	DVI_DE	17
IO_L19P_1_J16	J16	DVI_H	17
IO_L10N_1_B22	B22	DVI_V	17
IO_L10P_1_B21	B21	USB_1_RX	15
IO_L9N_1_H17	H17	USB_1_TX	15
IO_L9P_1_H16	H16	PMBUS_CTRL	21,26
IO_L1N_A24_VREF_1_F19	F19	USB_1_RTS	15
IO_L1P_A25_1_F18	F18	USB_1_CTS	15

VCC2V5_FPGA

W21	VCC0_1_W21
U18	VCC0_1_U18
R21	VCC0_1_R21
N18	VCC0_1_N18
L21	VCC0_1_L21
L16	VCC0_1_L16
J18	VCC0_1_J18
G21	VCC0_1_G21
E19	VCC0_1_E19
C21	VCC0_1_C21

U1

FPGA Bank 1



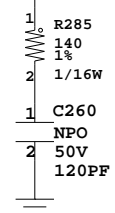
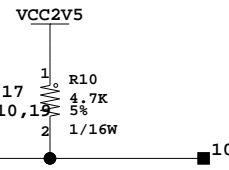
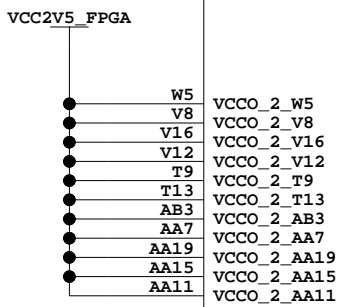
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SCHEM, ROHS COMPLIANT
SP605 EVALUATION PLATFORM

PCB P/N: 0431534
SCH P/N: 0381305
Test P/N: TSS0123
ART P/N: 1280473

Date:	9-18-2009_15:04	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	3 of 35	Drawn By	BF

DUT
BANK 2
6slx45tfg484

IO_L65N_CS0_B_2_AA3	AA3	SPI_CS_B	18
IO_L65P_INIT_B_2_Y4	Y4	FPGA_INIT_B	14,20
IO_L64N_D9_2_U6	U6	FLASH_D9	19
IO_L64P_D8_2_T7	T7	FLASH_D8	19
IO_L63N_2_AB4	AB4	GPIO_LED_1	14
IO_L63P_2_AA4	AA4	IIC_SDA_DVI	16,17
IO_L62N_D6_2_AB5	AB5	FLASH_D6	19
IO_L62P_D5_2_Y5	Y5	FLASH_D5	19
IO_L60N_2_Y6	Y6	GPIO_SWITCH_1	14
IO_L60P_2_W6	W6	GPIO_SWITCH_2	14
IO_L59N_2_R8	R8	FMC_LA20_N	10
IO_L59P_2_R9	R9	FMC_LA20_P	10
IO_L58N_2_W8	W8	FMC_LA22_N	10
IO_L58P_2_V7	V7	FMC_LA22_P	10
IO_L57N_2_U8	U8	PHY_TXER	11
IO_L57P_2_T8	T8	PHY_TXCTL_TXEN	11
IO_L50N_2_V9	V9	FMC_LA23_N	10
IO_L50P_2_U9	U9	FMC_LA23_P	10
IO_L49N_D4_2_AB6	AB6	FLASH_D4	19
IO_L49P_D3_2_AA6	AA6	FLASH_D3	19
IO_L48N_RDWR_B_VREF_2_Y8	Y8	SFP_TX_DISABLE_FPGA	12
IO_L48P_D7_2_W9	W9	FLASH_D7	19
IO_L47N_2_AB7	AB7	PHY_TXC_GTXCLK	11
IO_L47P_2_Y7	Y7	NC	
IO_L46N_2_U10	U10	PHY_TXD0	11
IO_L46P_2_T10	T10	PHY_TXD1	11
IO_L45N_2_AB8	AB8	PHY_TXD2	11
IO_L45P_2_AA8	AA8	PHY_TXD3	11
IO_L44N_2_Y10	Y10	PMBUS_DATA	21,26
IO_L44P_2_W10	W10	PMBUS_CLK	21,26
IO_L43N_2_AB9	AB9	PHY_TXD4	11
IO_L43P_2_Y9	Y9	PHY_TXD5	11
IO_L42N_2_W11	W11	FMC_LA21_N	10
IO_L42P_2_V11	V11	FMC_LA21_P	10
IO_L41N_VREF_2_AB10	AB10	FMC_LA27_N	10
IO_L41P_2_AA10	AA10	FMC_LA27_P	10
IO_L40N_2_Y12	Y12	PHY_TXD6	11
IO_L40P_2_W12	W12	PHY_TXD7	11
IO_L32N_GCLK28_2_AB11	AB11	FMC_LA17_CC_N	10
IO_L32P_GCLK29_2_Y11	Y11	FMC_LA17_CC_P	10
IO_L31N_GCLK30_D15_2_AB12	AB12	FLASH_D15	19
IO_L31P_GCLK31_D14_2_AA12	AA12	FLASH_D14	19
IO_L30N_GCLK0_USERCLK_2_AB13	AB13	USER_CLOCK	14
IO_L30P_GCLK1_D13_2_Y13	Y13	FLASH_D13	19
IO_L29N_GCLK2_2_U12	U12	FMC_LA18_CC_N	10
IO_L29P_GCLK3_2_T12	T12	FMC_LA18_CC_P	10
IO_L23N_2_U15	U15	FMC_LA29_N	10
IO_L23P_2_T15	T15	FMC_LA29_P	10
IO_L22N_2_T11	T11	FMC_LA19_N	10
IO_L22P_2_R11	R11	FMC_LA19_P	10
IO_L21N_2_AB15	AB15	FMC_LA30_N	10
IO_L21P_2_Y15	Y15	FMC_LA30_P	10
IO_L20N_2_Y14	Y14	FMC_LA25_N	10
IO_L20P_2_W14	W14	FMC_LA25_P	10
IO_L19N_2_AB16	AB16	FMC_LA28_N	10
IO_L19P_2_AA16	AA16	FMC_LA28_P	10
IO_L18N_2_W13	W13	IIC_SCL_DVI	16,17
IO_L18P_2_V13	V13	FMC_PWR_GOOD_FLASH_RST_B	7,10,15
IO_L17N_2_W15	W15	GPIO_LED_3	14
IO_L17P_2_Y16	Y16	FMC_PRSENT_M2C_L	
IO_L16N_VREF_2_U13	U13	FMC_LA26_N	10
IO_L16P_2_U14	U14	FMC_LA26_P	10
IO_L15N_2_AB17	AB17	FMC_LA33_N	10
IO_L15P_2_Y17	Y17	FMC_LA33_P	10
IO_L14N_D12_2_AB18	AB18	FLASH_D12	19
IO_L14P_D11_2_AA18	AA18	FLASH_D11	19
IO_L13N_D10_2_AB19	AB19	FLASH_D10	19
IO_L13P_M1_2_Y19	Y19	FPGA_M1	18
IO_L12N_D2_MISO3_2_T14	T14	FPGA_D2_MISO3	18,19
IO_L12P_D1_MISO2_2_R13	R13	FPGA_D1_MISO2	18,19
IO_L6N_2_AB14	AB14	FMC_LA24_N	10
IO_L6P_2_AA14	AA14	FMC_LA24_P	10
IO_L5N_2_Y18	Y18	FMC_LA32_N	10
IO_L5P_2_W17	W17	FMC_LA32_P	10
IO_L4N_VREF_2_V15	V15	FMC_LA31_N	10
IO_L4P_2_U16	U16	FMC_LA31_P	10
IO_L3N_MOSI_CSI_B_MISO0_2_AB20	AB20	FPGA_MOSI_CSI_B_MISO0	18
IO_L3P_D0_DIN_MISO1_2_AA20	AA20	FPGA_D0_DIN_MISO_MISO1	18,19
IO_L2N_CMPMOSI_2_W18	W18	FPGA_CMP_MOSI	18
IO_L2P_CMPCLK_2_V17	V17	FPGA_CMP_CLK	18
IO_L1N_M0_CMPMISO_2_AA21	AA21	FPGA_M0_CMP_MISO	18
IO_L1P_CCLK_2_Y20	Y20	FPGA_CCLK	18



FPGA Bank 2

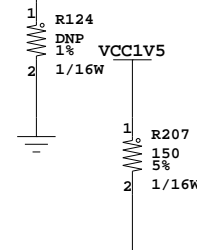
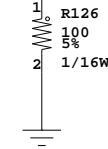


Title: FPGA Bank 2 SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
Date: 9-18-2009_15:04	Ver: D	
Sheet Size: B	Rev: 04	
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DUT
BANK 3
6slx45tfg484

IO_L83N_VREF_3_B1	B1		
IO_L83P_3_C1	C1	GPIO_BUTTON3	14
IO_L82N_3_G6	G6	GPIO_BUTTON1	14
IO_L82P_3_F5	F5	GPIO_BUTTON2	14
IO_L81N_3_H8	H8	CPU_RESET	14
IO_L81P_3_J7	J7	PCIE_PERST_B_LS	35
IO_L80N_3_G7	G7	GPIO_HEADER_0_LS	35
IO_L80P_3_H6	H6	GPIO_HEADER_1_LS	35
IO_L60N_3_E4	E4	GPIO_SWITCH_3	14
IO_L60P_3_F3	F3	GPIO_BUTTON0	14
IO_L59N_3_D1	D1	GPIO_HEADER_2_LS	35
IO_L59P_3_D2	D2	SYSACE_MPA06_LS	35
IO_L58N_3_G4	G4	SYSACE_MPA05_LS	35
IO_L58P_3_H4	H4	SYSACE_MPA04_LS	35
IO_L57N_VREF_3_K8	K8		
IO_L57P_3_K7	K7	FPGA_ONCHIP_TERM2	
IO_L55N_M3A14_3_H5	H5	MEM1_A14	9
IO_L55P_M3A13_3_J6	J6	MEM1_A13	9
IO_L54N_M3A11_3_E1	E1	MEM1_A11	9
IO_L54P_M3RESET_3_E3	E3	MEM1_RESET_B	9
IO_L53N_M3A12_3_F1	F1	MEM1_A12	9
IO_L53P_M3CKE_3_F2	F2	MEM1_CKE	9
IO_L52N_M3A9_3_G1	G1	MEM1_A9	9
IO_L52P_M3A8_3_G3	G3	MEM1_A8	9
IO_L51N_M3A4_3_H3	H3	MEM1_A4	9
IO_L51P_M3A10_3_J4	J4	MEM1_A10	9
IO_L50N_M3BA2_3_H1	H1	MEM1_BA2	9
IO_L50P_M3WE_3_H2	H2	MEM1_WE_B	9
IO_L49N_M3A2_3_K5	K5	MEM1_A2	9
IO_L49P_M3A7_3_K6	K6	MEM1_A7	9
IO_L48N_M3BA1_3_J1	J1	MEM1_BA1	9
IO_L48P_M3BA0_3_J3	J3	MEM1_BA0	9
IO_L47N_M3A1_3_K1	K1	MEM1_A1	9
IO_L47P_M3A0_3_K2	K2	MEM1_A0	9
IO_L46N_M3CLKN_3_K3	K3	MEM1_CLK_N	9
IO_L46P_M3CLK_3_K4	K4	MEM1_CLK_P	9
IO_L45N_M3ODT_3_L6	L6	MEM1_ODT	9
IO_L45P_M3A3_3_M6	M6	MEM1_A3	9
IO_L44N_GCLK20_M3A6_3_L4	L4	MEM1_A6	9
IO_L44P_GCLK21_M3A5_3_M3	M3	MEM1_A5	9
IO_L43N_GCLK22_M3CASN_3_M4	M4	MEM1_CAS_B	9
IO_L43P_GCLK23_M3RASN_3_M5	M5	MEM1_RAS_B	9
IO_L42N_GCLK24_M3LDM_3_N4	N4	MEM1_LDM	9
IO_L42P_GCLK25_M3UDM_3_P3	P3	MEM1_UDM	9
IO_L41N_GCLK26_M3DQ5_3_L1	L1	MEM1_DQ5	9
IO_L41P_GCLK27_M3DQ4_3_L3	L3	MEM1_DQ4	9
IO_L40N_M3DQ7_3_M1	M1	MEM1_DQ7	9
IO_L40P_M3DQ6_3_M2	M2	MEM1_DQ6	9
IO_L39N_M3LDQSN_3_N1	N1	MEM1_LDQS_N	9
IO_L39P_M3LDQS_3_N3	N3	MEM1_LDQS_P	9
IO_L38N_M3DQ3_3_P1	P1	MEM1_DQ3	9
IO_L38P_M3DQ2_3_P2	P2	MEM1_DQ2	9
IO_L37N_M3DQ1_3_R1	R1	MEM1_DQ1	9
IO_L37P_M3DQ0_3_R3	R3	MEM1_DQ0	9
IO_L36N_M3DQ9_3_T1	T1	MEM1_DQ9	9
IO_L36P_M3DQ8_3_T2	T2	MEM1_DQ8	9
IO_L35N_M3DQ11_3_U1	U1	MEM1_DQ11	9
IO_L35P_M3DQ10_3_U3	U3	MEM1_DQ10	9
IO_L34N_M3UDQSN_3_V1	V1	MEM1_UDQS_N	9
IO_L34P_M3UDQS_3_V2	V2	MEM1_UDQS_P	9
IO_L33N_M3DQ13_3_W1	W1	MEM1_DQ13	9
IO_L33P_M3DQ12_3_W3	W3	MEM1_DQ12	9
IO_L32N_M3DQ15_3_Y1	Y1	MEM1_DQ15	9
IO_L32P_M3DQ14_3_Y2	Y2	MEM1_DQ14	9
IO_L31N_VREF_3_M8	M8		
IO_L31P_3_M7	M7	FPGA_ONCHIP_TERM1	
IO_L26N_3_R4	R4	SYSACE_D7_LS	35
IO_L26P_3_T3	T3	SYSACE_D6_LS	35
IO_L25N_3_P7	P7	SYSACE_D5_LS	35
IO_L25P_3_P6	P6	SYSACE_D4_LS	35
IO_L24N_3_T4	T4	SYSACE_D3_LS	35
IO_L24P_3_U4	U4	SYSACE_D2_LS	35
IO_L23N_3_N7	N7	SYSACE_D1_LS	35
IO_L23P_3_N6	N6	SYSACE_D0_LS	35
IO_L10N_3_AA1	AA1	SYSACE_MPERDY_LS	35
IO_L10P_3_AA2	AA2	SYSACE_MPIRQ_LS	35
IO_L9N_3_P4	P4	SYSACE_MPA03_LS	35
IO_L9P_3_P5	P5	SYSACE_MPA02_LS	35
IO_L8N_3_V3	V3	SYSACE_MPA01_LS	35
IO_L8P_3_V5	V5	SYSACE_MPA00_LS	35
IO_L7N_3_T5	T5	SYSACE_MPWE_LS	35
IO_L7P_3_T6	T6	SYSACE_MPOE_LS	35
IO_L2N_3_Y3	Y3	FPGA_VTEMP	
IO_L2P_3_W4	W4	SYSACE_MPCE_LS	35
IO_L1N_VREF_3_P8	P8		
IO_L1P_3_R7	R7	GPIO_HEADER_3_LS	35

VTTVREF



VCC1V5_FPGA

W2	VCC0_3_W2
U5	VCC0_3_U5
R2	VCC0_3_R2
N5	VCC0_3_N5
L7	VCC0_3_L7
L2	VCC0_3_L2
J5	VCC0_3_J5
G2	VCC0_3_G2
F4	VCC0_3_F4
C2	VCC0_3_C2

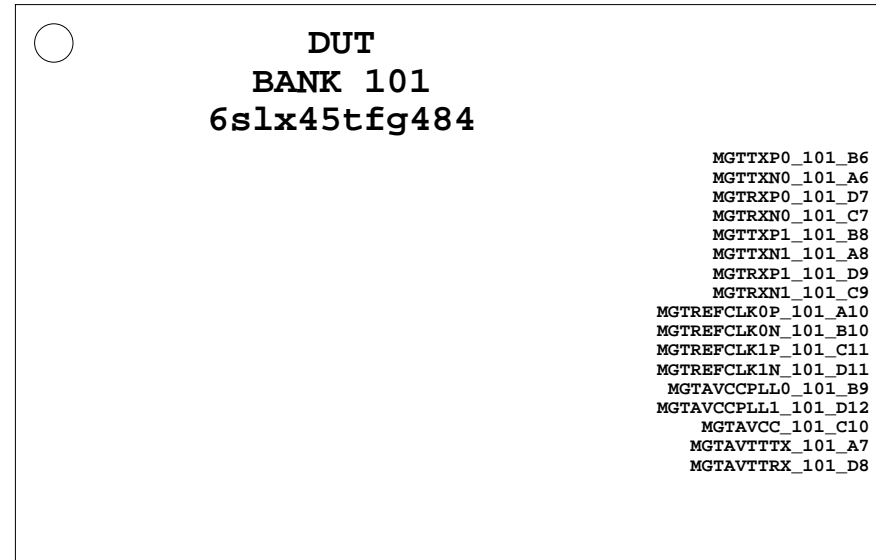
FPGA Bank 3



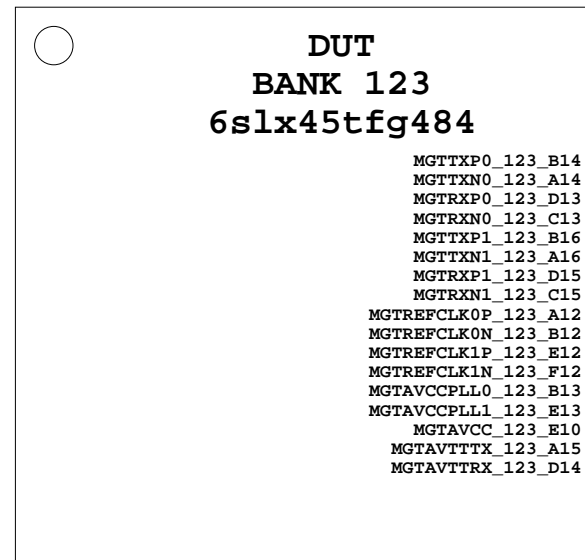
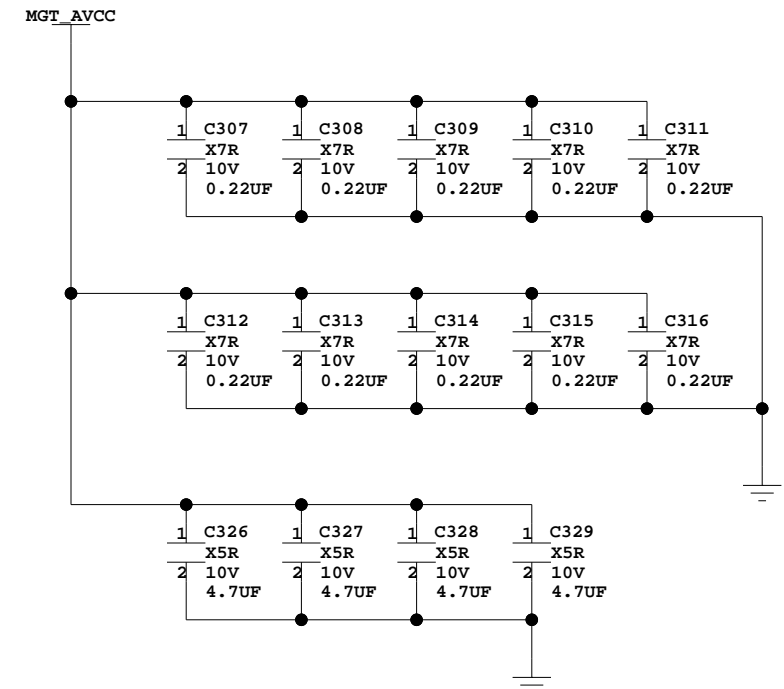
Title: FPGA Bank 3
SCHEM, ROHS COMPLIANT
SP605 EVALUATION PLATFORM

PCB P/N: 0431534
SCH P/N: 0381305
Test P/N: TSS0123
ART P/N: 1280473

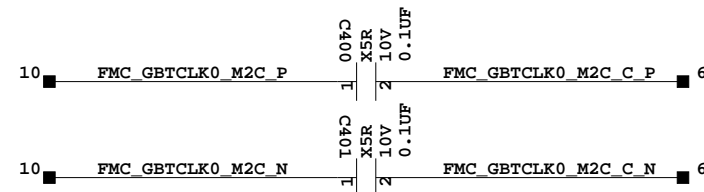
Date:	9-18-2009_15:04	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	5 of 35	Drawn By	BF



U1



U1



MGT Banks



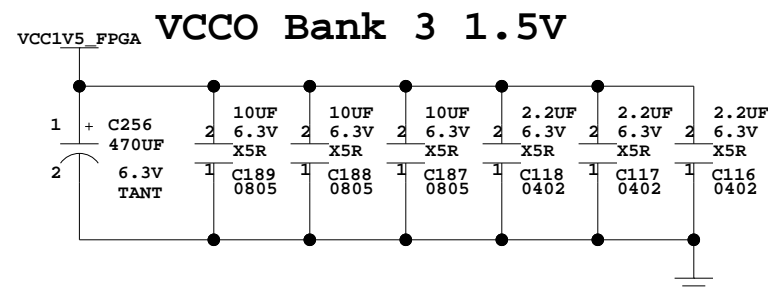
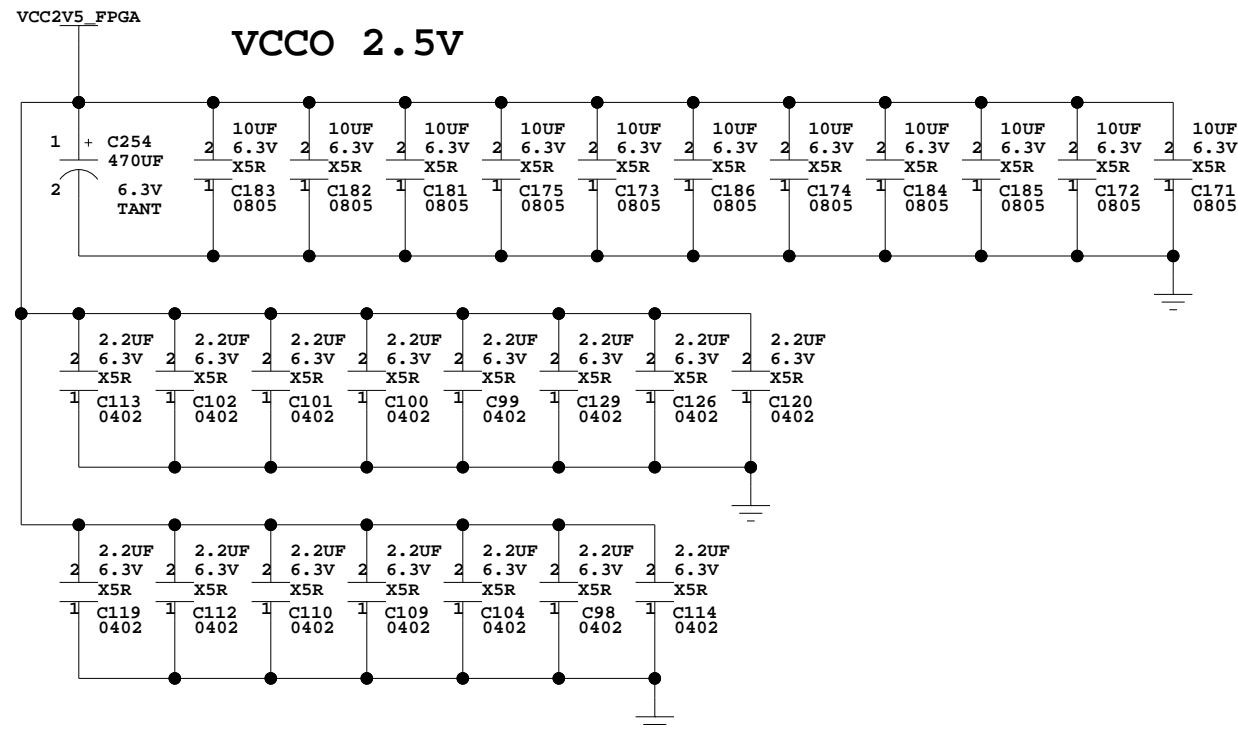
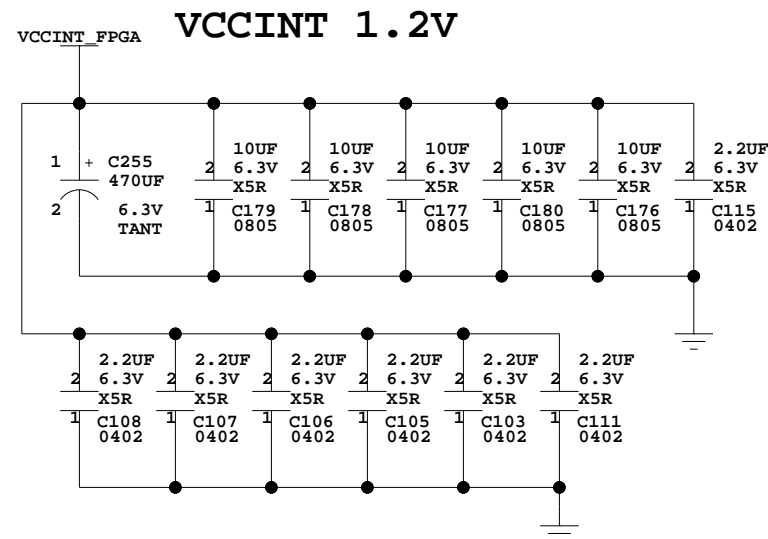
Title: MGT Banks
SCHEM, ROHS COMPLIANT
SP605 EVALUATION PLATFORM

PCB P/N: 0431534
SCH P/N: 0381305
Test P/N: TSS0123
ART P/N: 1280473

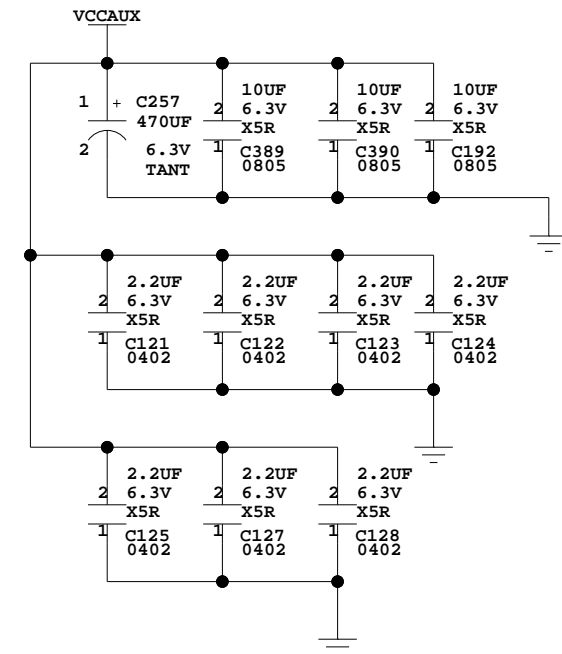
Date: 9-18-2009_15:04 Ver: D

Sheet Size: B Rev: 04

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VCCAUX 2.5V

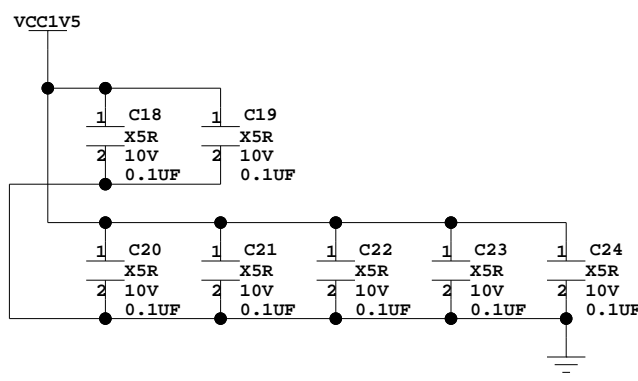
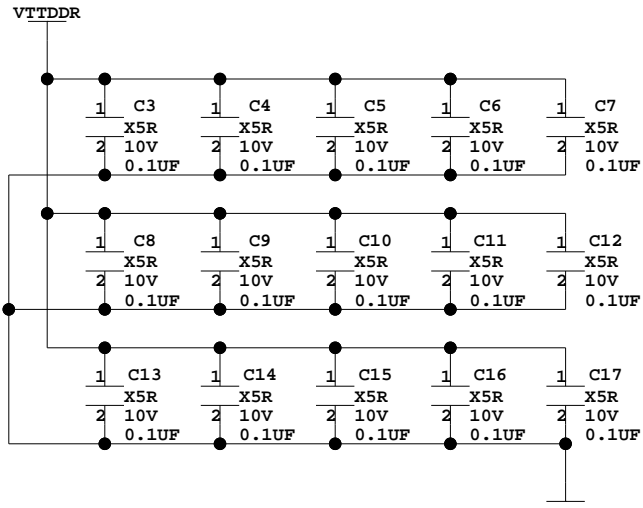
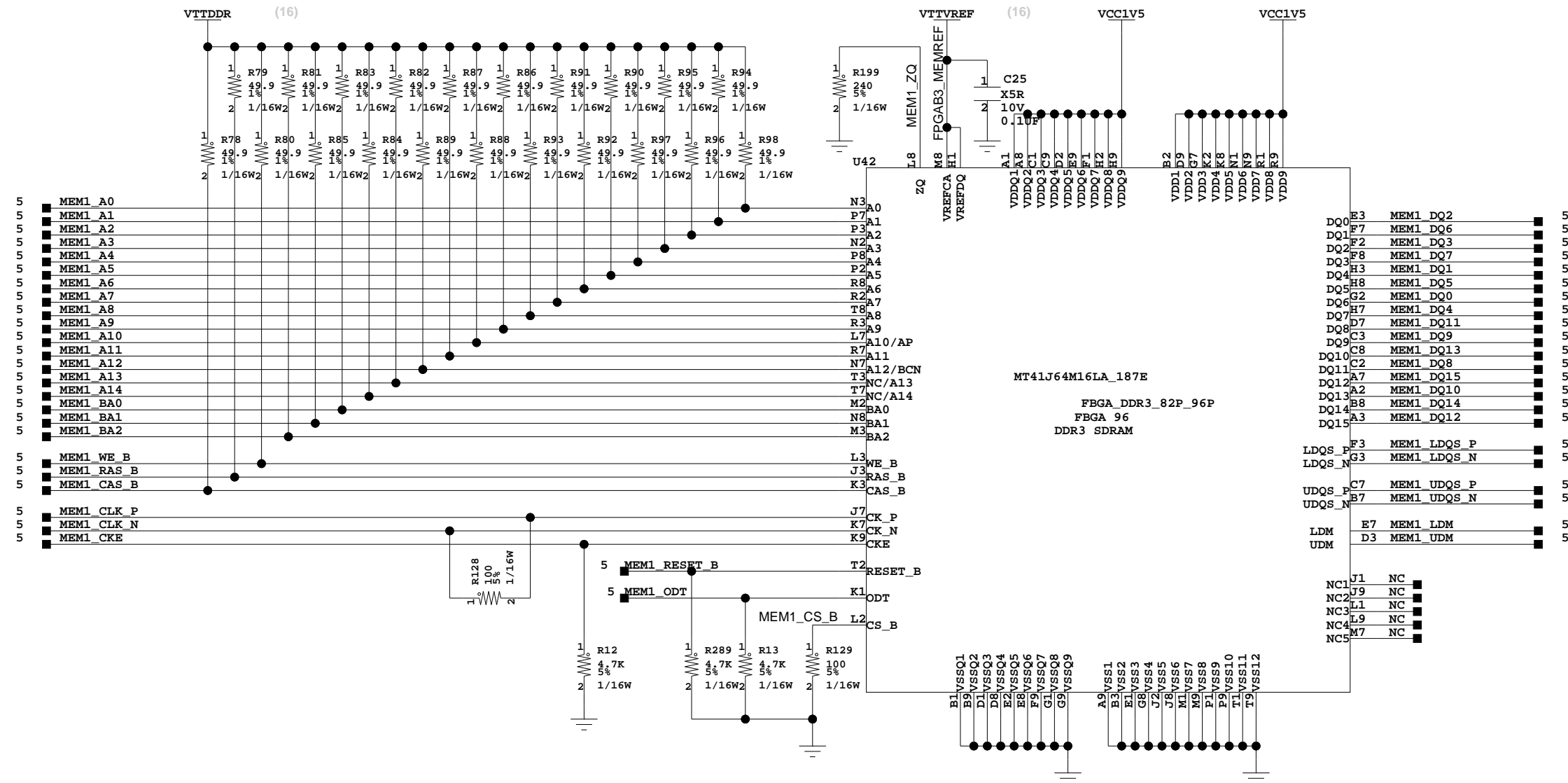


FPGA Decoupling



Title: FPGA Decoupling SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM
 PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

Date:	9-24-2009_15:46	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	8 of 35	Drawn By	BF



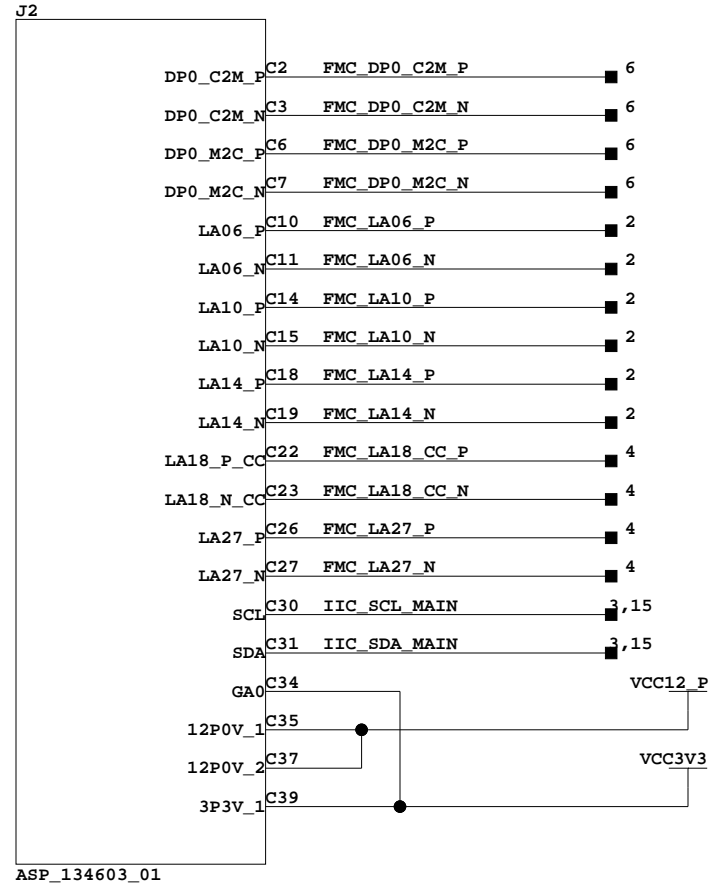
VCCOB3 remote sense pair connects from here back to (10)

DDR3

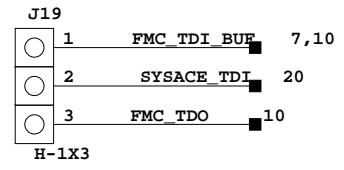


Title:	DDR3 SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
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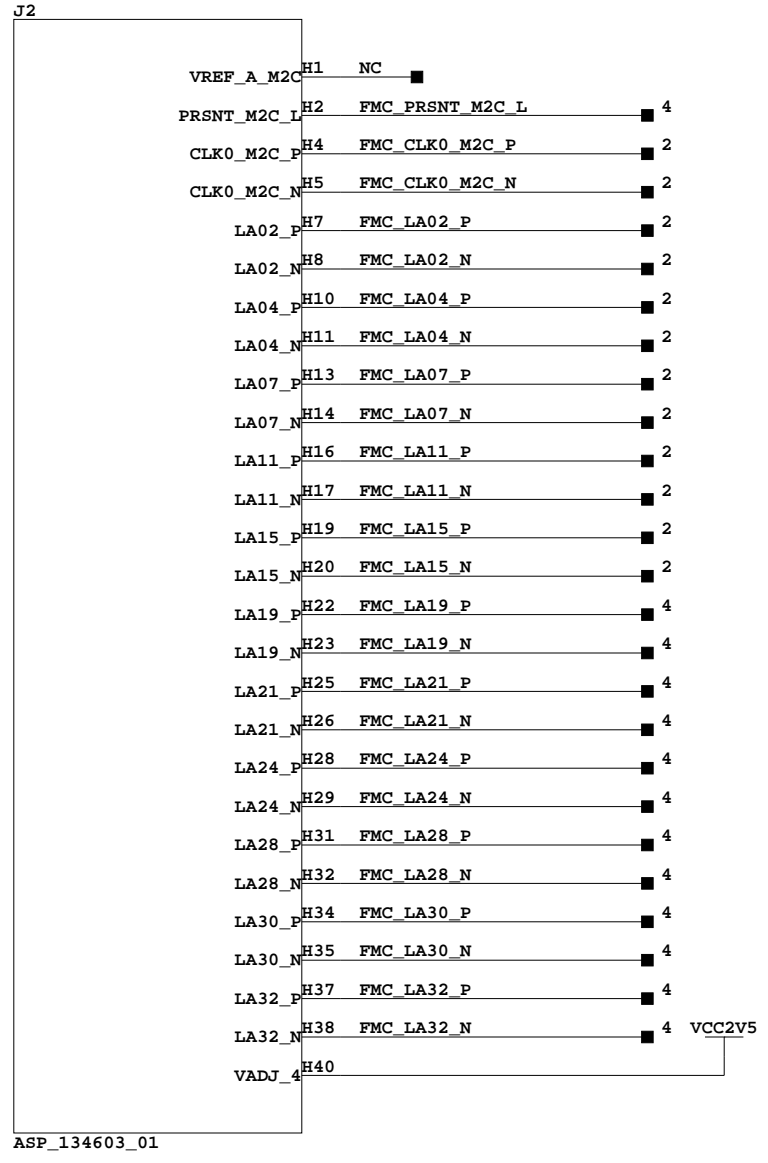
Date:	9-24-2009_15:00	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	9 of 35	Drawn By	BF



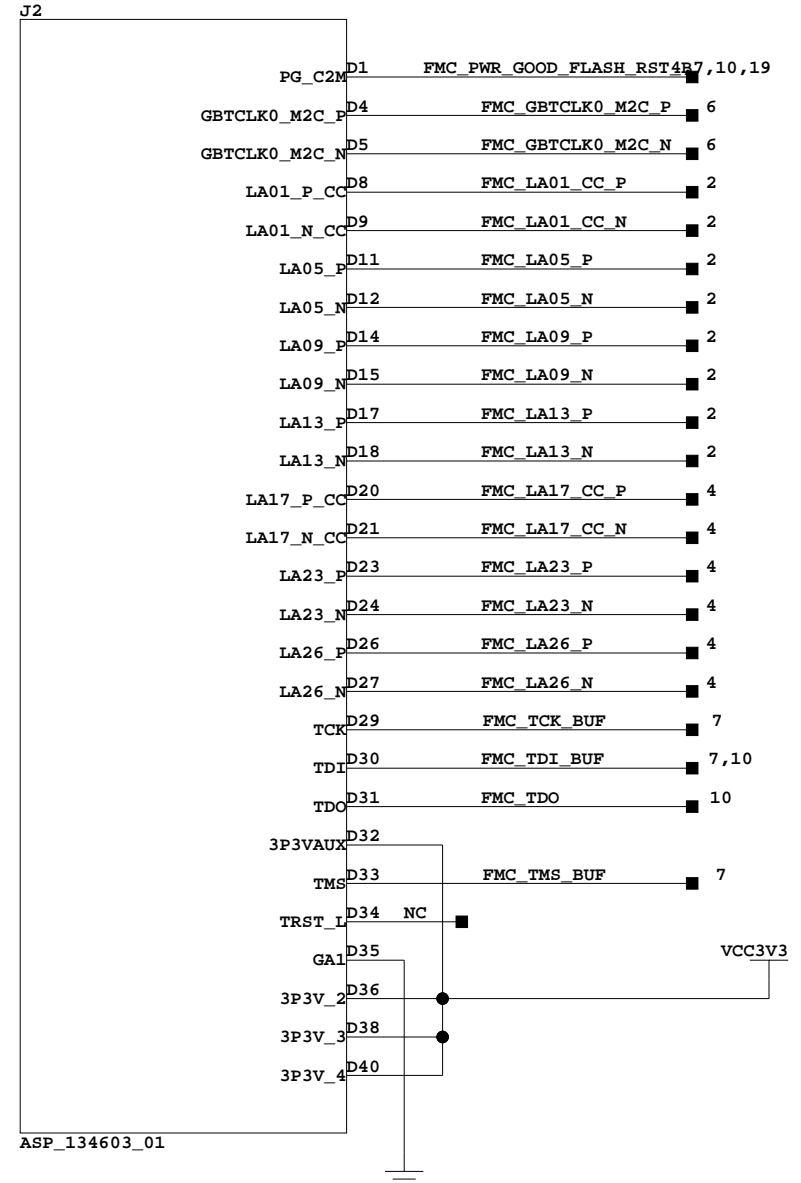
ASP_134603_01



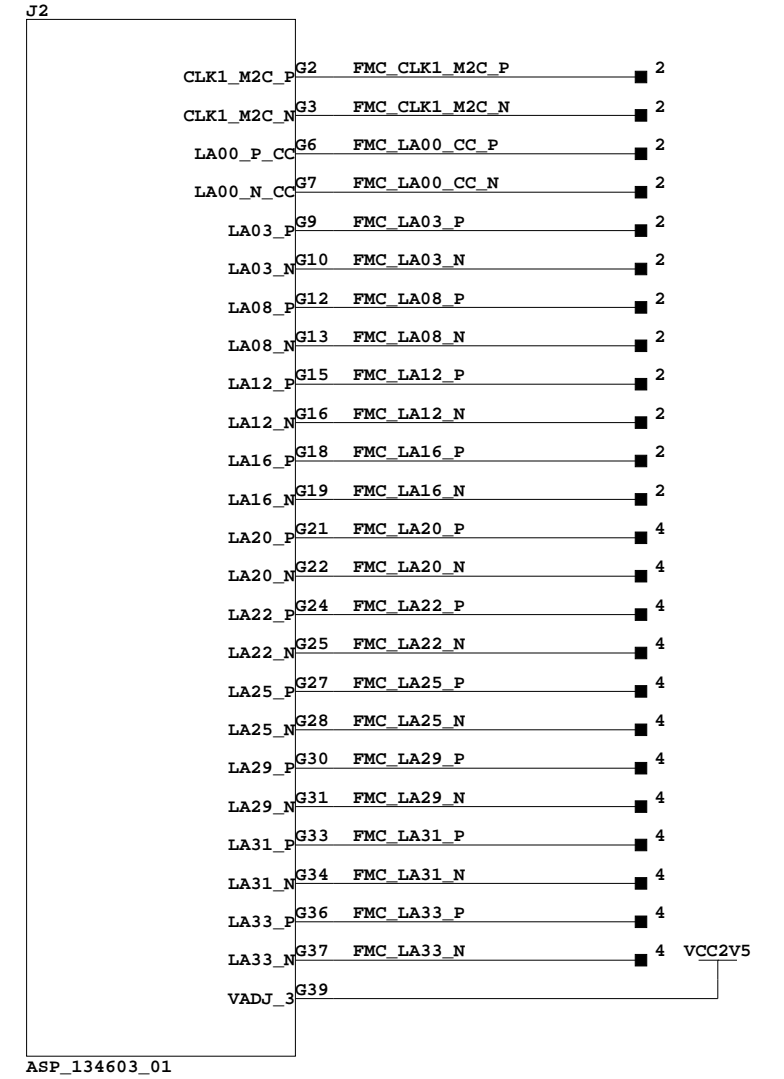
Jumper to include FMC in JTAG chain



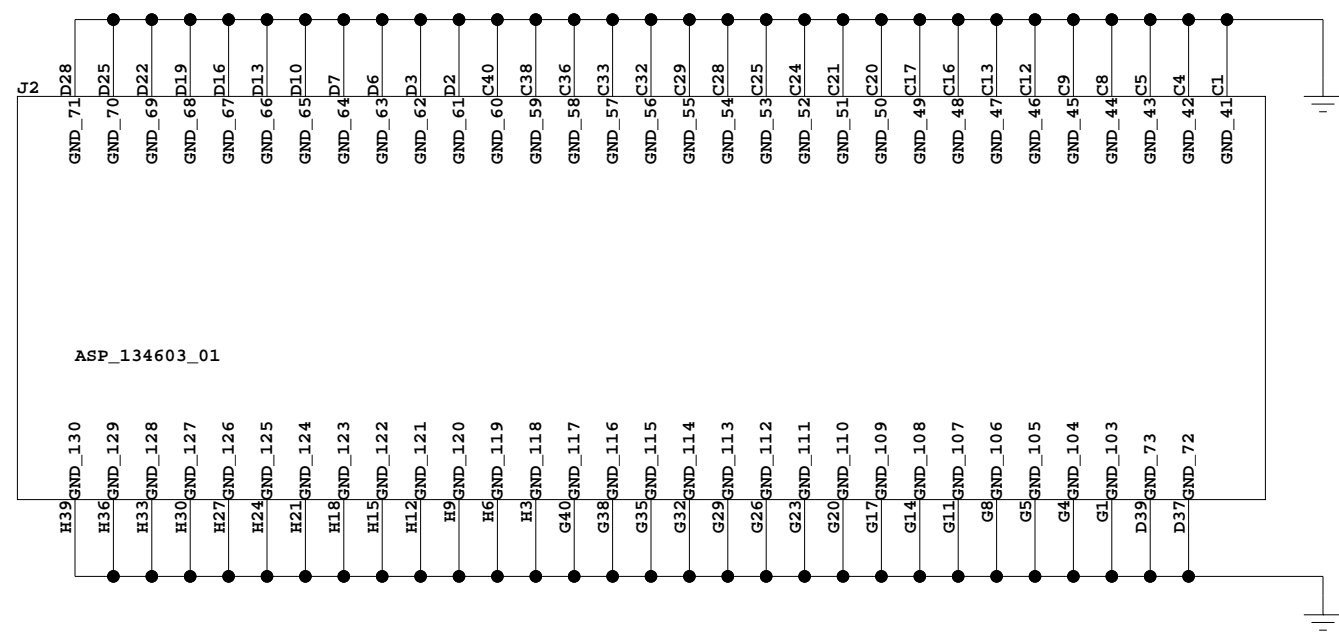
ASP_134603_01



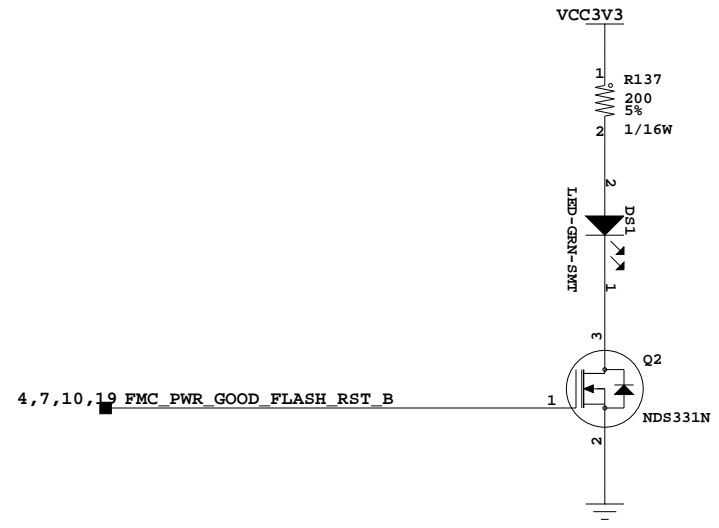
ASP_134603_01



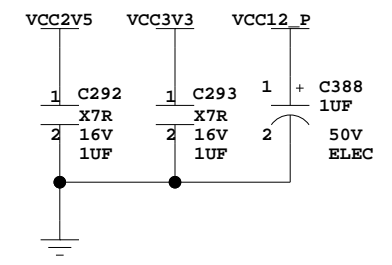
ASP_134603_01



ASP_134603_01



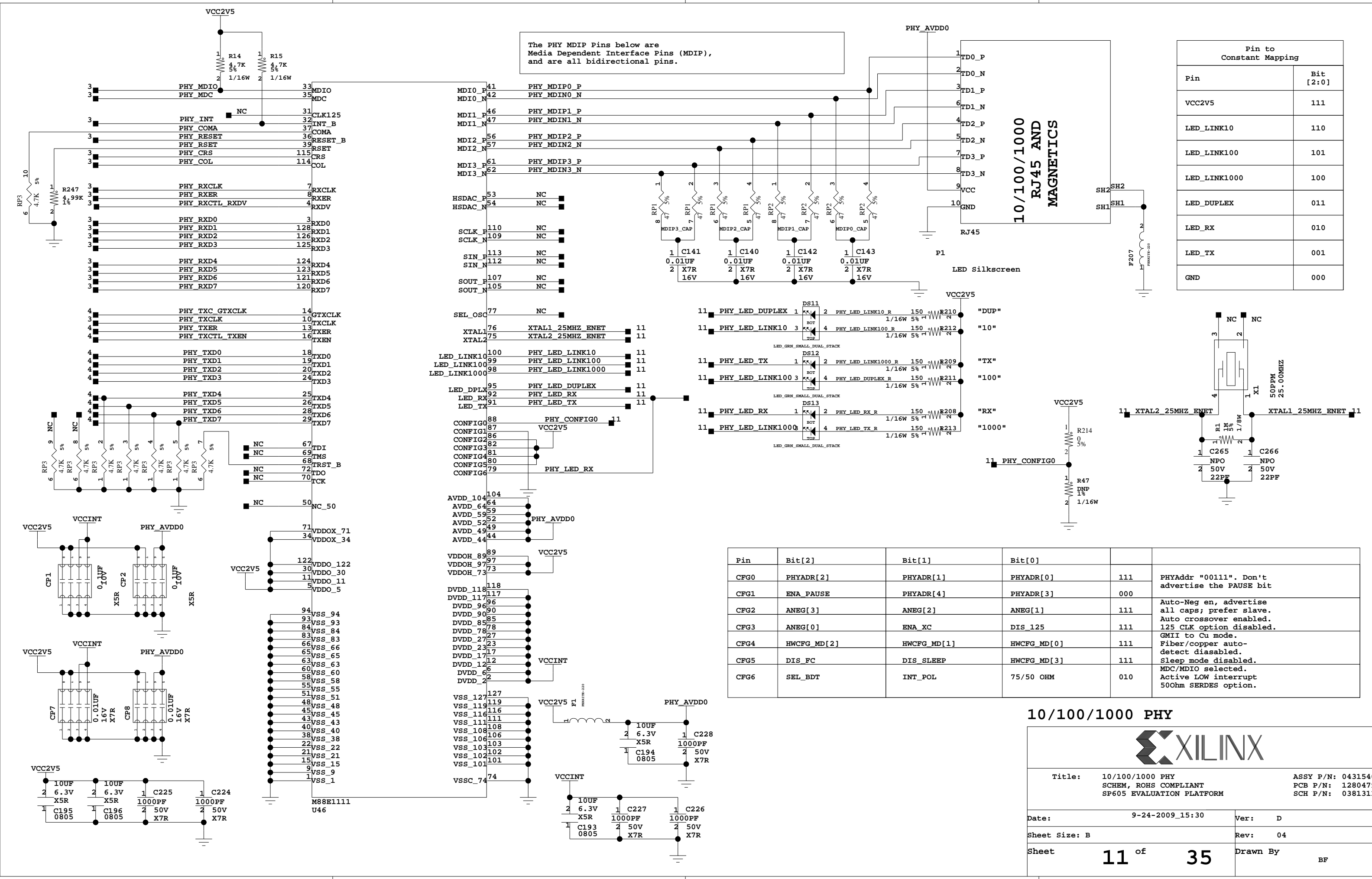
FMC Power Good LED



ANSI/VITA 57.1-2008 Version 1.1 FMC LPC Connector



Title: FMC LPC Connector SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
Date: 9-25-2009_10:32	Ver: D	
Sheet Size: B	Rev: 04	
Sheet 10 of 35	Drawn By BF	



10/100/1000 PHY

Title: 10/100/1000 PHY SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM

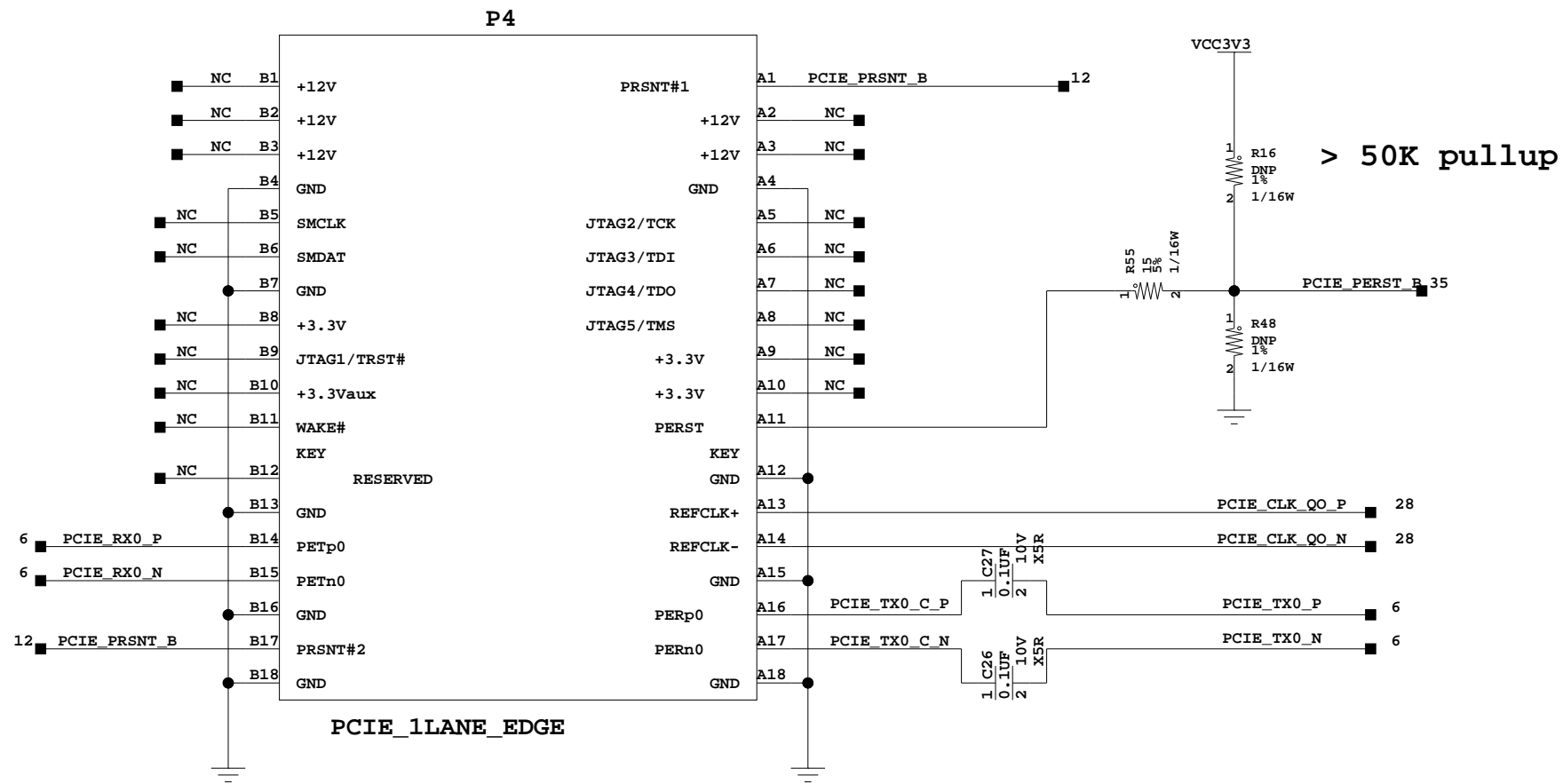
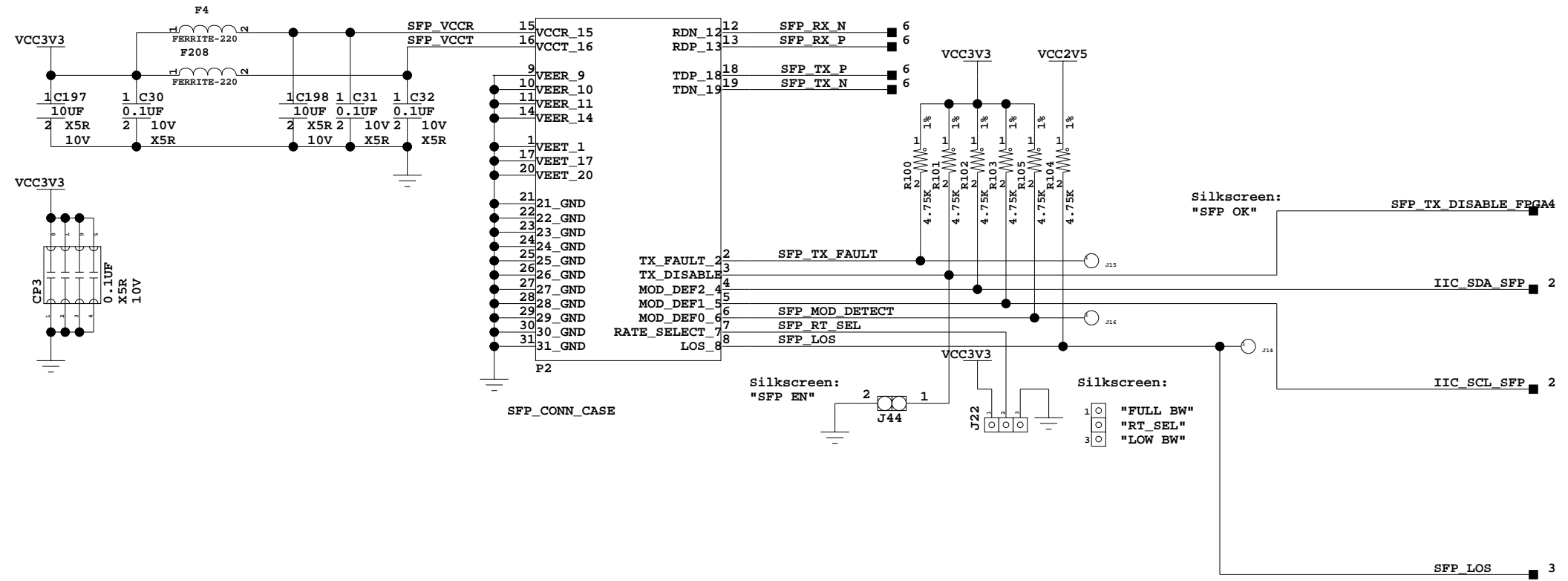
ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Date: 9-24-2009_15:30 Ver: D

Sheet Size: B Rev: 04

Sheet **11** of **35** Drawn By **BF**

SFP MODULE

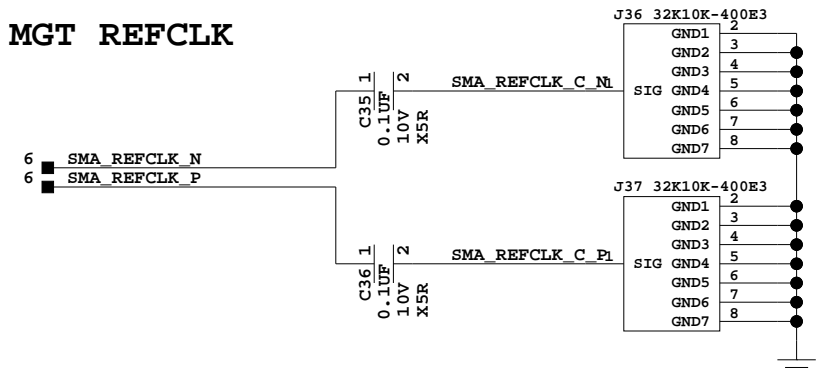


PCIE 1X Card Edge, SFP

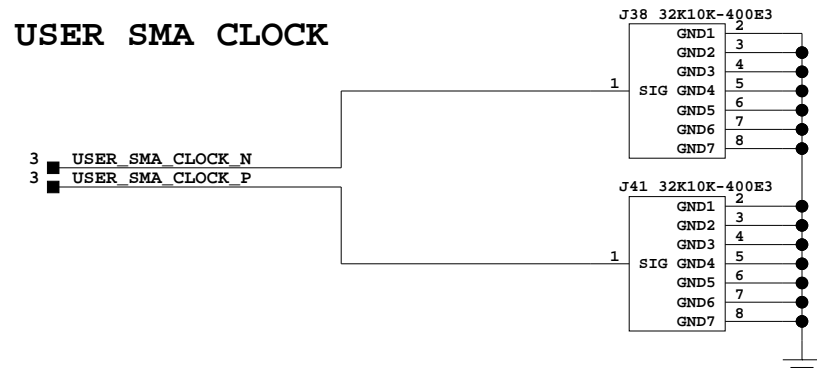


Title: PCIe 1X Card Edge, SFP SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
Date: 9-24-2009_15:00	Ver: D	
Sheet Size: B	Rev: 04	
Sheet 12 of 35	Drawn By BF	

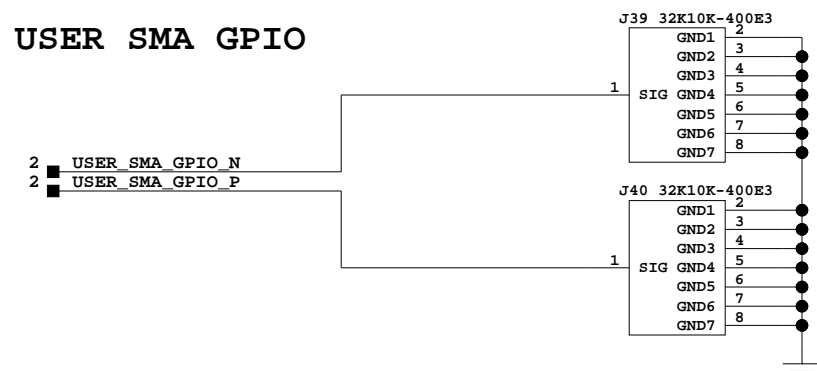
MGT REFCLK



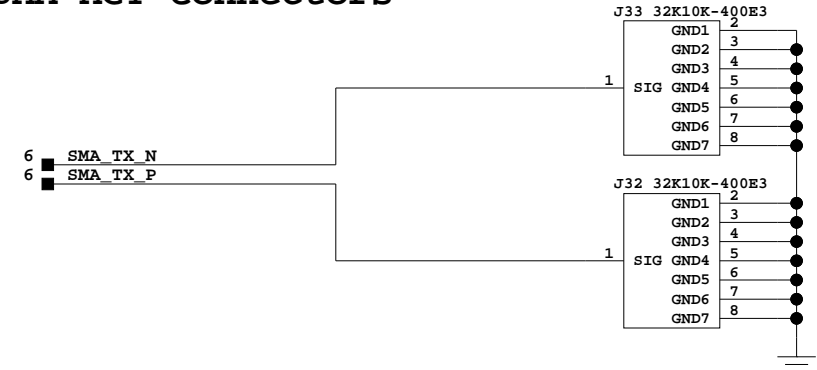
USER SMA CLOCK



USER SMA GPIO



SMA MGT Connectors



SMA Connectors

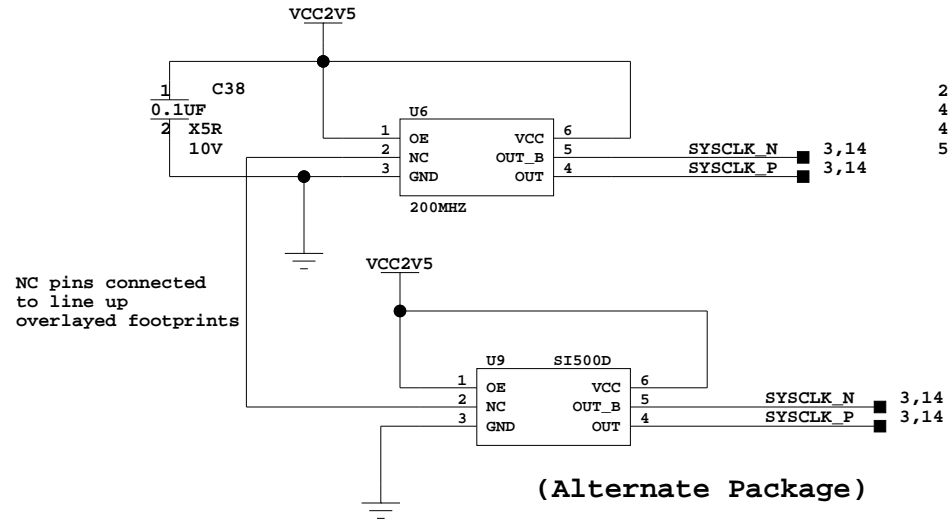


Title: SMA Connectors SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
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Date: 9-18-2009_15:04	Ver: D
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Sheet Size: B	Rev: 04
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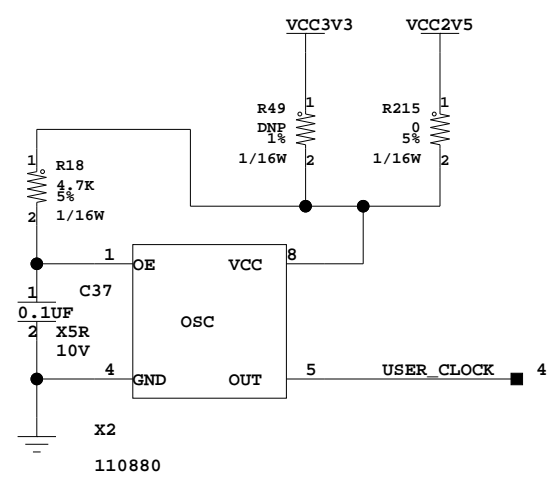
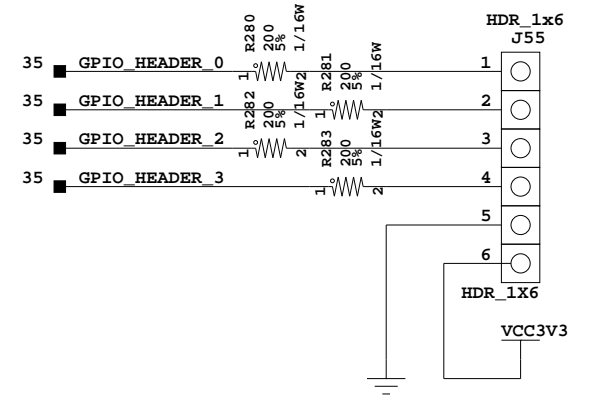
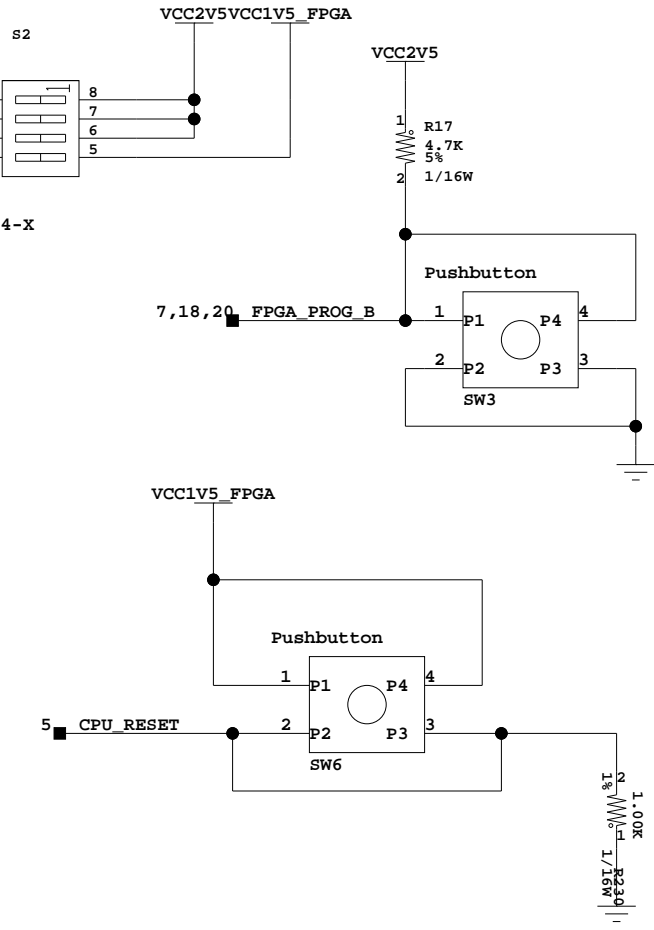
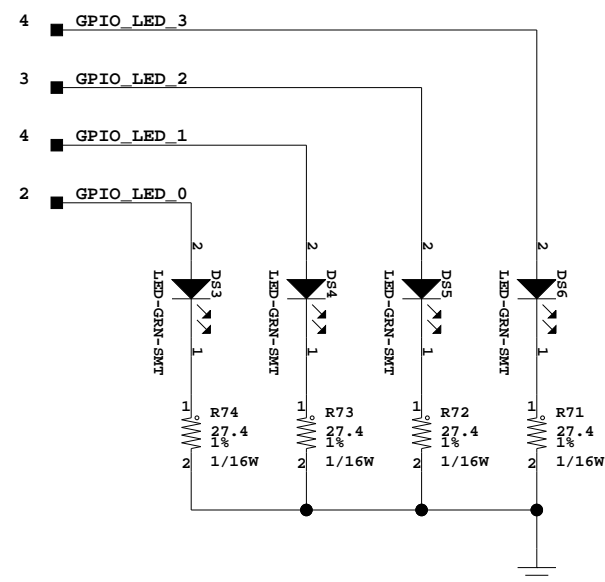
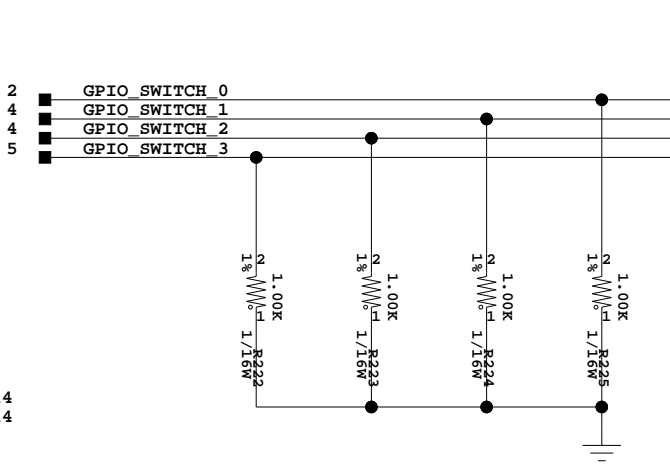
Sheet 13 of 35	Drawn By BF
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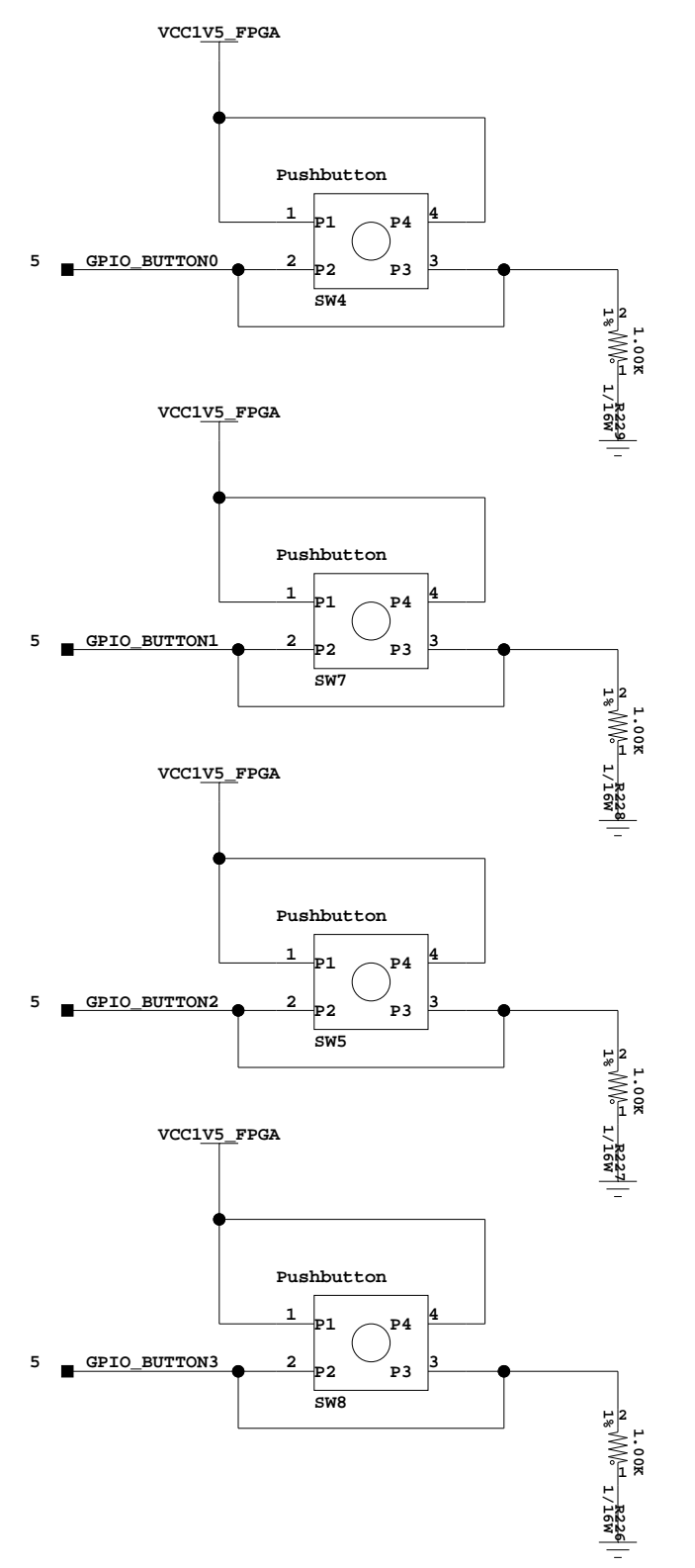
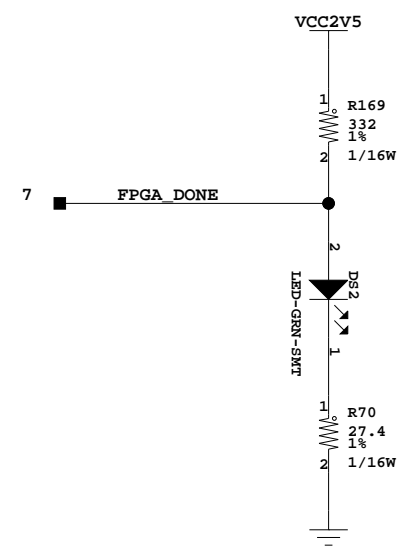
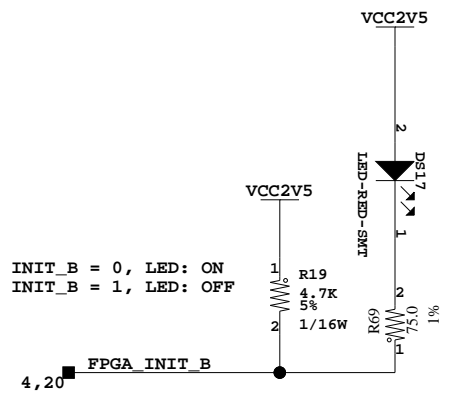
(Alternate Package)

Differential System Clock

NC pins connected to line up overlaid footprints



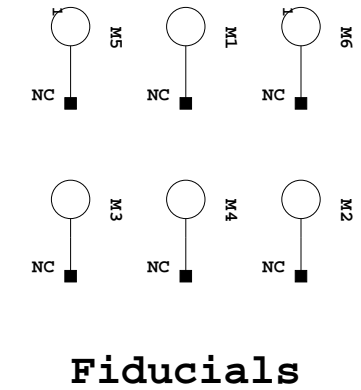
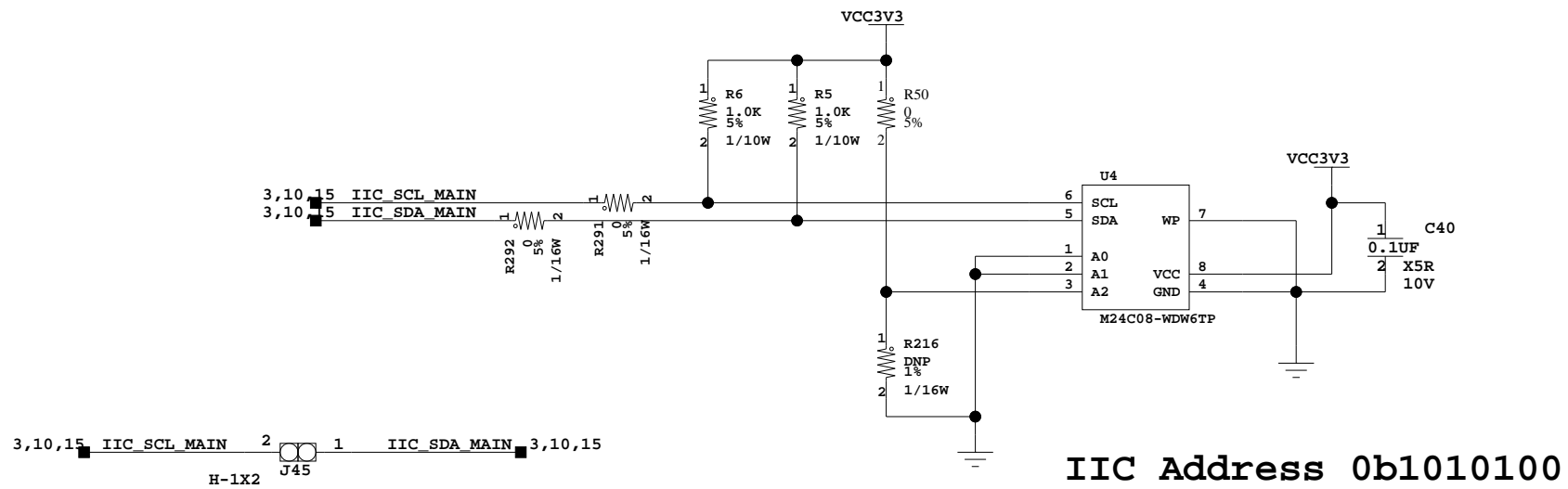
Single Ended User Clock



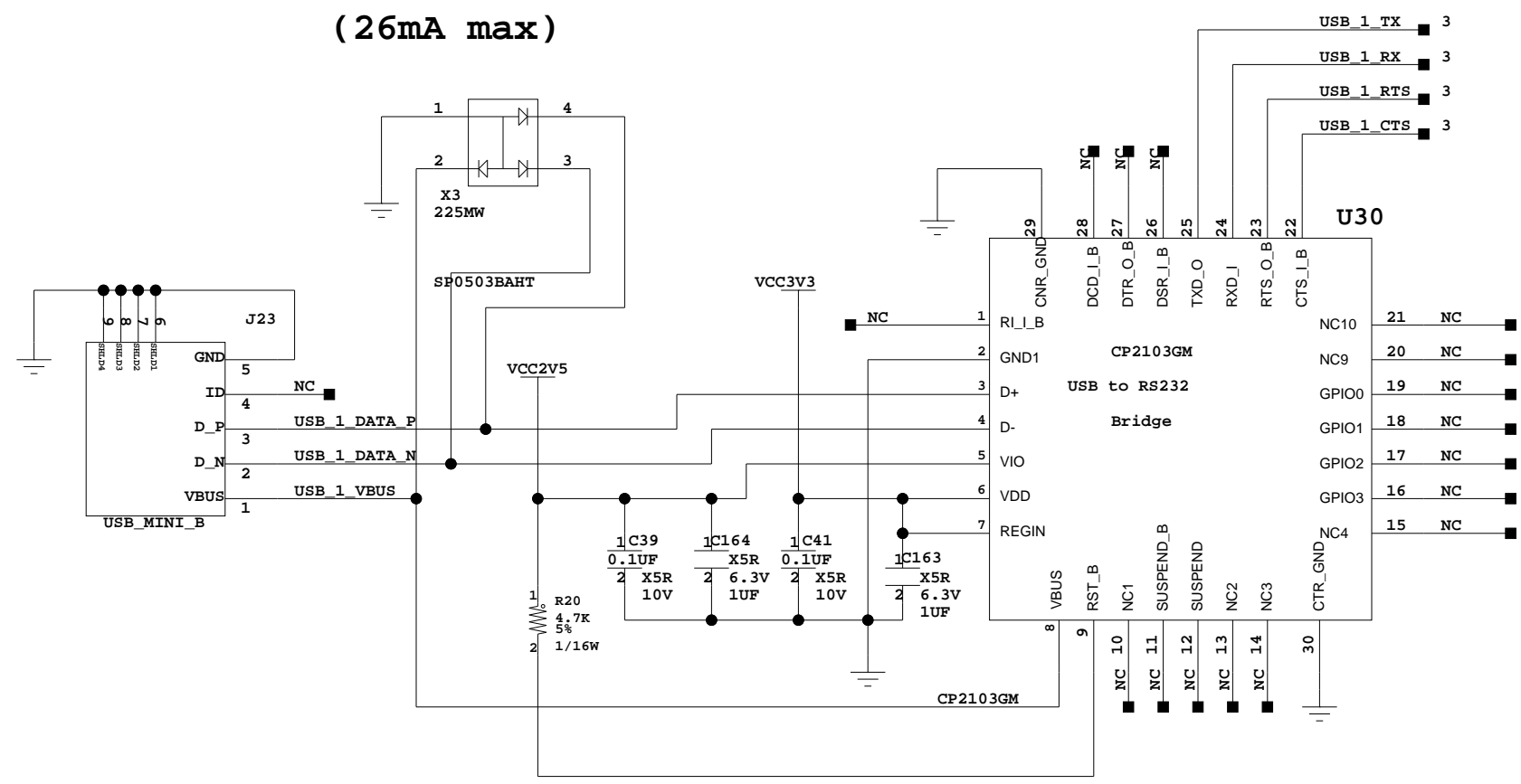
Clocks, LEDs, Buttons, Switches



Title: Clocks, LEDs, Buttons, Switches		PCB P/N: 0431534
SCHEM, ROHS COMPLIANT		SCH P/N: 0381305
SP605 EVALUATION PLATFORM		Test P/N: TSS0123
		ART P/N: 1280473
Date: 3-17-2010_9:23	Ver: D	
Sheet Size: B	Rev: 04	
Sheet 14 of 35	Drawn By	BF

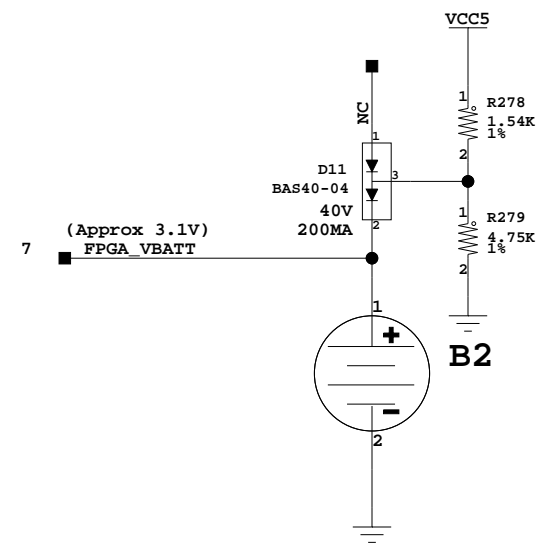


**CP2103 USB Self-Powered
(26mA max)**



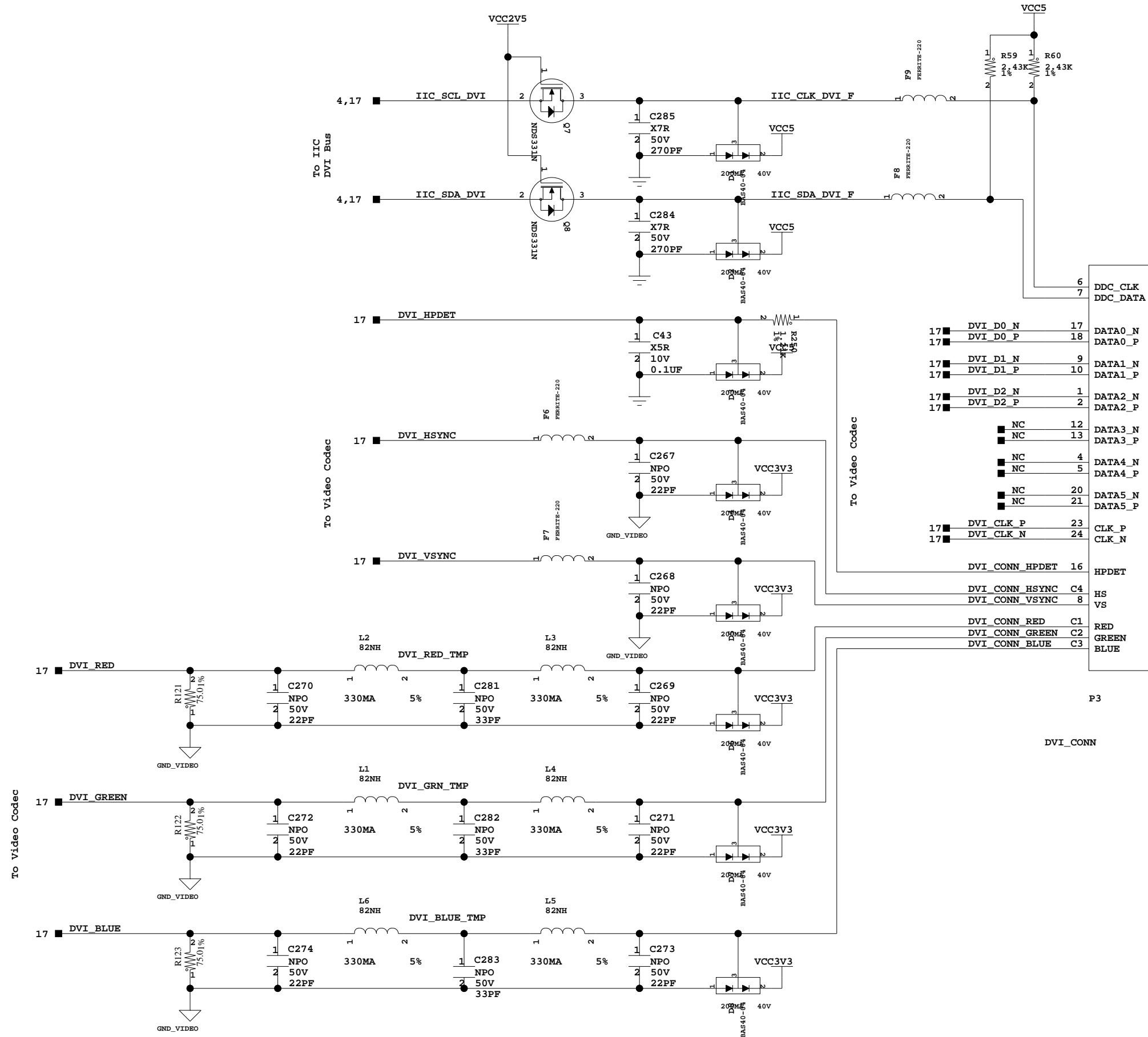
The VIO voltage must match the appropriate bank IO voltage

**Rechargeable
Battery**



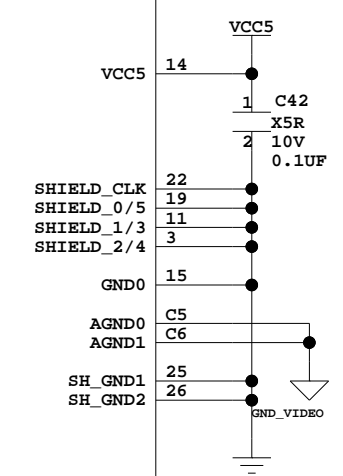
UART, IIC Header/EEPROM

Title: UART, IIC Header/EEPROM SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	
PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473	
Date: 9-24-2009_15:00	Ver: D
Sheet Size: B	Rev: 04
Sheet 15 of 35	Drawn By BF



DVI_CONN

6	DDC_CLK	17	DATA0_N
7	DDC_DATA	18	DATA0_P
17	DVI_D0_N	17	DATA1_N
17	DVI_D0_P	18	DATA1_P
17	DVI_D1_N	9	DATA2_N
17	DVI_D1_P	10	DATA2_P
17	DVI_D2_N	1	DATA3_N
17	DVI_D2_P	2	DATA3_P
	NC	12	DATA4_N
	NC	13	DATA4_P
	NC	4	DATA5_N
	NC	5	DATA5_P
17	DVI_CLK_P	23	CLK_P
17	DVI_CLK_N	24	CLK_N
	DVI_CONN_HPDET	16	HPDET
	DVI_CONN_HSYNC	C4	HS
	DVI_CONN_VSYNC	8	VS
	DVI_CONN_RED	C1	RED
	DVI_CONN_GREEN	C2	GREEN
	DVI_CONN_BLUE	C3	BLUE

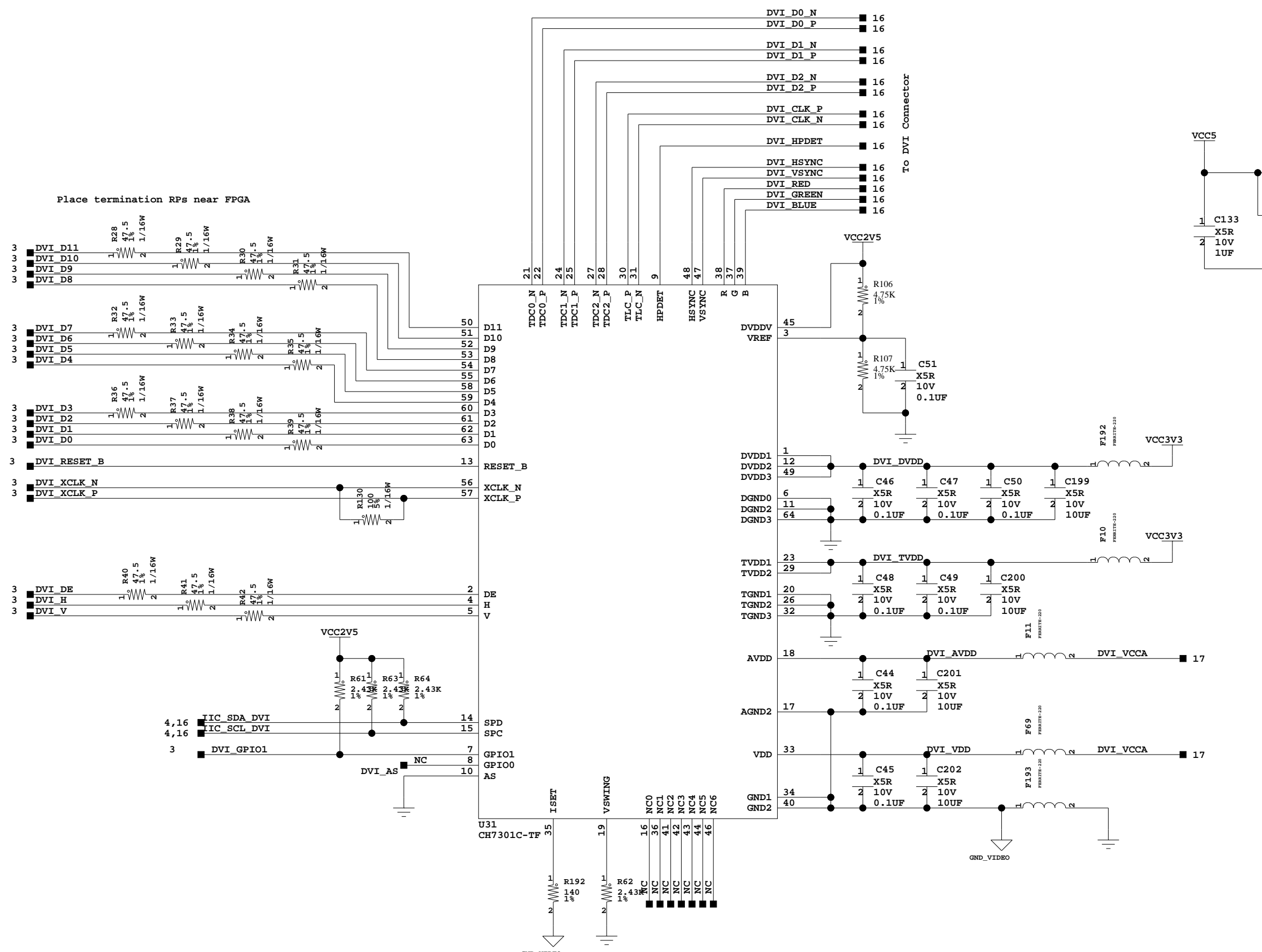


DVI VIDEO CONNECTOR



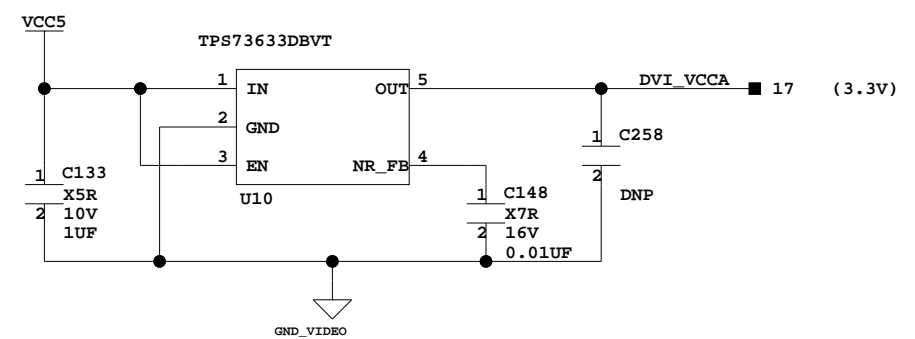
Title: DVI VIDEO CONNECTOR SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM
 PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

Date:	9-18-2009_15:03	Ver:	D
Sheet Size:	B	Rev:	04
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Place termination RPs near FPGA

Near DVI IC



IIC Address = 0x76

DVI CODEC

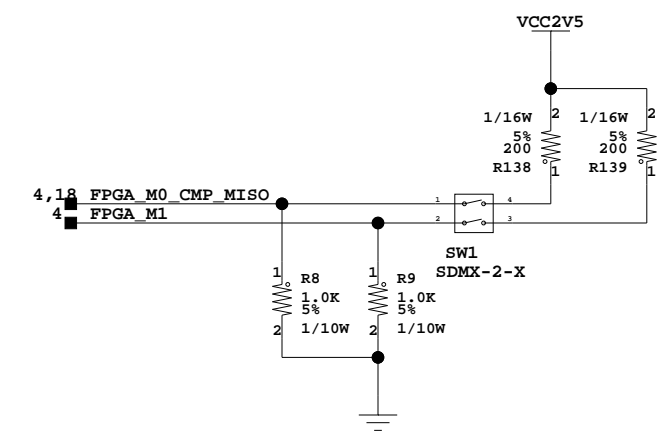
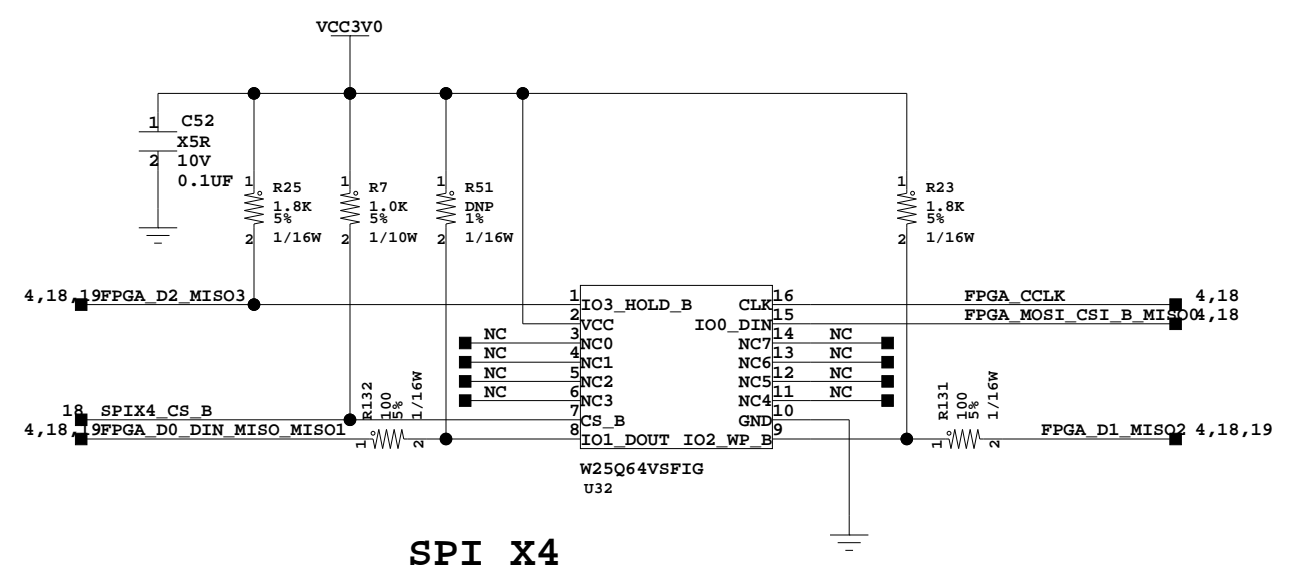
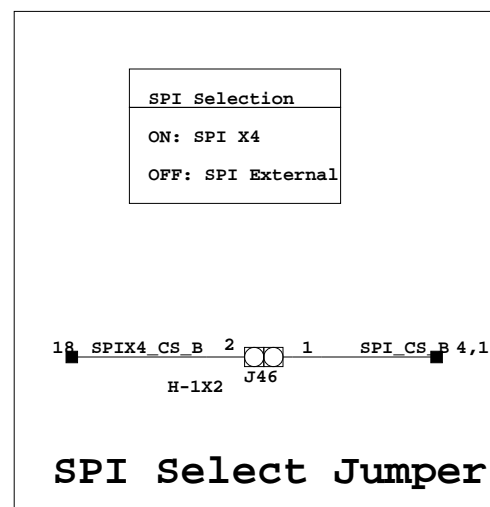


Title: DVI CODEC SCHEM, ROHS COMPLIANT, SP605 EVALUATION PLATFORM
 PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

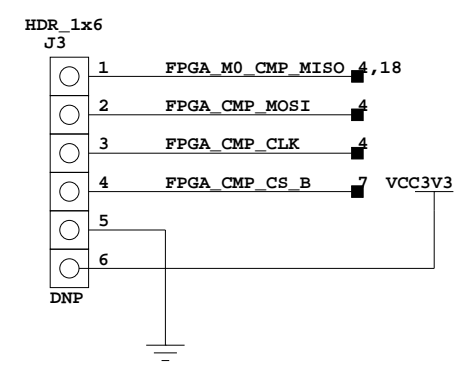
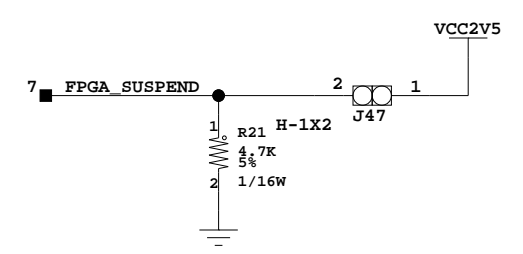
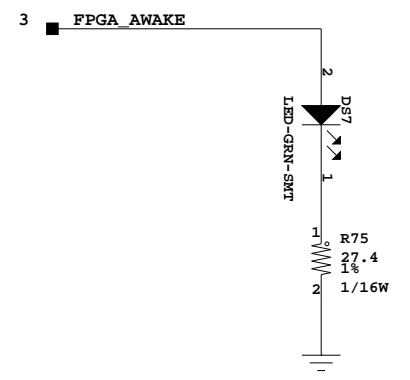
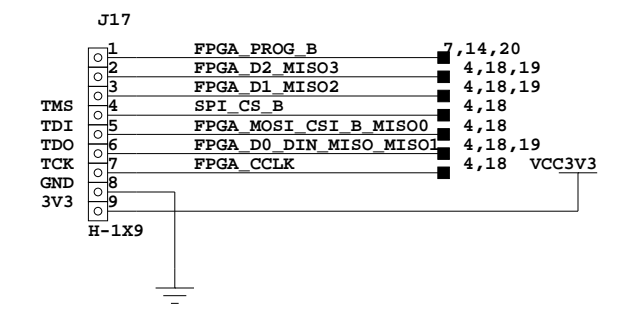
Date: 9-18-2009_15:03 Ver: D

Sheet Size: B Rev: 04

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Silkscreen:



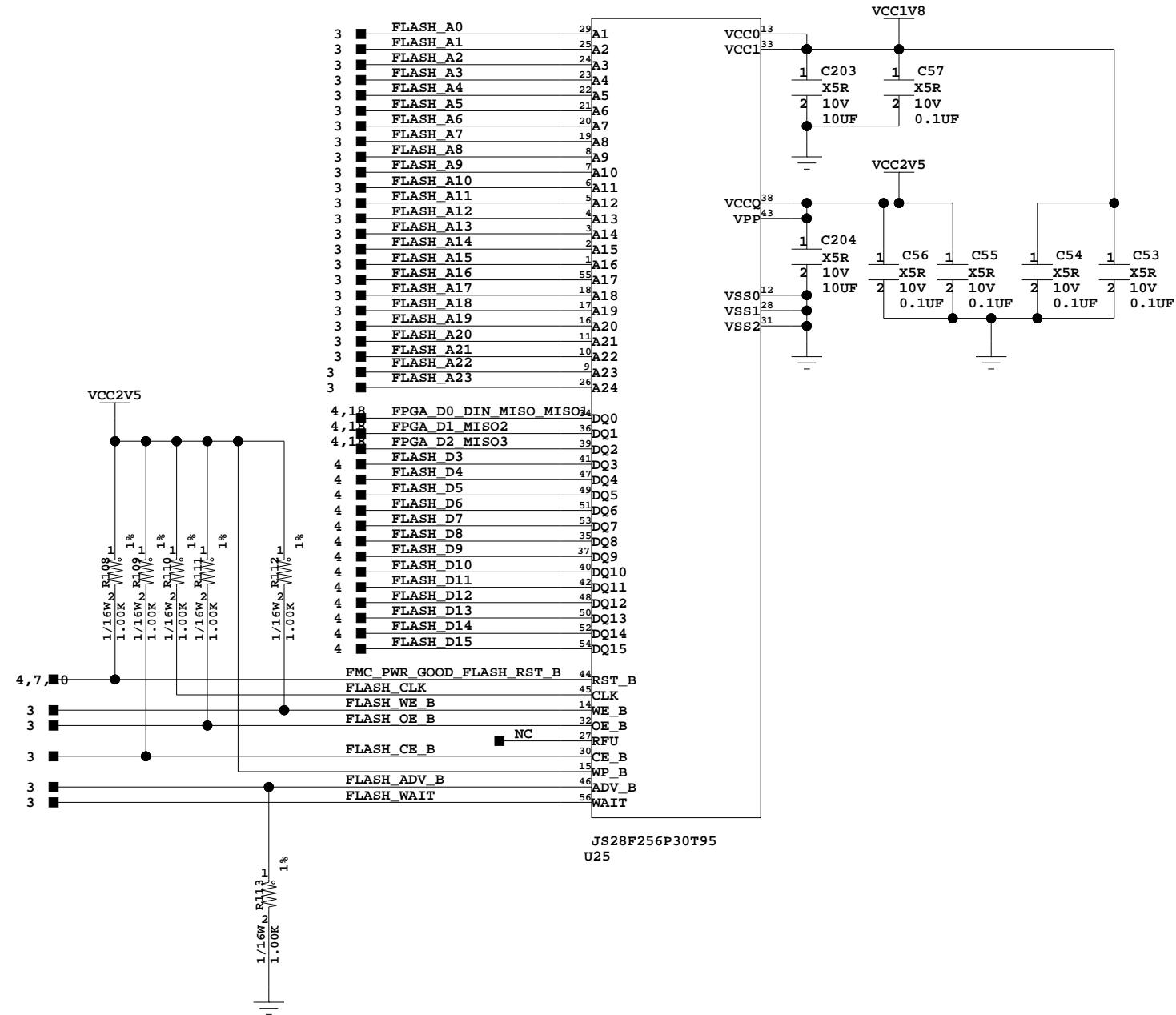
SPI, CMP, Mode, and Suspend



Title:	SPI, CMP, Mode, and Suspend SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N:	0431534
		SCH P/N:	0381305
		Test P/N:	TSS0123
		ART P/N:	1280473

Date:	9-24-2009_15:00	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	18 of 35	Drawn By	BF

Silkscreen:
 "Strata FLASH"
 "256 MBit"



Synchronous mode
 not supported

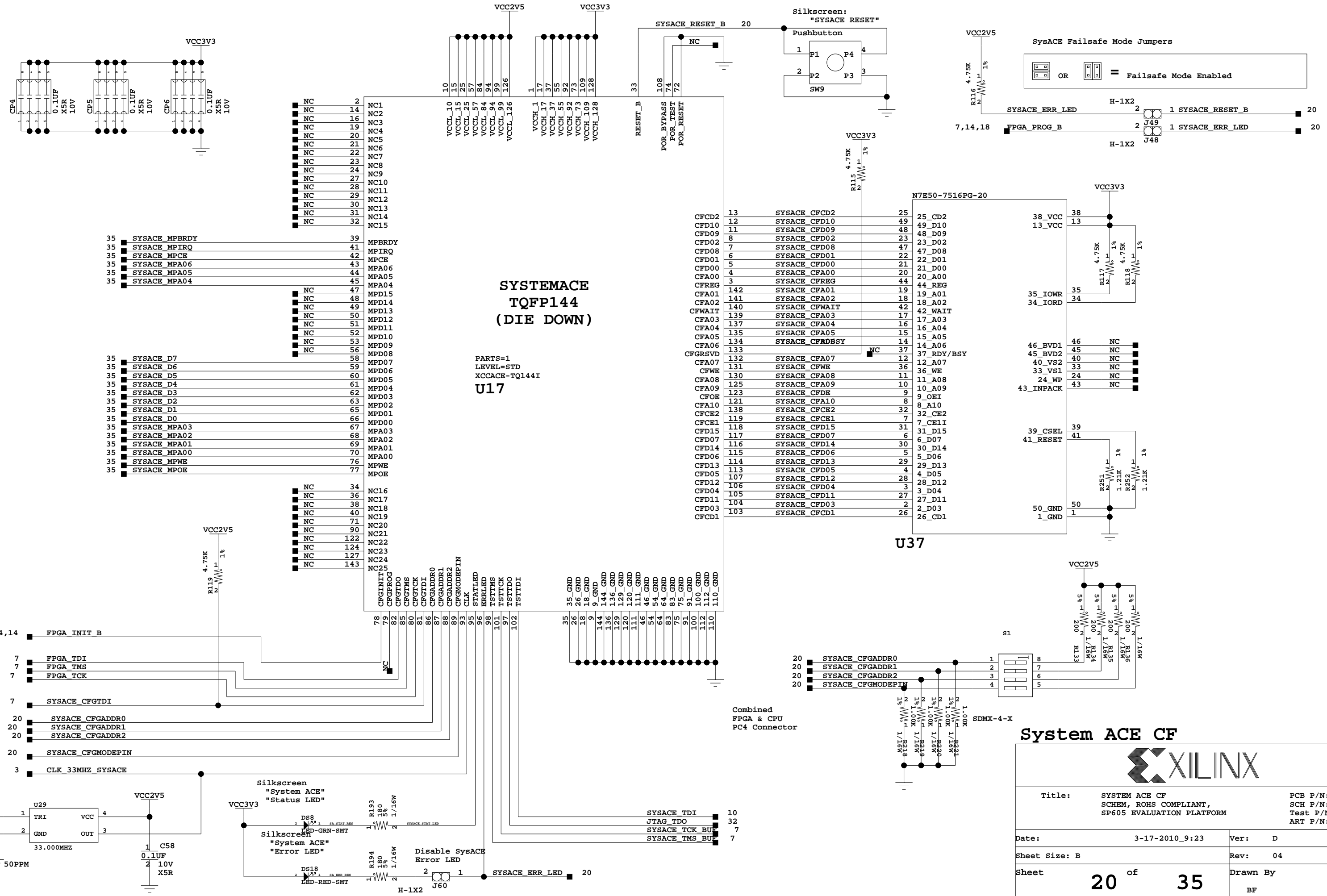
ASYNCR. SRAM FLASH

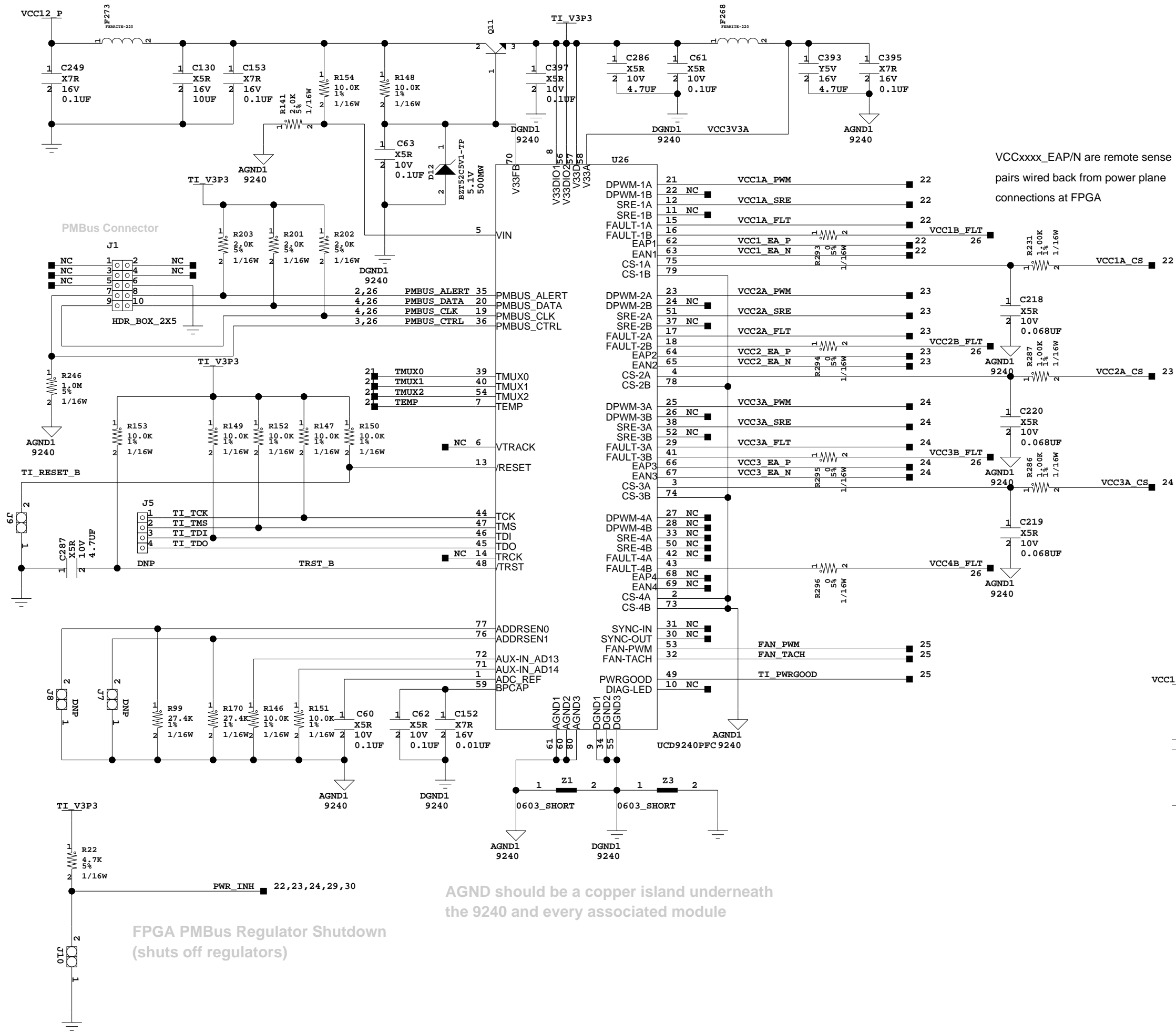


Title: ASYNCR. SRAM FLASH
 SCHEM, ROHS COMPLIANT
 SP605 EVALUATION PLATFORM

PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

Date:	9-18-2009_15:03	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	19 of 35	Drawn By	BF

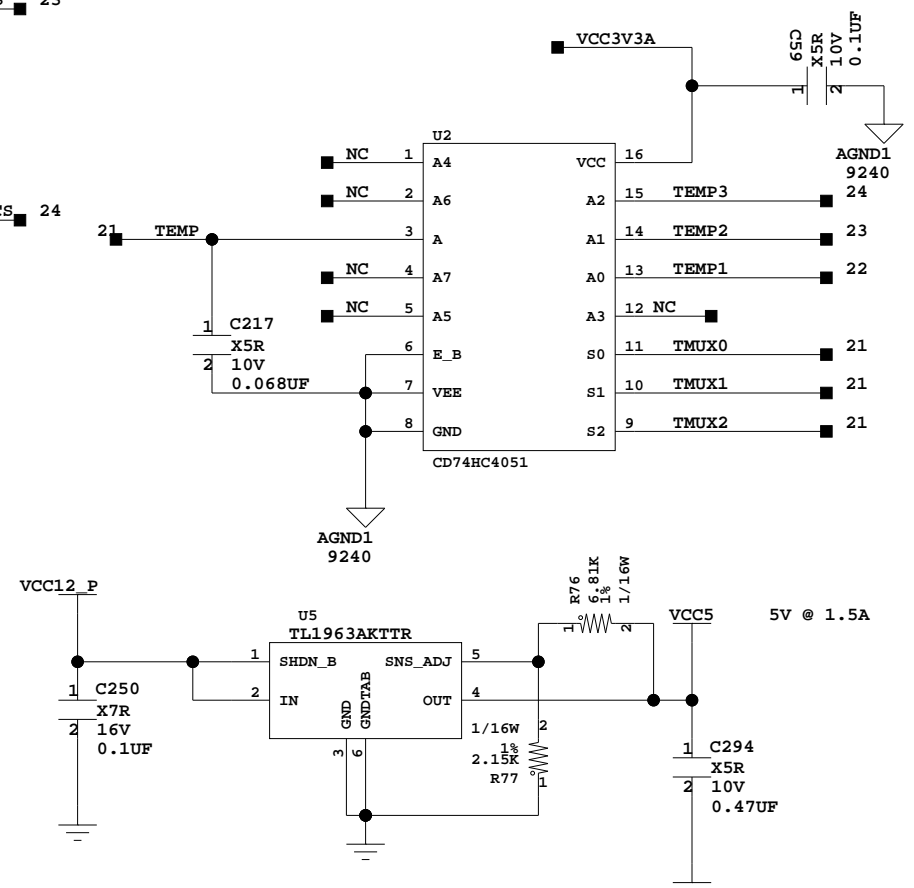




PMBus Address is calculated as follows:
 PMBus Address = 12 x Value(ADDRSEN1) + Value(ADDRSEN0)
 Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k
 PMBus Address = (12 x 4) + 4 = 52 decimal

ADDRSENx Value	RPMBus
Open	-
11	210k
10	158k
9	115k
8	84.5k
7	63.4k
6	47.5k
5	36.5k
4	27.4k
3	21.5k
2	16.9k
1	13.0k
0	10.2k
Short	-

Note:
 Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127



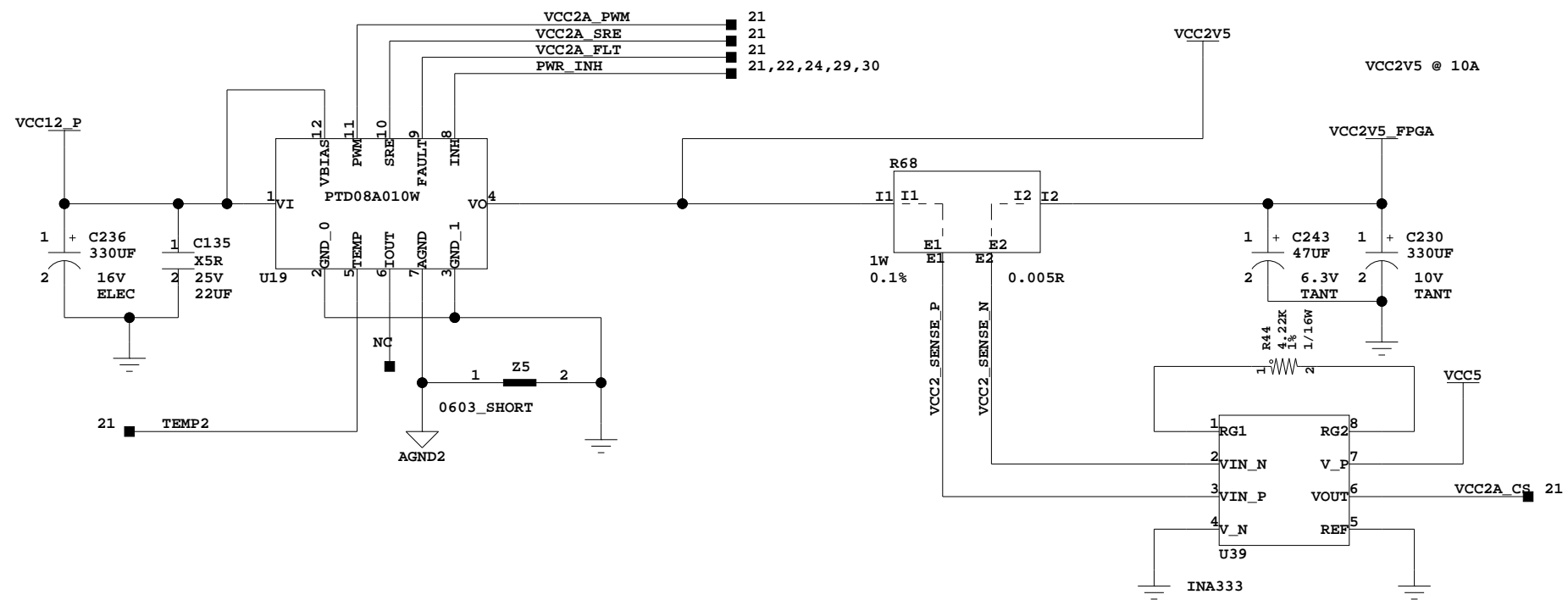
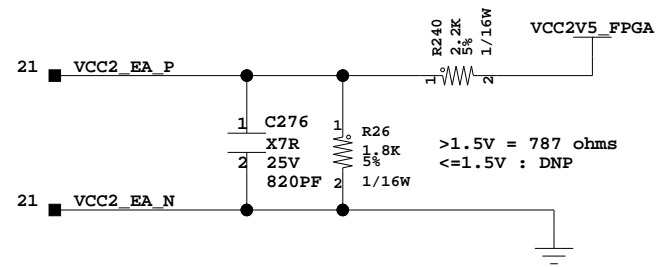
FPGA UCD9240 PMBus Controller



Title: TI UCD9240 Power System SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
Date: 9-24-2009_15:00	Ver: D	
Sheet Size: B	Rev: 04	
Sheet 21 of 35	Drawn By BF	

AGND should be a copper island underneath the 9240 and every associated module

FPGA PMBus Regulator Shutdown (shuts off regulators)



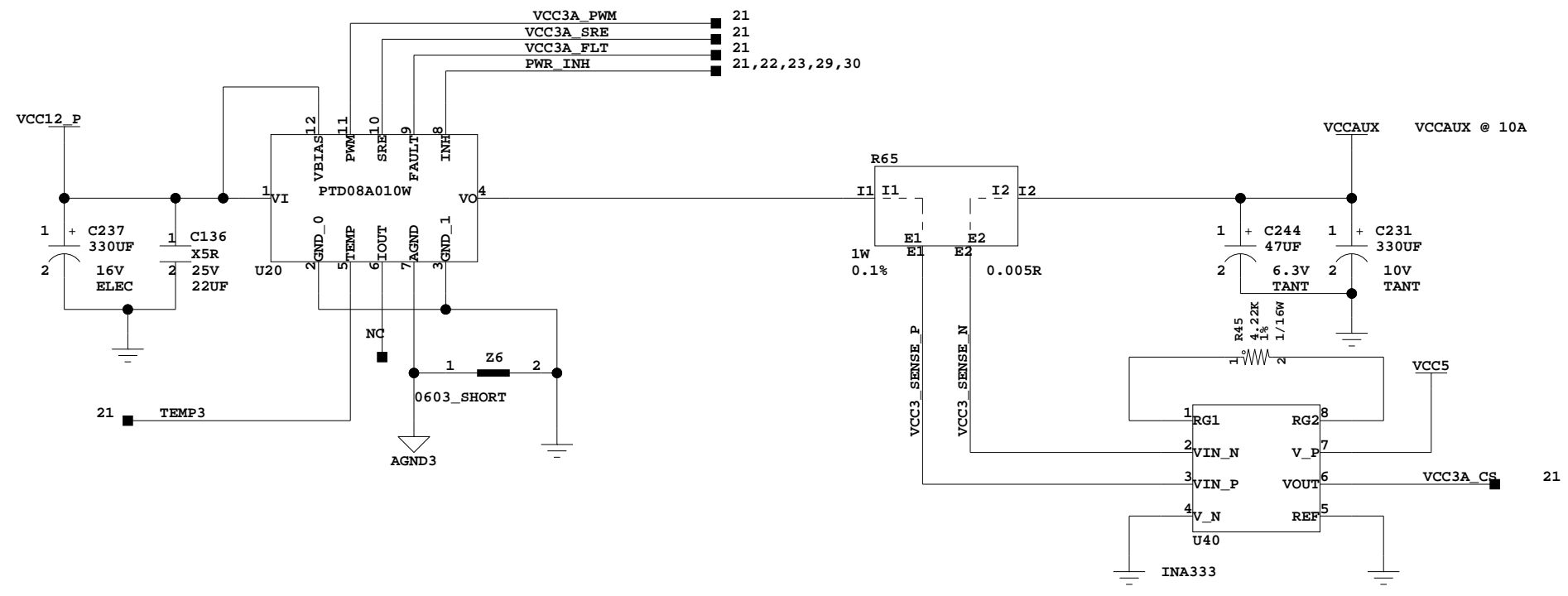
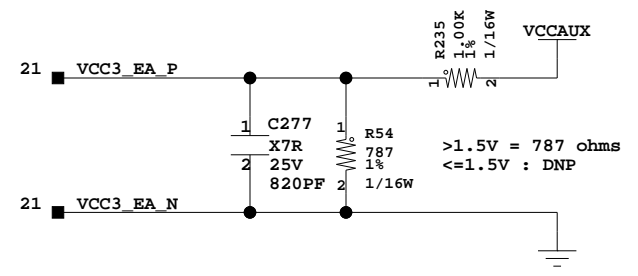
PTD08A010W 10A Max. Power Channel



Title: PTD08A010W 20A Max. Power Channel
 SCHEM, ROHS COMPLIANT
 SP605 EVALUATION PLATFORM

PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

Date:	9-18-2009_15:03	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	23 of 35	Drawn By	BF



PTD08A010W 10A Max. Power Channel



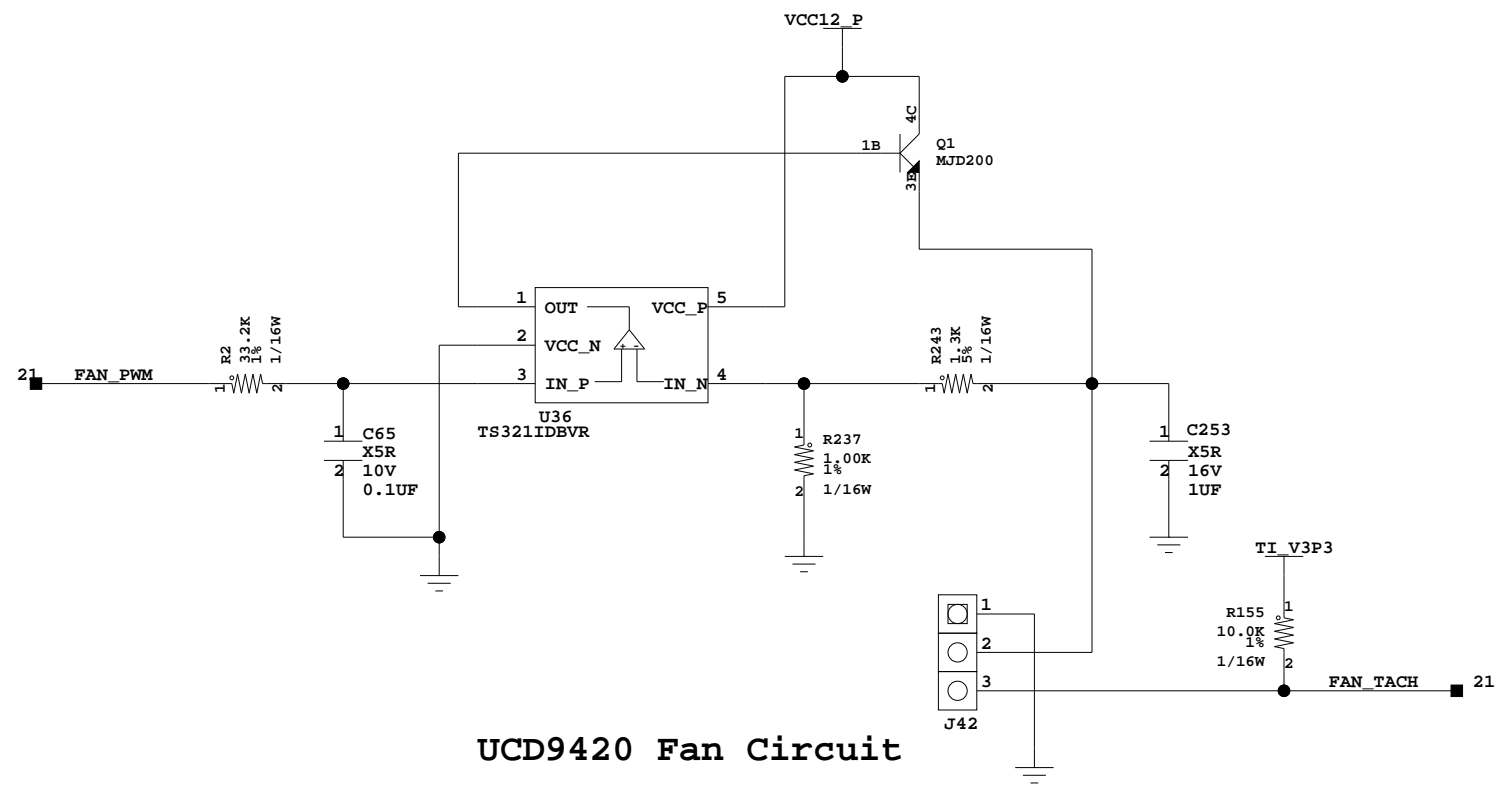
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 SCHEM, ROHS COMPLIANT
 SP605 EVALUATION PLATFORM

PCH P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

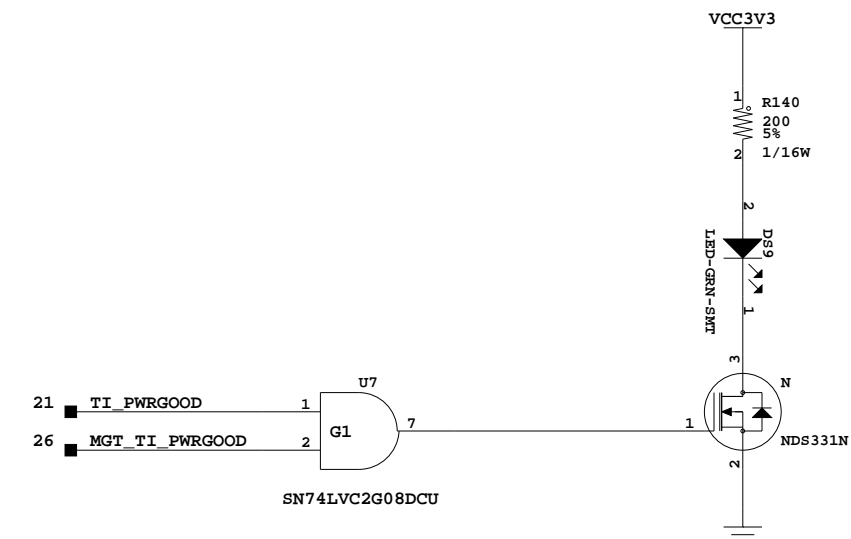
Date: 9-24-2009_15:00 Ver: D

Sheet Size: B Rev: 04

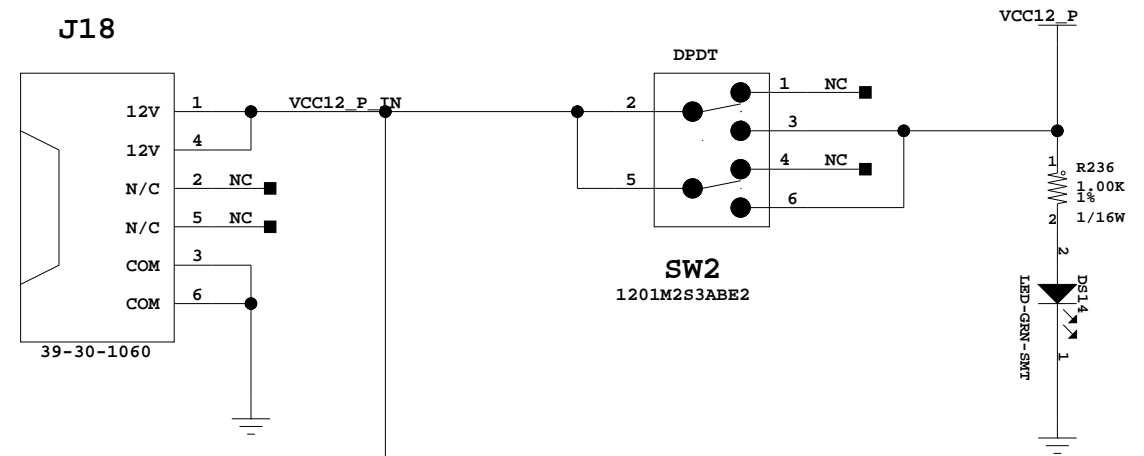
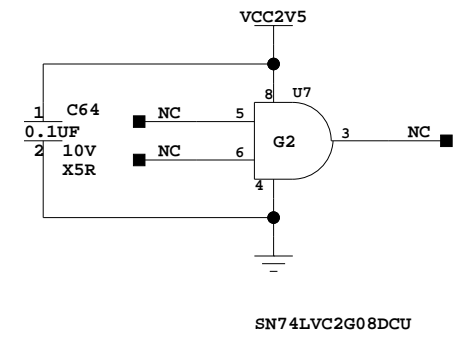
Sheet 24 of 35 Drawn By BF



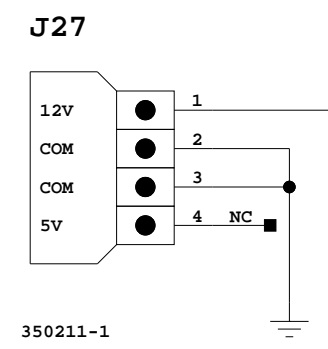
UCD9420 Fan Circuit



SP605 Power Good



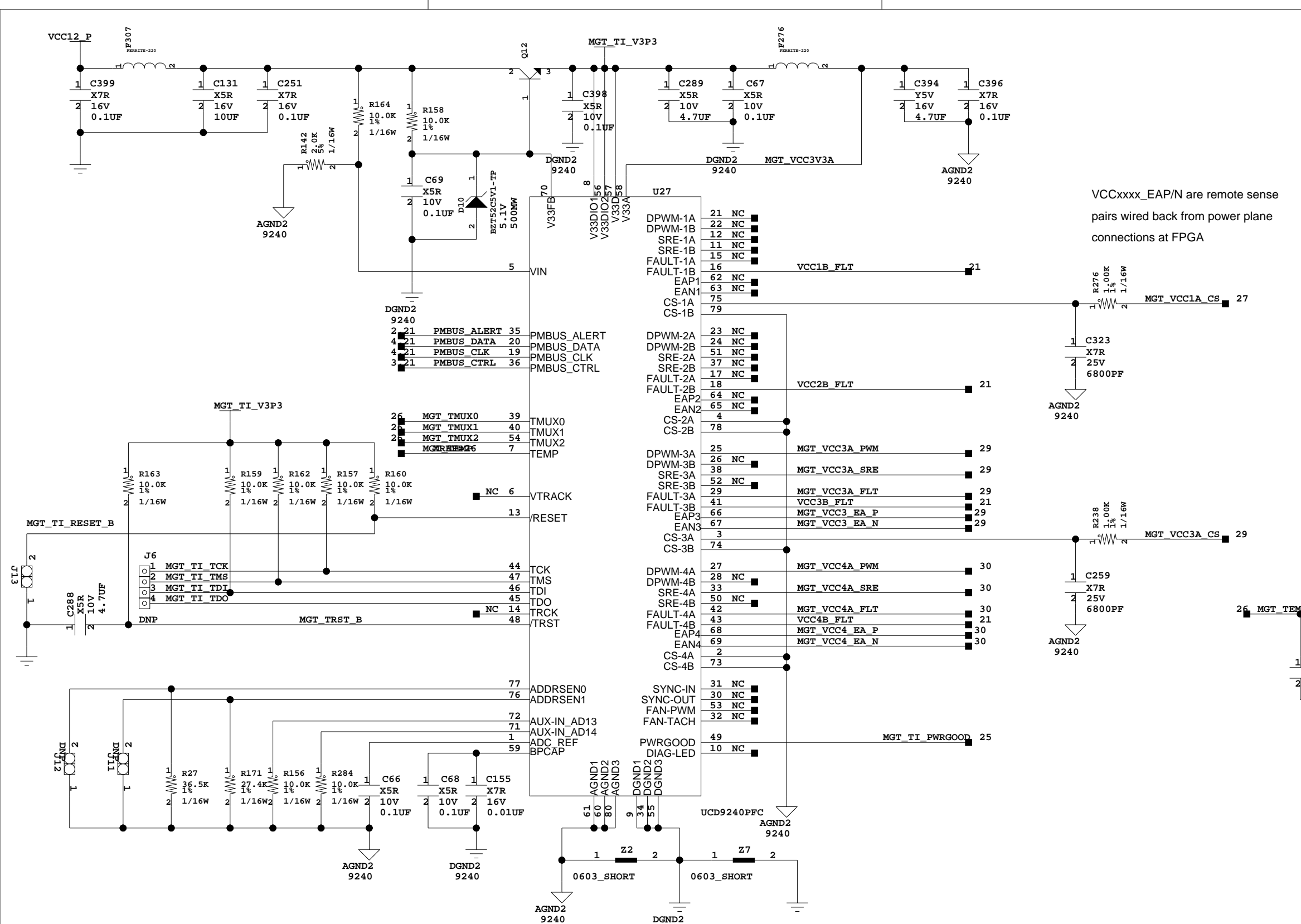
ATX Peripheral Cable



12V Power Jacks, 12V Fan



Title: TI UCD9240 Power System SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473	
Date: 9-24-2009_15:00	Ver: D		
Sheet Size: B	Rev: 04		
Sheet 25 of 35	Drawn By BF		



PMBus Address is calculated as follows:
 PMBus Address = 12 x Value(ADDRSEN1) + Value(ADDRSEN0)
 Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k
 PMBus Address = (12 x 4) + 4 = 52 decimal

ADDRSENx Value	RPMBus
Open	-
11	210k
10	158k
9	115k
8	84.5k
7	63.4k
6	47.5k
5	36.5k
4	27.4k
3	21.5k
2	16.9k
1	13.0k
0	10.2k
Short	-

Note:
 Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127

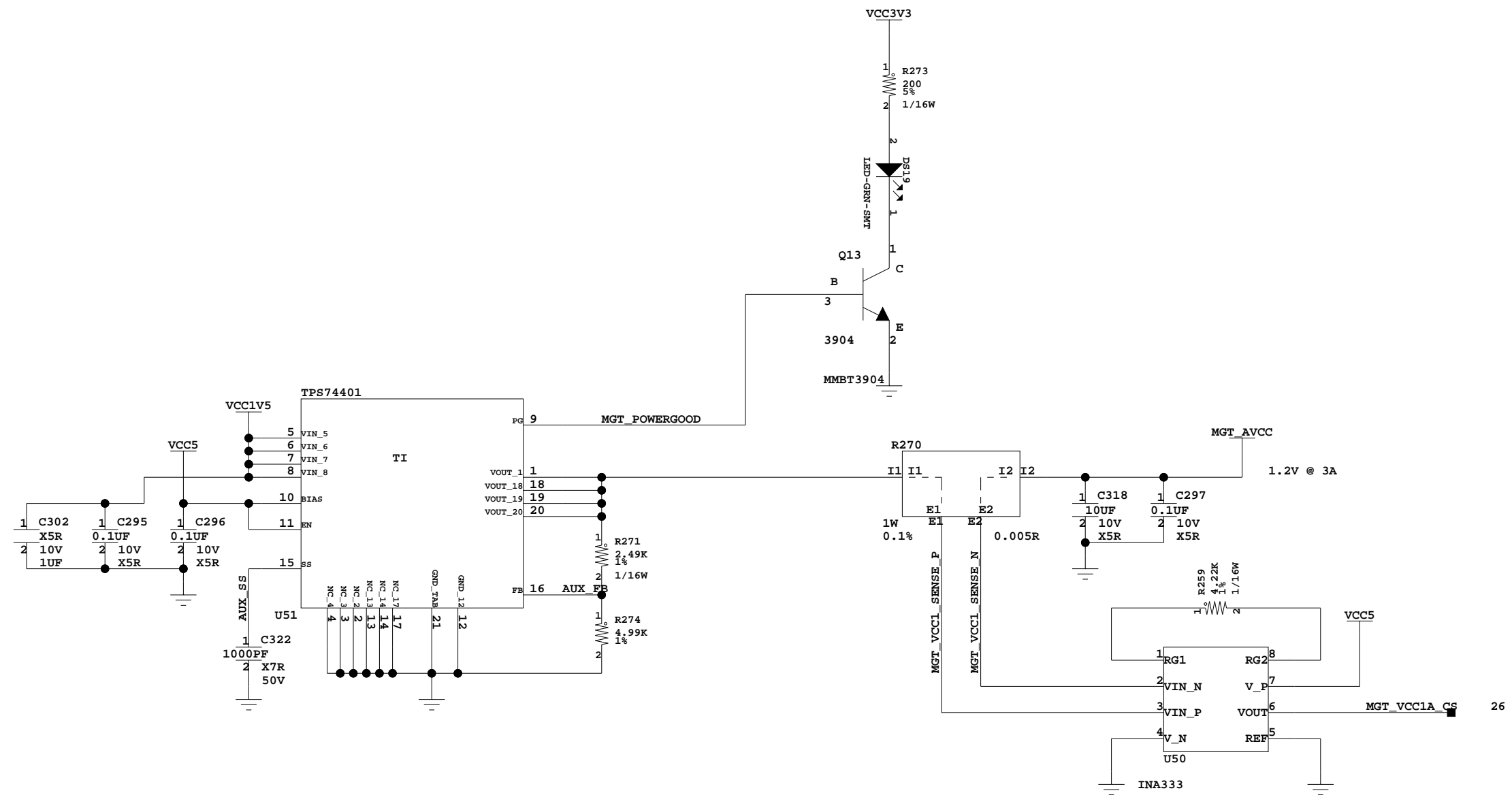
AGND should be a copper island underneath the 9240 and every associated module

FPGA UCD9240 PMBus Controller



Title: TI UCD9240 Power System SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM
 PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

Date: 9-24-2009_15:00 Ver: D
 Sheet Size: B Rev: 04
 Sheet 26 of 35 Drawn By BF

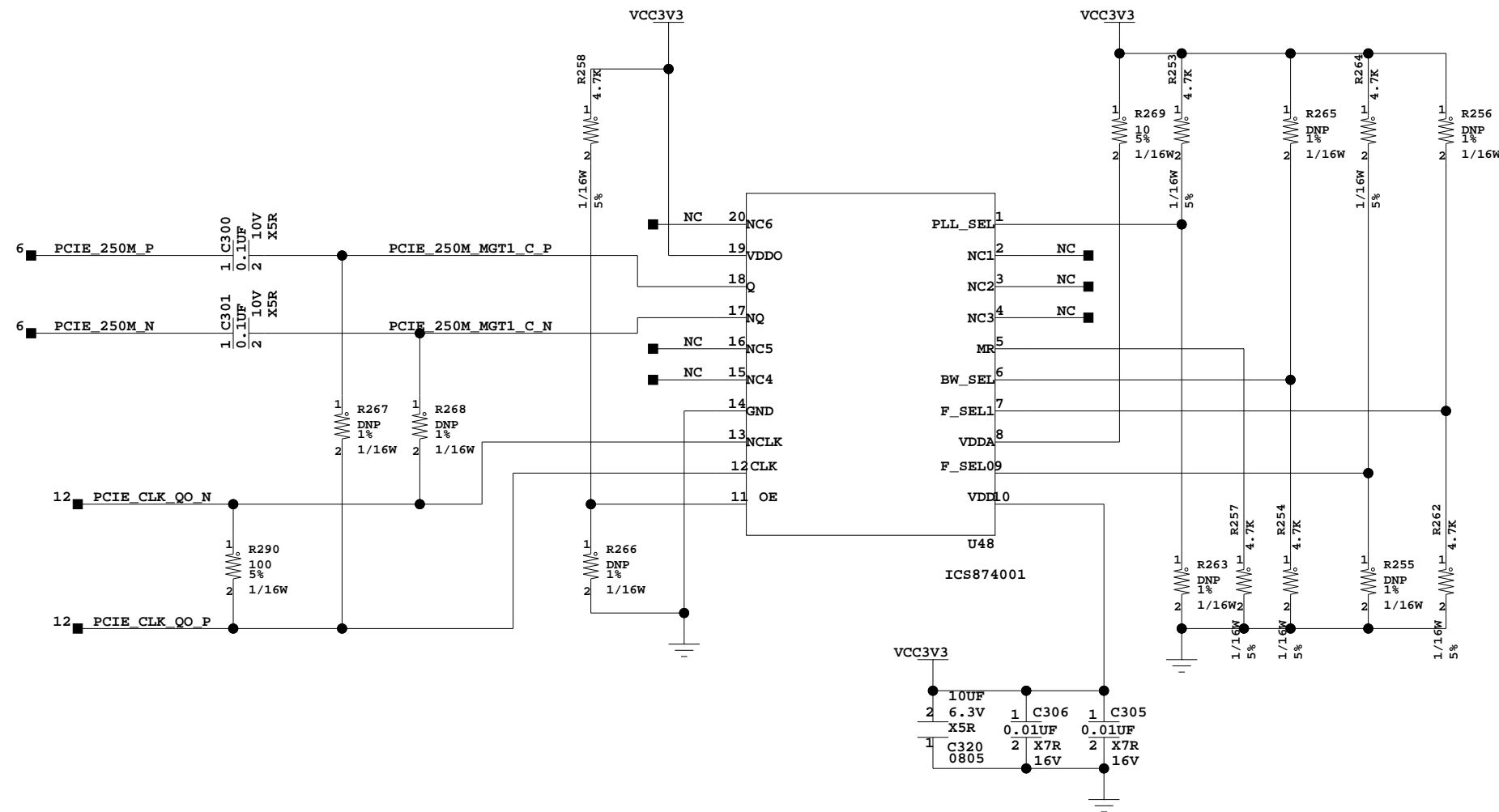
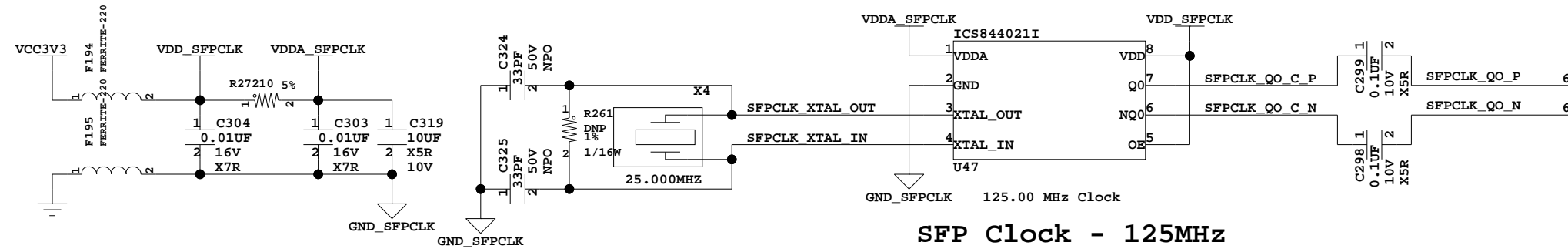


TPS74401 3A Max MGT Power



Title:	TPS74401 3A Max MGT Power SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCH P/N:	0431534
		SCH P/N:	0381305
		Test P/N:	TSS0123
		ART P/N:	1280473

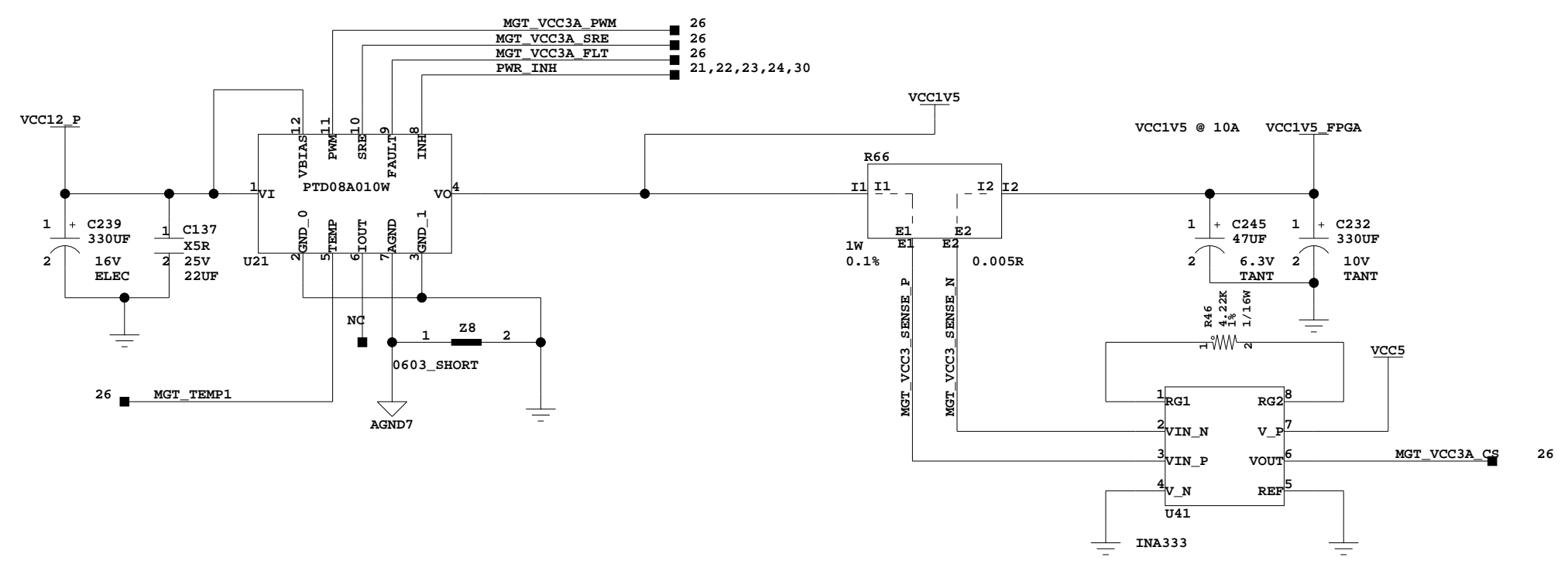
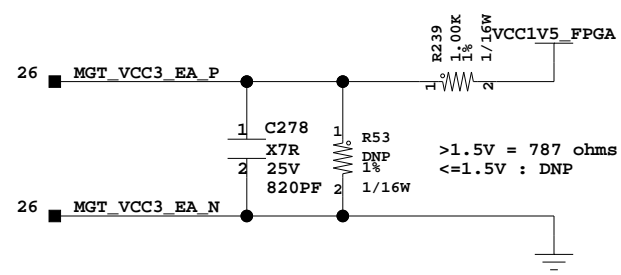
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Sheet Size:	B	Rev:	04
Sheet	27 of 35	Drawn By	BF



MGT Clocks



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Date: 9-24-2009_15:30	Ver: D	
Sheet Size: B	Rev: 04	
Sheet 28 of 35	Drawn By BF	



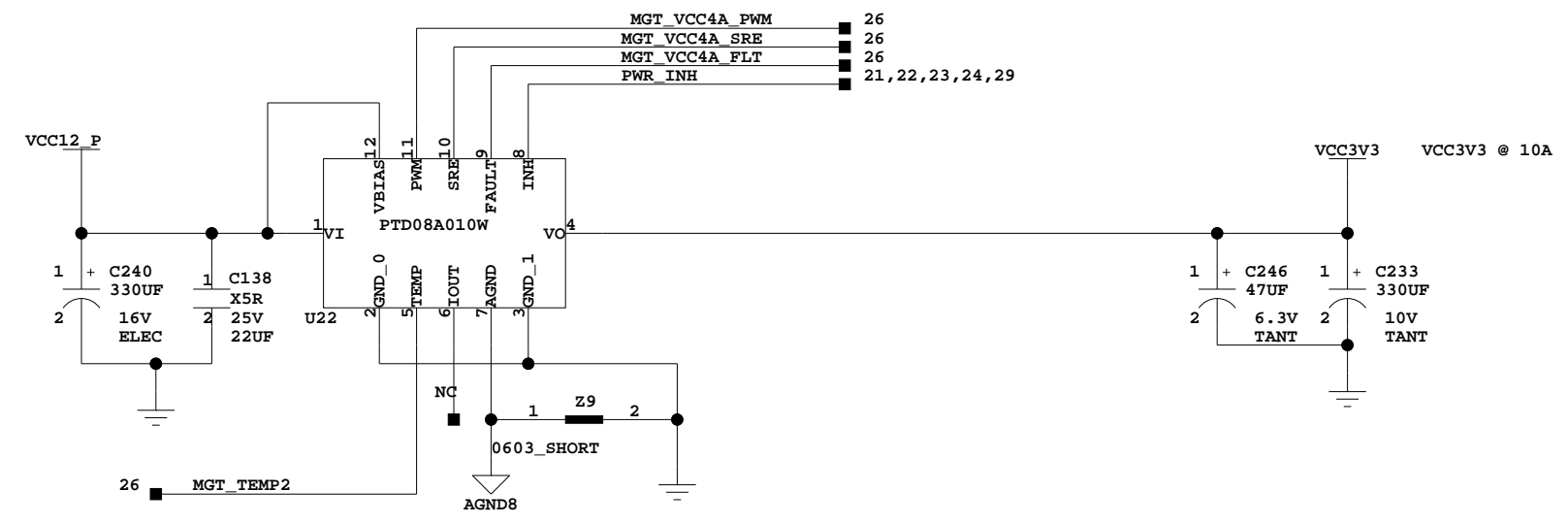
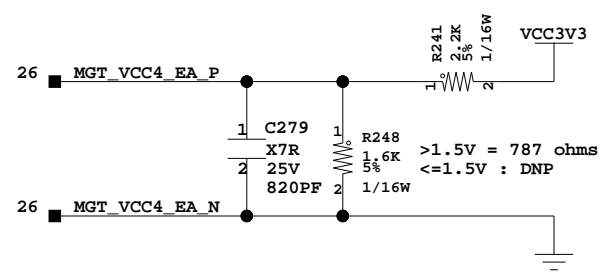
PTD08A010W 10A Max. Power Channel



Title: PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM

PCH P/N: 0431534
SCH P/N: 0381305
Test P/N: TSS0123
ART P/N: 1280473

Date:	9-18-2009_15:03	Ver:	D
Sheet Size:	B	Rev:	04
Sheet	29 of 35	Drawn By	BF

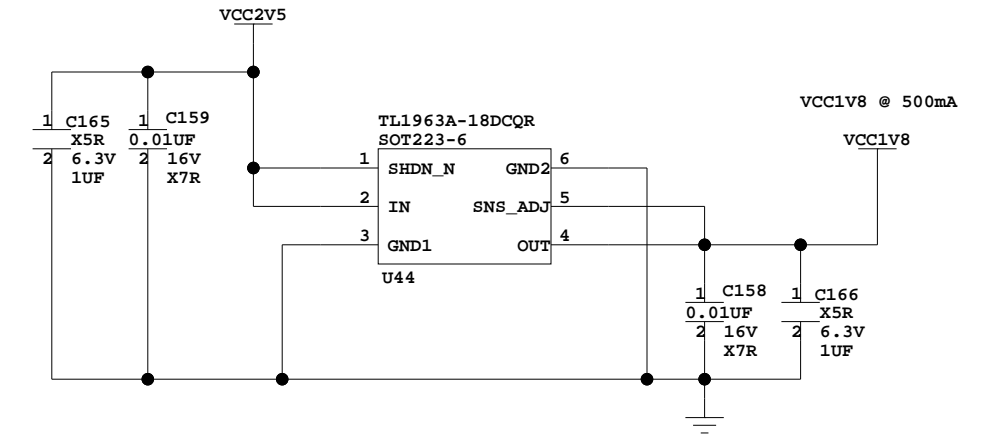
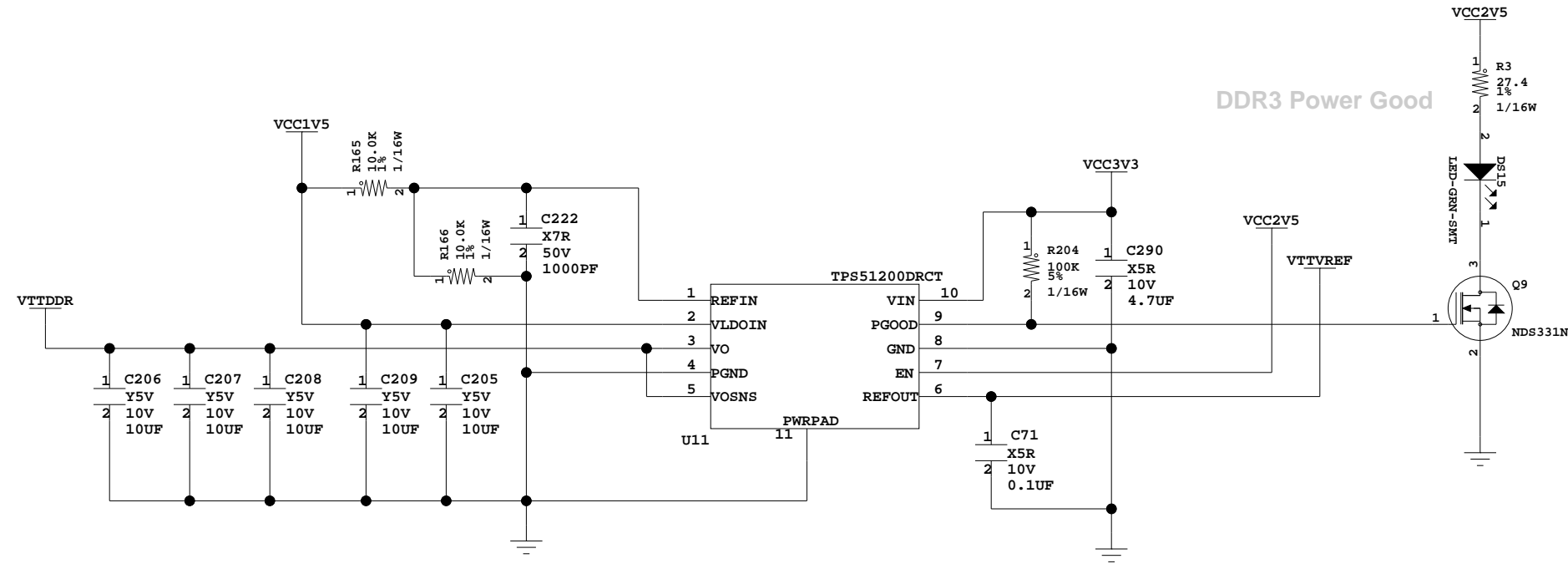


PTD08A010W 10A Max. Power Channel

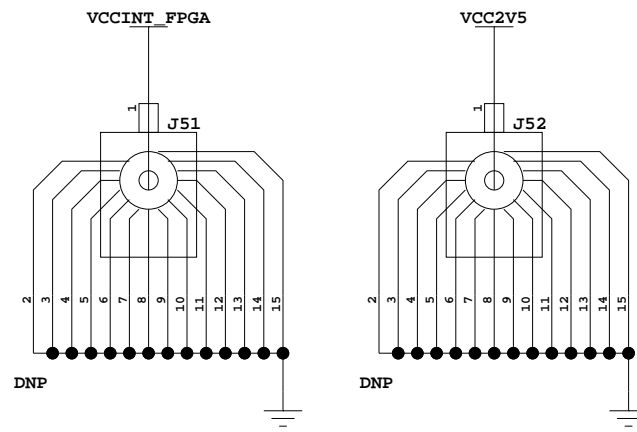


Title: PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM		PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473	
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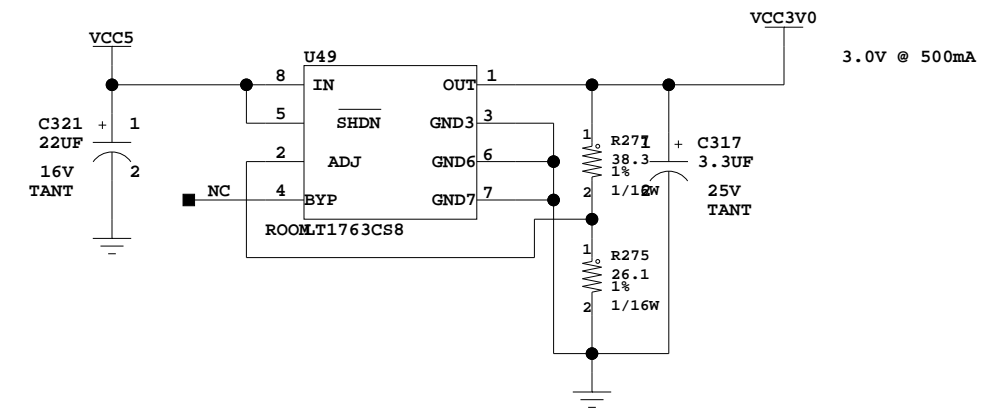
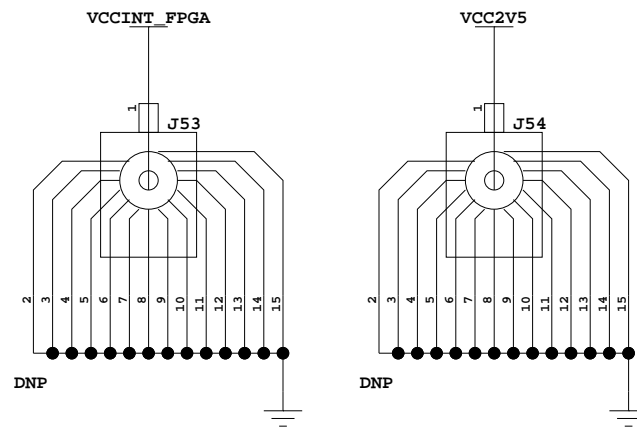
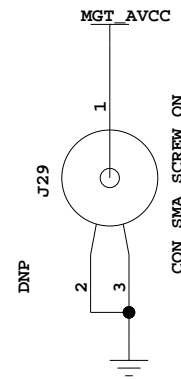
Date: 9-18-2009_15:03	Ver: D
Sheet Size: B	Rev: 04
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VCCINT_FPGA, VCCAUX Power Probe Channels



MGT Power Probe Channel



DDR3 Termination Regulator, power probe

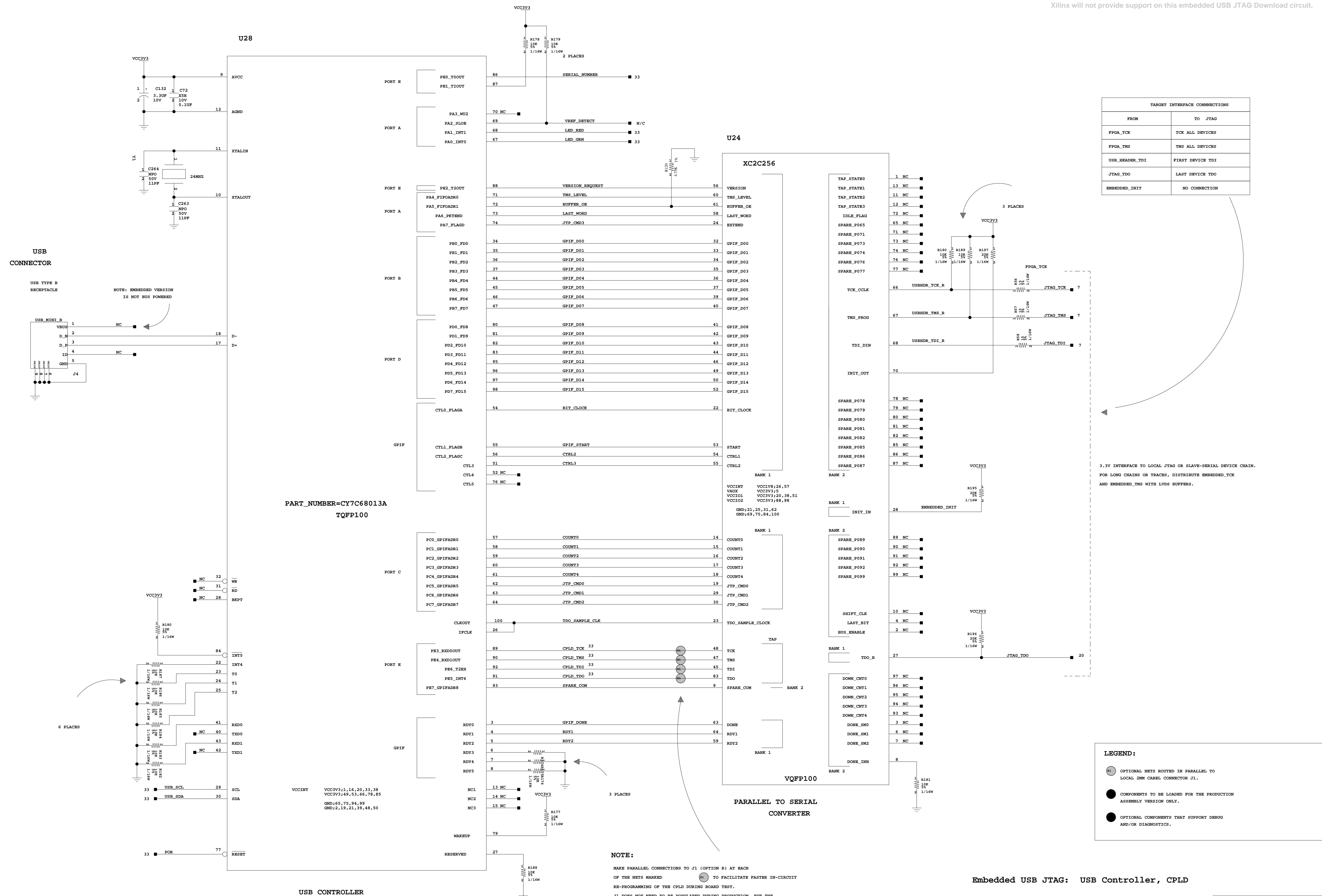


Title: DDR3 Termination Regulator, power probe
 SCHEM, ROHS COMPLIANT
 SP605 EVALUATION PLATFORM

PCB P/N: 0431534
 SCH P/N: 0381305
 Test P/N: TSS0123
 ART P/N: 1280473

Date:	9-24-2009_15:00	Ver:	D
Sheet Size:	B	Rev:	04
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The Embedded USB JTAG Download circuit on this page is for reference only!
 This circuit should not be designed into an end customer product or solution.
 Xilinx will not provide support on this embedded USB JTAG Download circuit.



TARGET INTERFACE CONNECTIONS	
FROM	TO JTAG
FPGA_TCK	TCK ALL DEVICES
FPGA_TMS	TMS ALL DEVICES
USB_HEADER_TDI	FIRST DEVICE TDI
JTAG_TDO	LAST DEVICE TDO
EMBEDDED_INIT	NO CONNECTION

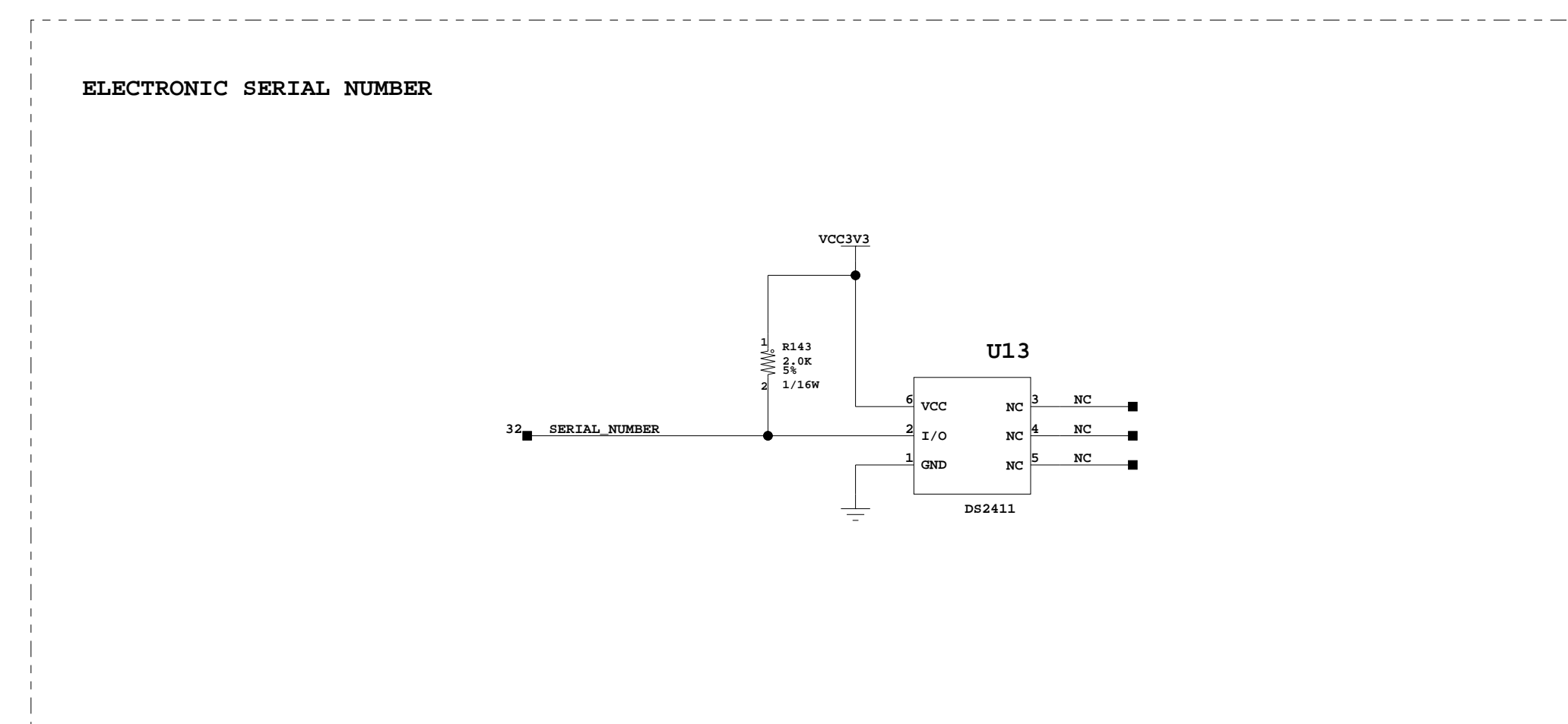
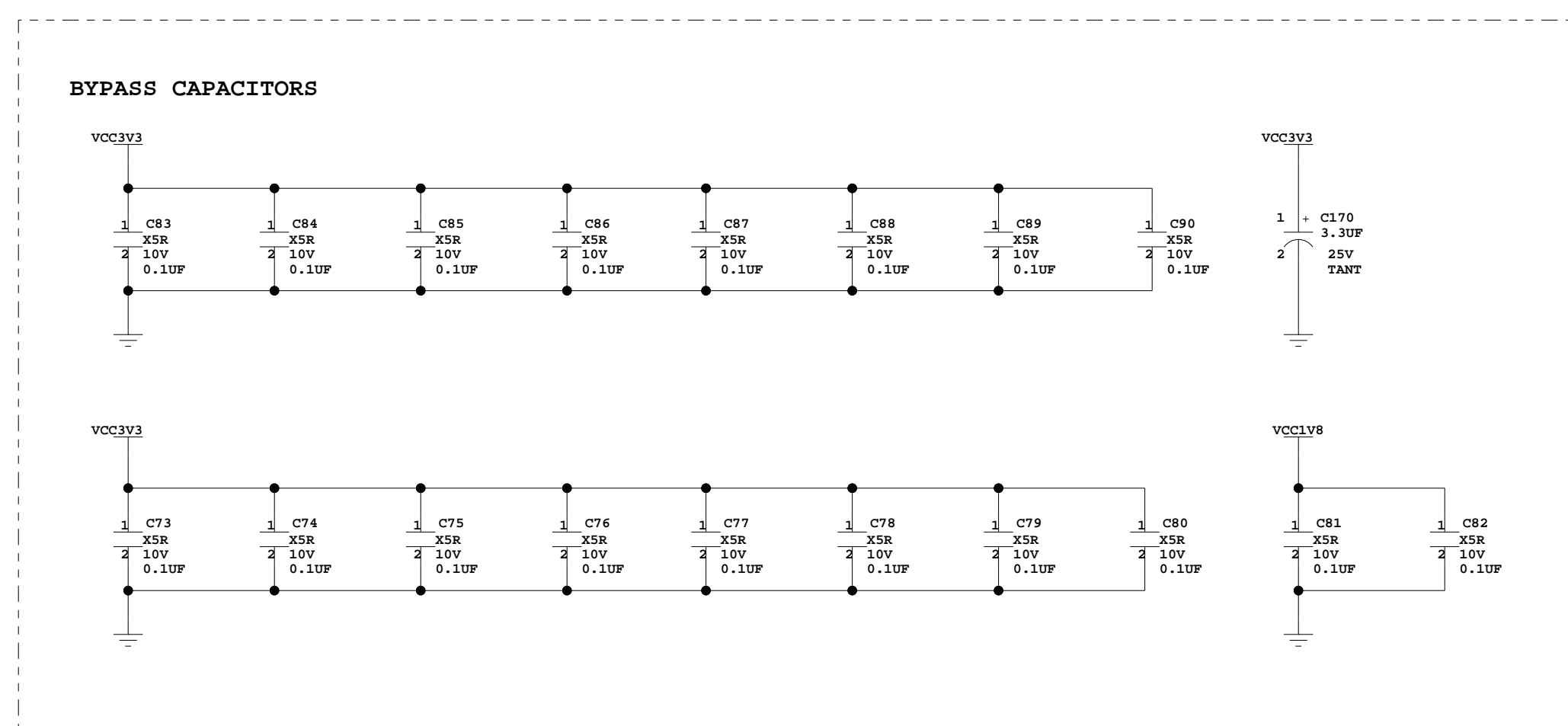
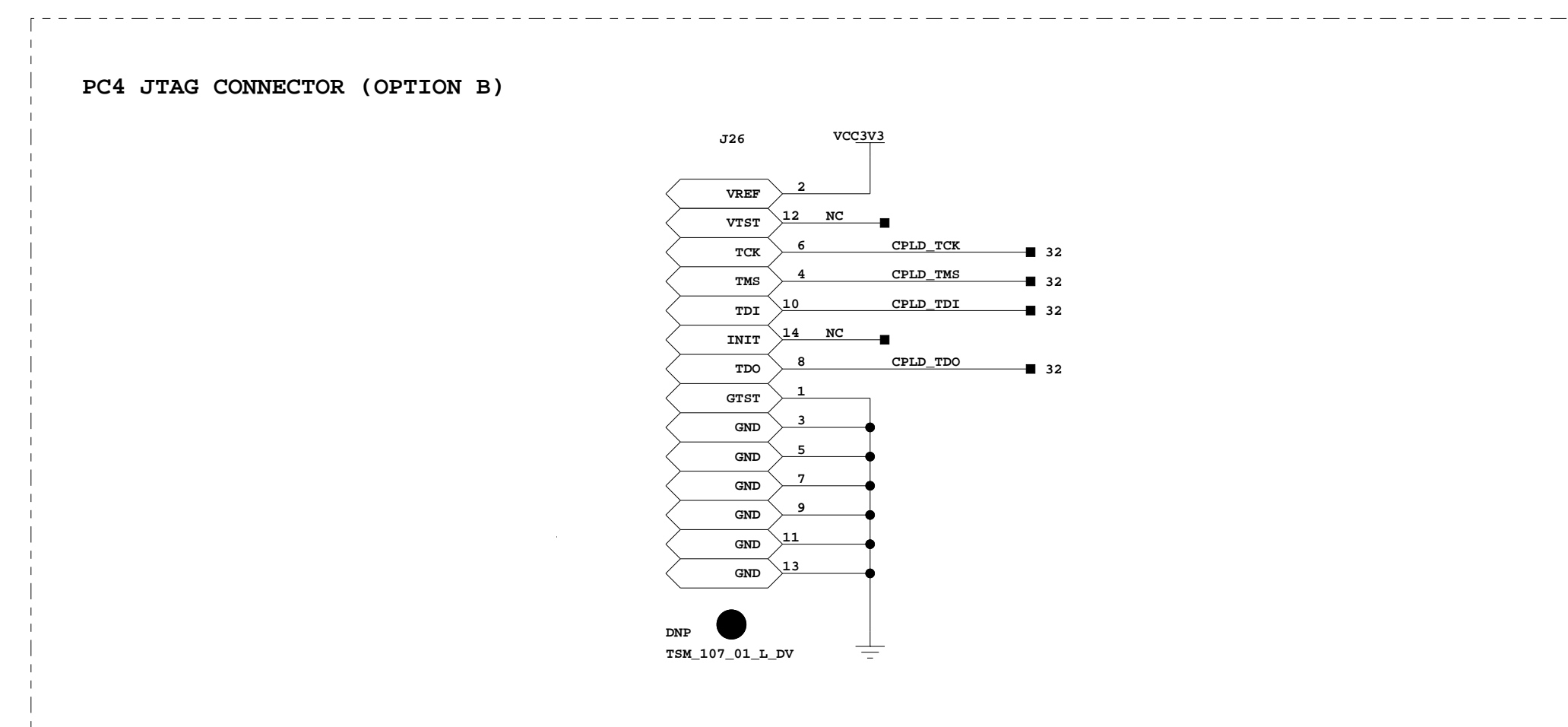
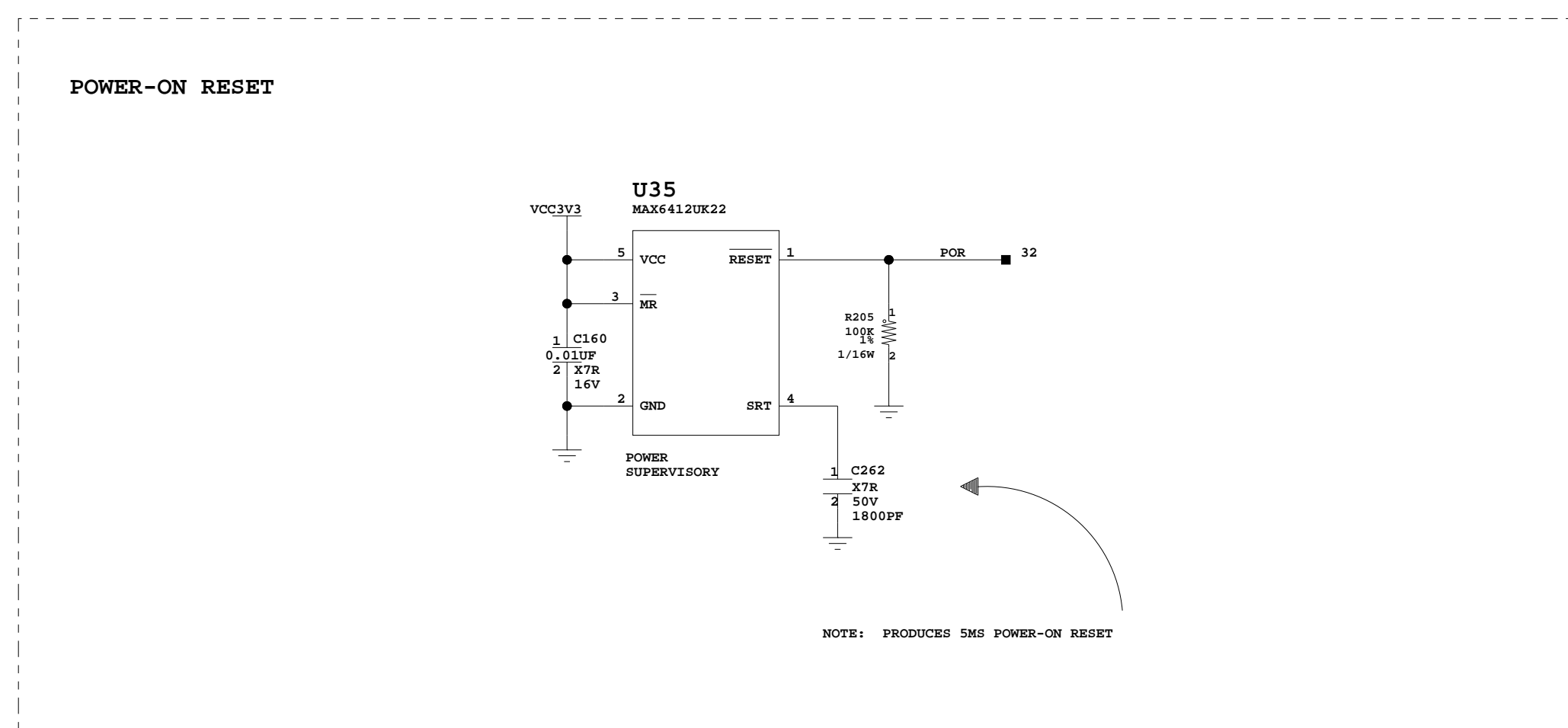
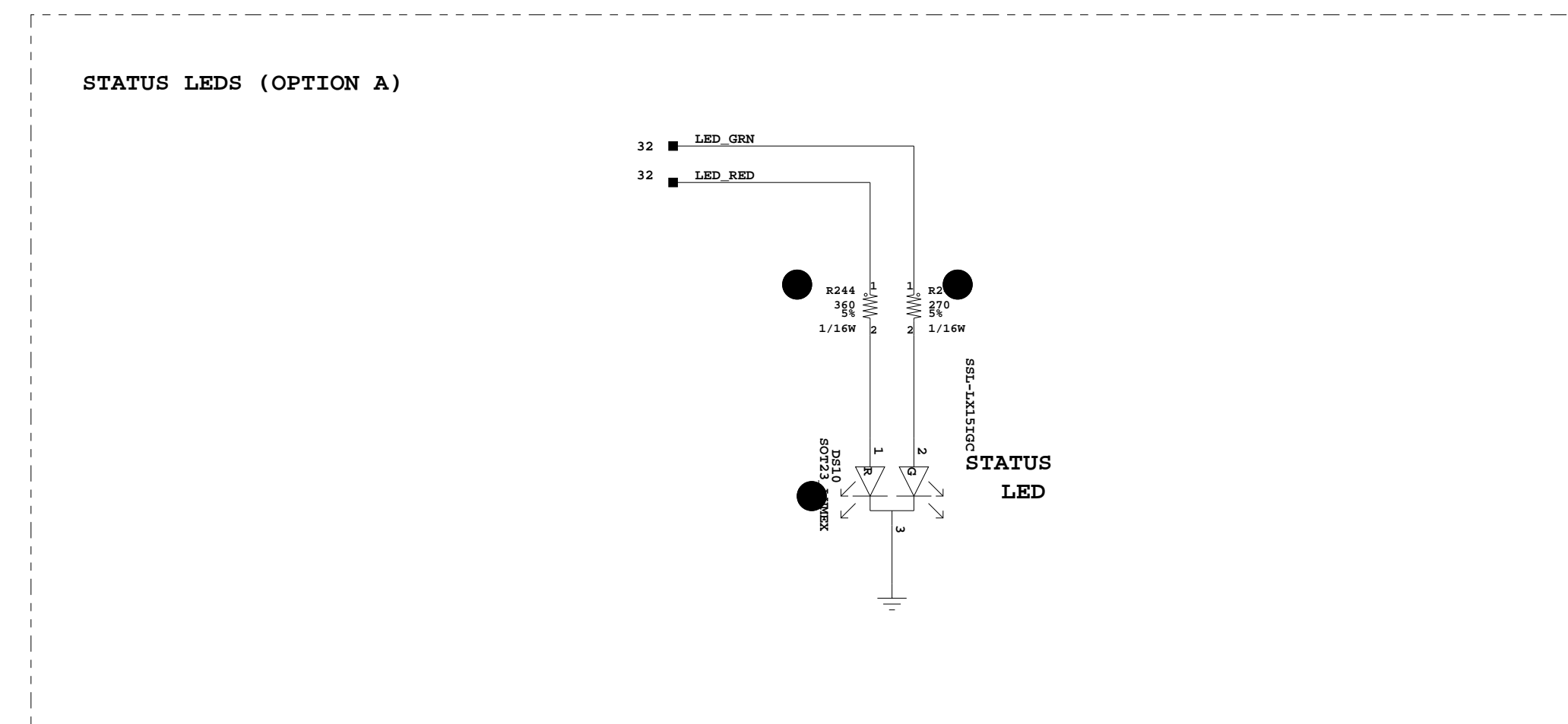
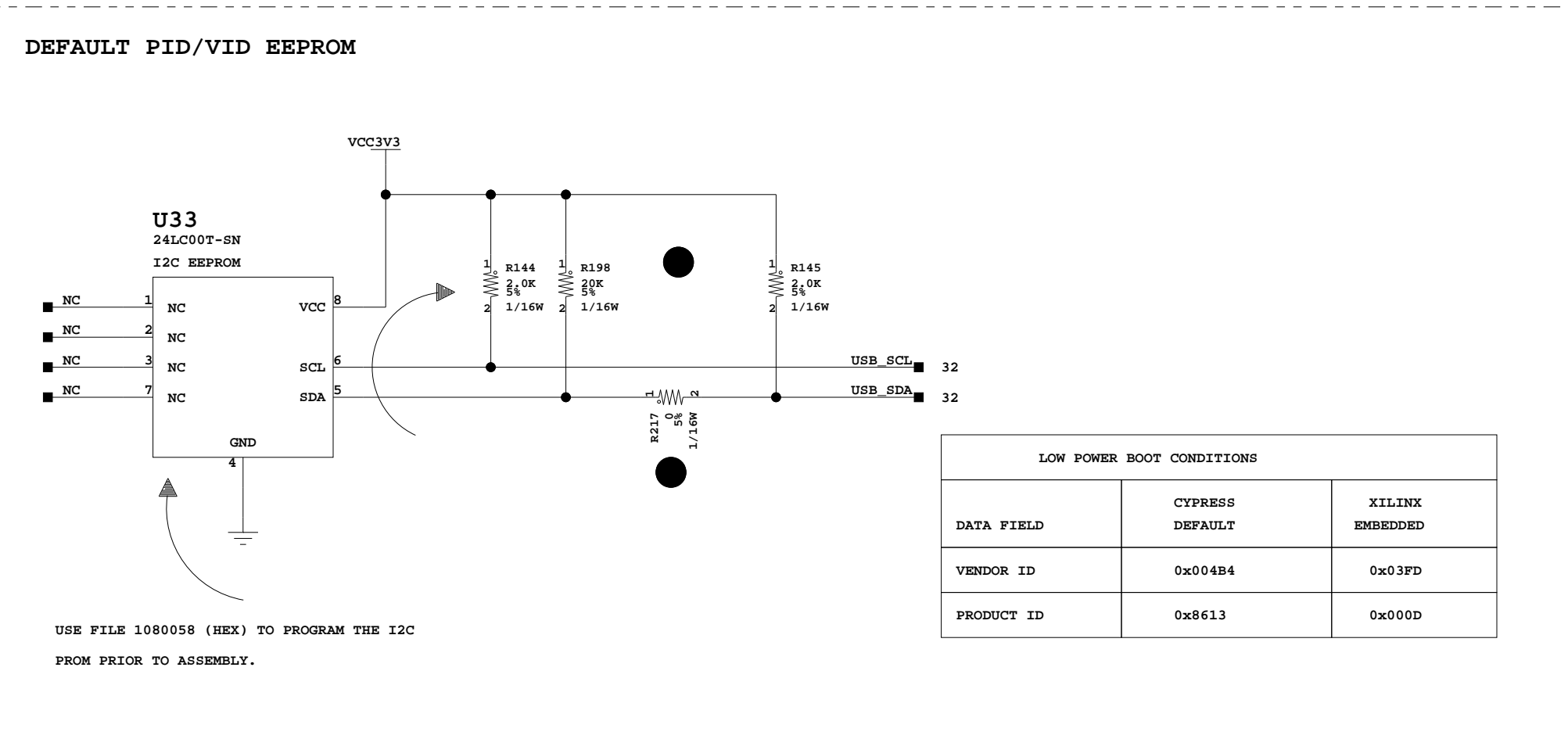
3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN.
 FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK
 AND EMBEDDED_TMS WITH LVDS BUFFERS.

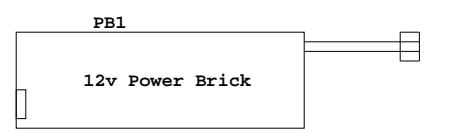
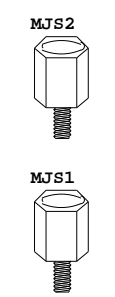
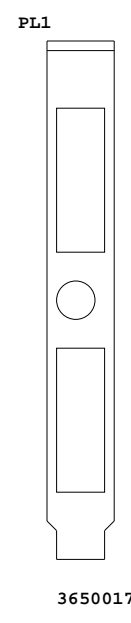
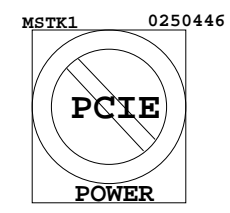
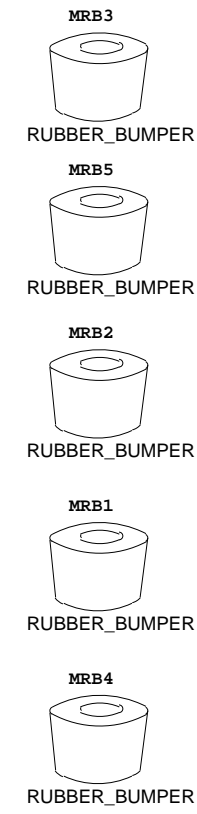
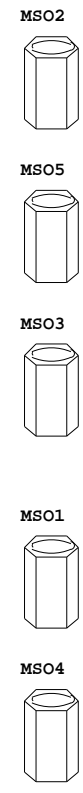
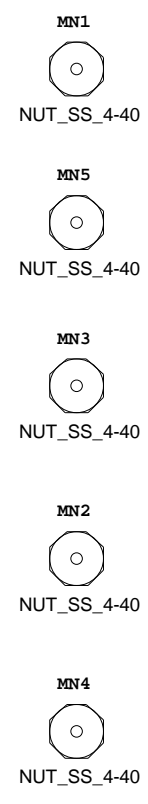
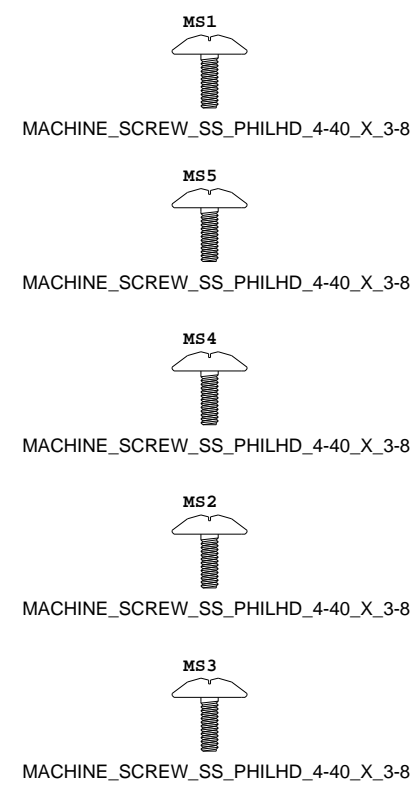
LEGEND:

- (○) OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 2MM CABEL CONNECTOR J1.
- (●) COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY.
- (○) OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS.

NOTE:
 MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH OF THE NETS MARKED (○) TO FACILITATE FASTER IN-CIRCUIT RE-PROGRAMMING OF THE CPLD DURING BOARD TEST. J1 DOES NOT NEED TO BE POPULATED DURING PRODUCTION, BUT THE ASSEMBLY FOOTPRINT IS RECOMMENDED FOR THE PWB LAYOUT.

Embedded USB JTAG: USB Controller, CPLD

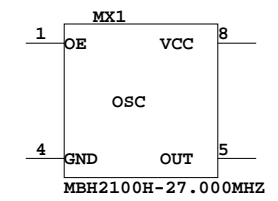




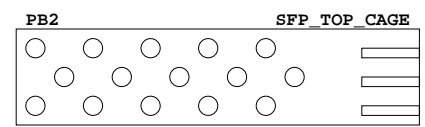
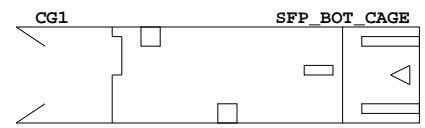
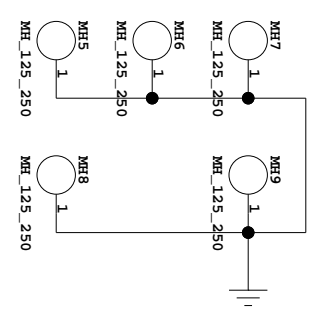
Power Cord



USB Mini-B Cable



Half Size Oscillator

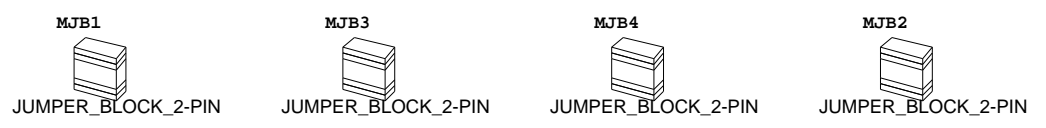


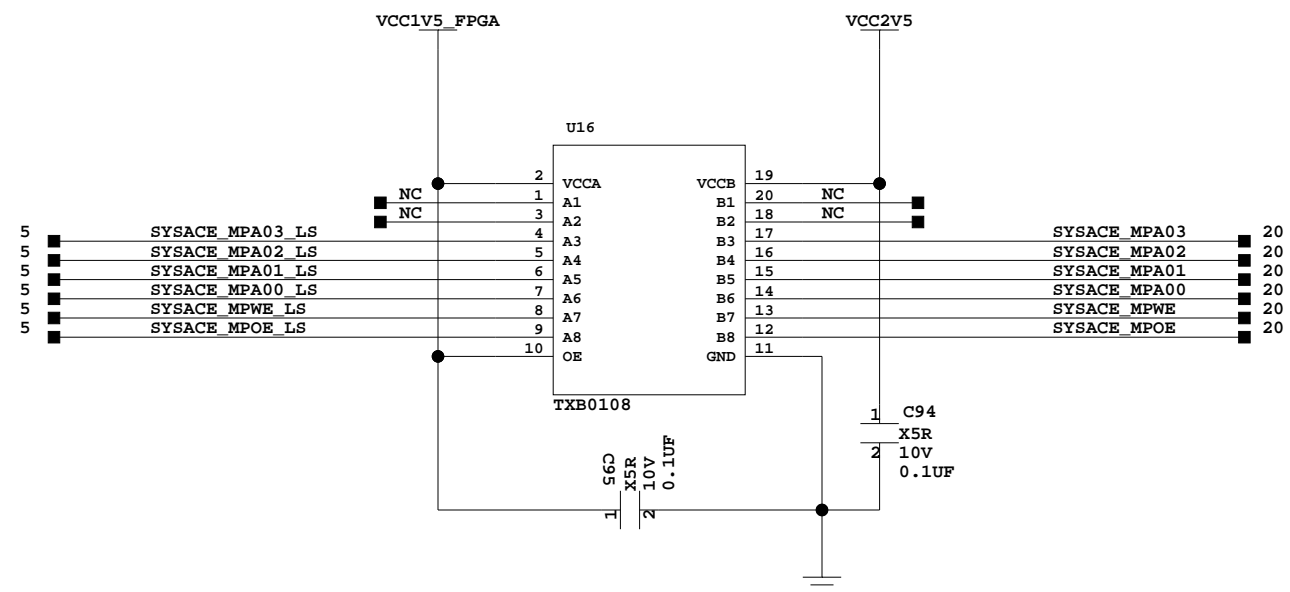
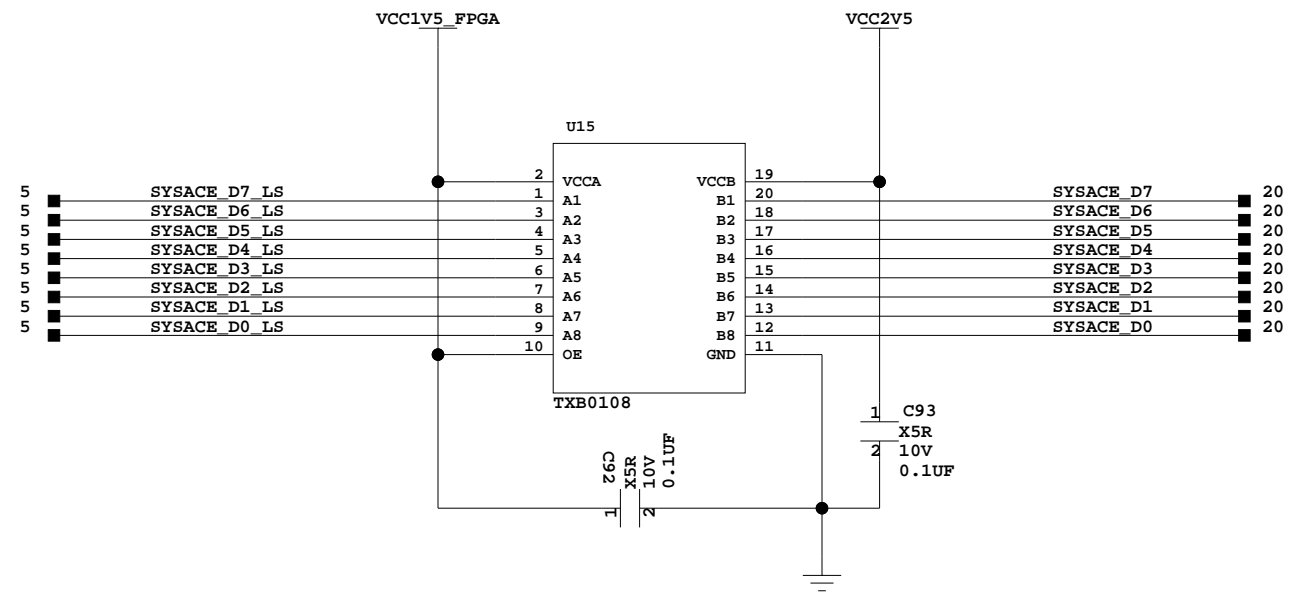
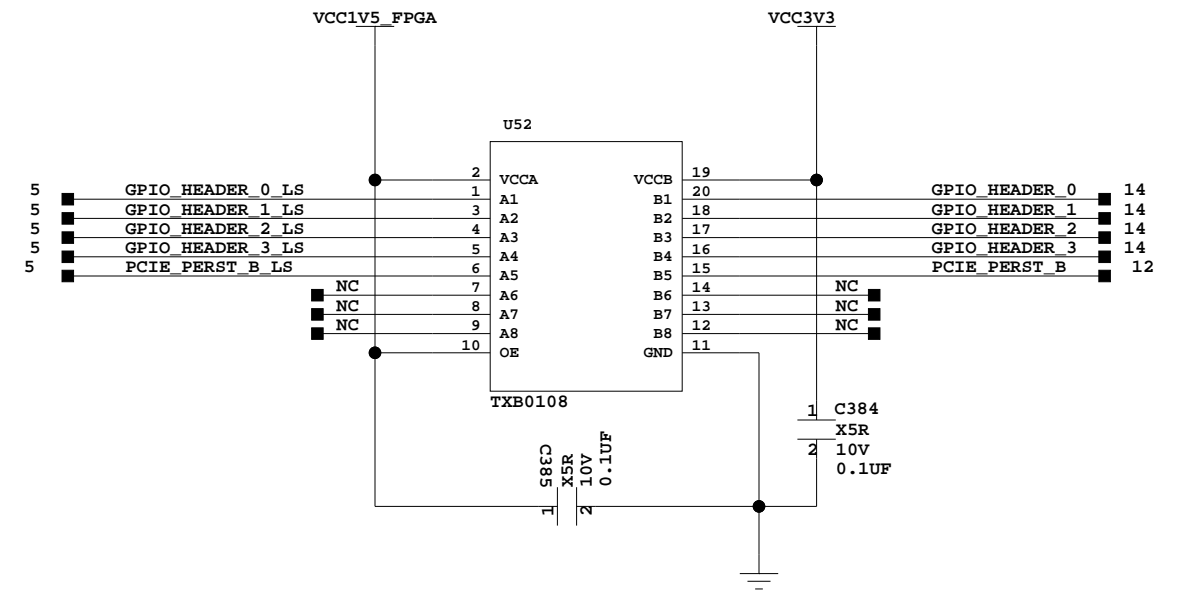
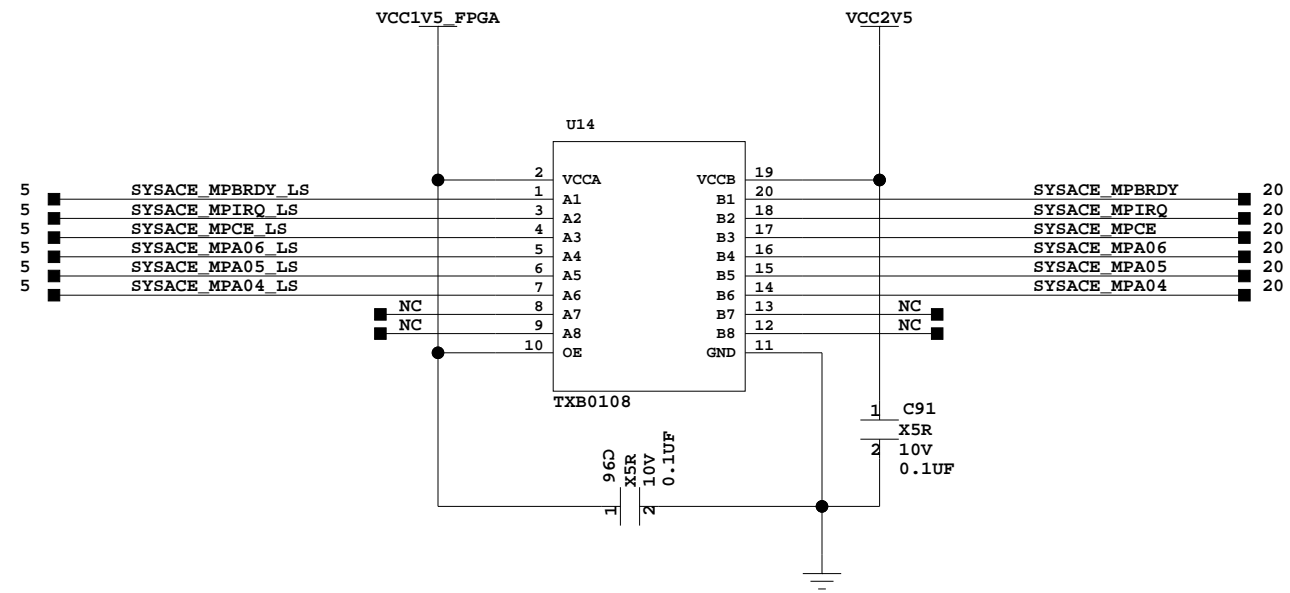
Mechanical Components



Title:	Mechanical Components SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	Pcb P/N:	0431534
		SCH P/N:	0381305
		Test P/N:	TSS0123
		ART P/N:	1280473

Date:	9-25-2009_10:34	Ver:	D
Sheet Size:	B	Rev:	04
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Level Shifters



Title:	Level Shifters SCHEM, ROHS COMPLIANT SP605 EVALUATION PLATFORM	PCB P/N: 0431534 SCH P/N: 0381305 Test P/N: TSS0123 ART P/N: 1280473
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Date:	9-24-2009_15:00	Ver:	D
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Sheet Size:	B	Rev:	04
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Sheet	35 of 35	Drawn By	BF
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