ZC702 Built-In Self Test
Flash Application

May 2012
Revision History

<table>
<thead>
<tr>
<th>Date</th>
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</tr>
</thead>
<tbody>
<tr>
<td>05/25/12</td>
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</tbody>
</table>

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Overview

- Xilinx ZC702 Board
- Software Requirements
- ZC702 Setup
- ZC702 BIST (Built-In Self Test)
  - Run the BIST Design
  - Run the USB Design
  - Run the LwIP Ethernet Design
- Compile ZC702 BIST Design
  - Run the USB Design from SDK
  - Creating and Testing an LwIP Ethernet Design
- References

Note: This presentation applies to the ZC702
ZC702 Board

Note: Presentation applies to the ZC702
ISE Software Requirement

- Xilinx ISE 14.1 software

Note: Presentation applies to the ZC702
EDK Software Requirement

- Xilinx EDK 14.1 software

Note: Presentation applies to the ZC702
EDK Software Requirement

- Xilinx SDK 14.1 software

Note: Presentation applies to the ZC702.
ZC702 Setup

Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the ZC702 board

- Connect this cable to your PC
- Set the JTAG Select Switch, SW10, to 01
- If using a Platform Cable USB (II) JTAG Cable, set SW10 to 10
ZC702 Setup

Connect a USB Type-A to Mini-B cable to the USB UART connector on the ZC702 board

- Connect this cable to your PC
- Power on the ZC702 board for UART Drivers Installation

Note: Presentation applies to the ZC702
ZC702 Setup

Installs USB UART Drivers

- CP210x VCP Win XP S2K3 Vista 7.exe

Note: Presentation applies to the ZC702
ZC702 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager

Note: Presentation applies to the ZC702
ZC702 Setup

➤ Expand the Ports Hardware
  – Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties

Note: Presentation applies to the ZC702
ZC702 Setup

Under Port Settings tab
- Click **Advanced**
- Set the COM Port to an open Com Port setting from COM1 to COM4

**Note:** Presentation applies to the ZC702
ZC702 Setup

- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to 115200

Note: Presentation applies to the ZC702
ZC702 Setup

➢ Set the SW16 DIP switches to boot from QSPI: 00010
  – The ZC702 QSPI comes preloaded with the BIST Application
  – Cycle power to start the BIST Application

Note: Presentation applies to the ZC702
ZC702 BIST

View initial BIST screen

Note: Presentation applies to the ZC702
ZC702 BIST

UART Test

- Type “1” to start the UART Test
- After each test, press any key to return to the main menu

Note: Presentation applies to the ZC702
ZC702 BIST

- LED Test
  - Type 2 to begin LED Test
- View LED DS23 Blinking

Note: Presentation applies to the ZC702
ZC702 BIST

IIC Test

- Type 3 to begin IIC Tests
- Completes four different IIC tests

Note: Presentation applies to the ZC702
ZC702 BIST

Timer Test
  - Type 4 to begin Timer Test

Note: Presentation applies to the ZC702
ZC702 BIST

- GPIO Switch Test
  - Set 2-position GPIO DIP Switch (SW15) or depress SW13 and SW14
  - Type 5 to begin GPIO Switch Test
    - Reads switch settings

Note: SW15-1 is tied to SW13; SW15-2 is tied to SW14
ZC702 BIST

SCU / GIC Test
  - Type 6 to begin SCU / GIC Test

Note: SCU / GIC means Snoop Control Unit / Generic Interrupt Controller
ZC702 BIST

SCU / GIC Test

- Type 7 to begin Device Configuration Interface Test

Note: Presentation applies to the ZC702
ZC702 BIST

Memory Test
  – Type 8 to begin External Memory Test

Note: Presentation applies to the ZC702
ZC702 BIST

Internal Memory Test

- Type 9 to begin Interrupt Tests

Note: Presentation applies to the ZC702
ZC702 BIST

Watchdog Timer Test
- Type A to begin Watchdog Timer Test

Note: Presentation applies to the ZC702
Run the USB Design
Run the USB Design

- Set SW16 DIP Switches to 00000
- Cycle board power to clear the BIST program

Note: Presentation applies to the ZC702
Caution

- This procedure will format a disk drive
  - Make sure you are formatting the ZC702 USB Flash and not your PC’s hard drive
  - Drive letters mentioned in this procedure will vary from PC to PC - verify the drive letter before formatting

- Xilinx cannot take responsibility for lost data or damaged hard drives

Note: Presentation applies to the ZC702
Run the USB Design

Start a ISE Design Suite Command Prompt and enter these commands:

```plaintext
cd C:\zc702_bist\ready_for_download
zc702_usb.bat
```
Run the USB Design

View your current set of disk drives

Note: Presentation applies to the ZC702
Run the USB Design

- Connect a USB Type-A to Micro-B cable to the USB ULPI connector on the ZC702 board
  - Connect this cable to your PC

Note: Presentation applies to the ZC702
Run the USB Design

» An extra removable drive will appear
  - In this case, “G:”

Note: Presentation applies to the ZC702
Run the USB Design

- Open the “G:” drive
  - A “Disk is not formatted” message will appear
  - If this is the correct drive, click Yes

Note: Presentation applies to the ZC702
Run the USB Design

- A format dialog for drive G: will appear
  - The size should be 1.00 MB
  - If this is the correct, click **Start**
  - Close this dialog when done

**Note:** Presentation applies to the ZC702
Run the USB Design

» At this point, you can copy small files to G: and verify the operation of this drive

Note: Presentation applies to the ZC702
Run the LwIP Ethernet Design
Run the LwIP Ethernet Design

» From the Windows Control Panel, open Network Connections
» Right-click on the Gigabit Ethernet Adapter and select Properties
Run the LwIP Ethernet Design

- Click Configure
  - Set the Media Type to Auto for 1 Gbps then click OK

Note: Presentation applies to the ZC702
Run the LwIP Ethernet Design

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:

![Local Area Connection 2 Properties](image1)

![Internet Protocol (TCP/IP) Properties](image2)

**Note:** Presentation applies to the ZC702
Run the LwIP Ethernet Design

» Set SW16 DIP Switches to 00000
» Cycle board power to clear the USB program

Note: Presentation applies to the ZC702
Run the LwIP Ethernet Design

- Connect an Ethernet cable to the Ethernet connector on the ZC702 board
  - Connect this cable to your PC

Note: Presentation applies to the ZC702
Run the USB Design

Start a ISE Design Suite Command Prompt and enter these commands:

```
    cd C:\zc702_bist\ready_for_download
    zc702_lwip.bat
```
Run the LwIP Ethernet Design

View LwIP echo server screen

--- lwIP TCP echo server -----
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
auto-negotiated link speed: 1000
TCP echo server started @ port 7

Note: Presentation applies to the ZC702
Run the LwIP Ethernet Design

» From a DOS window on the PC Host, enter the command:
  
  ```
  ping 192.168.1.10
  ```
  
  Ping from PC host 192.168.1.2 to ZC702 target 192.168.1.10

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design
Creating the ZC702 BIST Design

Open PlanAhead and Select Create New Project

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Click Next

Create a New PlanAhead Project

This wizard will guide you through the creation of a new project.

To create a PlanAhead project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you’ll be working with. Finally, you will specify your project sources and choose a default part.

To continue, click Next.
Creating the ZC702 BIST Design

- Set the Project name to “zc702_bist”
- Set the Project Location to “C:\”

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Select RTL Project

- **RTL Project**
  You will be able to add sources, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
  - Do not specify sources at this time

- **Post-synthesis Project**
  You will be able to add sources, view device resources, run design analysis, planning and implementation.
  - Do not specify sources at this time

- **I/O Planning Project**
  Do not specify design sources. You will be able to view part/package resources.

- **Import ISE Place & Route results**
  You will be able to do post-implementation analysis of your design.

- **Imported Project**
  Create a PlanAhead project from a Synplify, XST or ISE Project File.

**Note:** Presentation applies to the ZC702
Creating the ZC702 BIST Design

Select the ZC702 and click Next

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Click Finish

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

In PlanAhead, click Add Sources

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Select “Add or Create Embedded Sources” and click Next

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Click “Create Sub-Design”

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

» Name the module “zc702_bist_design”
» When XPS starts, click “No” for the BSB Wizard

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

In the XPS IP Catalog, add a Processing System instance

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Click on the Zynq tab to view the Processing System

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

» Click on the Import button
Creating the ZC702 BIST Design

- Select the ZC702 Development Board Template and click OK
- Click Yes to continue
- Once done, close XPS and return to PlanAhead

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

1. In PlanAhead, expand Design Sources
2. Right-click on the zc702_bist_design and select “Create Top HDL”
Creating the ZC702 BIST Design

The XPS project now appears as a sub-module.
Creating the ZC702 BIST Design

1. Select File → Export → Export Hardware
2. In the dialog, select Export Hardware and Launch SDK and click OK
Creating the ZC702 BIST Design

Create the BIST Application
- In SDK, select Xilinx C Project

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Create an empty application named bist_app
Creating the ZC702 BIST Design

Create a BSP named standalone_bsp_0
Creating the ZC702 BIST Design

The BIST application and BSP appears

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Create the Hello USB Application

- In SDK, select Xilinx C Project

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Create an empty application named hello_usb
Creating the ZC702 BIST Design

- Target the existing Standalone BSP
- Click Finish
Creating the ZC702 BIST Design

The Hello USB application appears

Note: Presentation applies to the ZC702
Creating the ZC702 BIST Design

Unzip the ZC702 BIST Design Files (14.1 CES)

- Available through http://www.xilinx.com/zc702
- This copies the BIST and USB source files to the SDK tree
- **Note:** This zip file includes a precompiled SDK project; if you want to open it in SDK, you must move it to C:\zc702_bist\ due to SDK path dependencies

**Note:** Presentation applies to the ZC702
Creating the ZC702 BIST Design

After the BSP finishes compiling, select the BIST and USB applications and press “F5” to refresh

- This will cause it to see the new source files and rebuild the design

Note: Presentation applies to the ZC702
Creating a BOOT.bin Image
Creating a BOOT.bin Image

- The Boot Image requires:
  - FSBL (First Stage Boot Loader) ELF file
  - An ELF for the PS

- To create an FSBL ELF file
  - In SDK select Xilinx C Project
Creating a BOOT.bin Image

Select Zynq FSBL and click Finish
Creating a BOOT.bin Image

Select Xilinx Tools → Create Boot Image

Note: Presentation applies to the ZC702
Creating a BOOT.bin Image

- Select “Create a new bif file…”
- Add the FSBL ELF, bitstream, and application ELF
  - The FSBL must be first
  - The bitstream must be before the application ELF
  - For use on an SD card, the output file must be named “BOOT.bin”

Note: Presentation applies to the ZC702
Creating a BOOT.bin Image

Click “Create Image”

Note: Presentation applies to the ZC702
Creating a BOOT.bin Image

Two files are created:

- BOOT.bin
- BOOT.mcs

Note: Presentation applies to the ZC702
Programming the ZC702 QSPI
Programming the ZC702 QSPI

Set SW16 DIP Switches to 00000

Note: Presentation applies to the ZC702
Programming the ZC702 QSPI

Select Xilinx Tools → Program Flash

Note: Presentation applies to the ZC702
Programming the ZC702 QSPI

- Select the BOOT.mcs as the image file
- Click Program
- When this second dialog appears, power cycle the board, if needed, then click OK

Note: Presentation applies to the ZC702
ZC702 Setup

- Set the SW16 DIP switches to boot from QSPI: 00010

Note: Presentation applies to the ZC702
Programming the ZC702 QSPI

Push POR_B Button (SW1)

Note: Presentation applies to the ZC702
Programming the ZC702 QSPI

The PL LEDs will be blinking in a pattern controlled by SW12

Note: Presentation applies to the ZC702
Run the USB Design from SDK
Run the USB Design from SDK

- Set SW16 DIP Switches to 00000

**Note:** Presentation applies to the ZC702
Run the USB Design from SDK

- Select “hello_usb”
- Under the green “Run” button, select Run As → Launch on Hardware

Note: Presentation applies to the ZC702
Run the USB Design from SDK

- View your current set of disk drives

[Image: My Computer window displaying disk drives]

**Note:** Presentation applies to the ZC702
Run the USB Design from SDK

- An extra removable drive will appear
  - In this case, “G:”

Note: Presentation applies to the ZC702
Run the USB Design from SDK

- Open the “G:” drive
  - A “Disk is not formatted” message will appear
  - If this is the correct drive, click Yes

Note: Presentation applies to the ZC702
Run the USB Design from SDK

- A format dialog for drive G: will appear
  - The size should be 1.00 MB
  - If this is the correct, click **Start**
  - Close this dialog when done

*Note: Presentation applies to the ZC702*
Run the USB Design from SDK

At this point, you can copy small files to G: and verify the operation of this drive

Note: Presentation applies to the ZC702
Creating and Testing an LwIP Ethernet Design
Creating and Testing an LwIP Ethernet Design

- Set SW16 DIP Switches to 00000

Note: Presentation applies to the ZC702
Creating and Testing an LwIP Ethernet Design

Create the LwIP Application
- In SDK, select Xilinx C Project

Note: Presentation applies to the ZC702
Creating and Testing an LwIP Ethernet Design

- Select the LwIP Echo Server project
- Click Next
Creating and Testing an LwIP Ethernet Design

- LwIP requires a different BSP
- Allow the tool to create a new BSP
- Click Finish
Creating and Testing an LwIP Ethernet Design

- Select “lwip_echo_server_0”
- Under the green “Run” button, select Run As → Launch on Hardware
Creating and Testing an LwIP Ethernet Design

View LwIP echo server screen

Note: Presentation applies to the ZC702
Creating and Testing an LwIP Ethernet Design

From a DOS window on the PC Host, enter the command:

`ping 192.168.1.10`

- Ping from PC host 192.168.1.2 to ZC702 target 192.168.1.10

Note: Presentation applies to the ZC702
References

EDK Documentation
  – Embedded System Tools Reference Guide
    • http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/est_rm.pdf

7 Series Configuration
  – 7 Series FPGAs Configuration User Guide
Documentation

- **Zynq-7000 EPP**
  - Zynq-7000 Extensible Processing Platform

- **ZC702 Documentation**
  - Xilinx Zynq-7000 EPP ZC702 Evaluation Kit
  - ZC702 Getting Started Guide