

## Overview

The purpose of this notification is to communicate a 10-layer package substrate change for select Virtex®-5 LX FPGA devices.

## Description

LX devices in packages greater than 1000 pins will begin transitioning to 10-layer package substrate, as part of the Xilinx material standardization for the Virtex-5 FPGA family. This change is backward-compatible with current production devices. This change will not affect the current package outline drawing.

## Key Dates and Ordering Information

Key dates for this notice are in the following table.

*Table 1: Key Dates for Package Transition*

Notification Date	Implementation Date* (Cross-shipping starts)
December 31, 2007	May 1, 2008

\*Starting from May 1, 2008, orders using standard part numbers will receive devices in either 8-layer or 10-layer.

## Products Affected

The affected devices are listed in Products Transitioning to 10-Layer. This change applies to all speeds and grades for the devices listed in Products Transitioning to 10-Layer.

*Table 2: Products Transitioning to 10-Layer*

Devices
XC5VLX50-FF(G)1153
XC5VLX85-FF(G)1153
XC5VLX110-FF(G)1153
XC5VLX110-FF(G)1760

## Traceability

Customers requiring information on traceability should contact [Xilinx Technical Support](#).

## Response

**Note:** In accordance with JESD46-C, this change is deemed accepted by the customer if no acknowledgement is received within 30 days from this notice.

No response is required by this notice. For additional information or questions, please contact [Xilinx Technical Support](#).

**Important Notice:** Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the MySupport website (<http://www.xilinx.com/support>). Register today and personalize your “MyAlerts” area to include Customer Notifications. This change provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Xilinx [Answer Record 18683](#).

## Additional Documentation

Below is a list of documents that are associated with this notice:

- Qualification Report ([RPT091](#))
- FAQ: Implications of XCN07025 ([XTP027](#))

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/24/07	1.0	Initial release.
03/11/08	1.0.1	Added Additional Documentation section.
06/15/09	1.0.2	Minor edit to remove XTP030 from the Additional Documentation section

## Disclaimer

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