

# Customer Update XCU2000-02

## Design Process Marginality on Virtex 32x1 Distributed SelectRAM

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**Subject:** The Virtex™ family contains a design process related marginality that may affect functionality of the distributed (LUT-based) SelectRAM when configured in a 32x1 mode. It is recommended that customers do not use these devices in this mode.

This marginality issue occurs when a customer write enables data into the LUT. The write strobe signal that loads the data into the memory cells is not wide enough to accommodate the full range of process variation across the die. The device then fails since some of the data was not written to the memory address location. The failure is seen as a random LUT failure typically at a single location within the array.

This failure is not time dependent; therefore, all devices that have shipped in fully functional systems are not expected to experience field failures. It is recommended that customers do not re-configure these devices with different patterns containing 32x1 distributed RAM once they have been deployed in the field.

**Products Affected:** All Virtex production devices, all Spartan™-II engineering (ES) devices, and some Spartan-II (non-ES) production devices are affected. This design marginality does not affect any Virtex-E production devices. This design marginality does not affect any designs configured in a 16x1 mode.

**Change Description:** The design process marginality was identified in all Virtex products. It is recommended that customers planning to use the 32x1 configuration in their design instead use two LUT's configured as 16x1 within a slice which can be combined to create a 32x1 bit RAM. Xilinx plans to implement a fix for this design process marginality.

**Reason For Change:** The fix widens the write strobe signal to accommodate a larger variation of memory cells.

**Key Dates:** Xilinx will issue a PCN (Product Change Notification) in November, 2000, which will have more detail on product traceability and availability. Xilinx plans to ship product with the fixed material in Q1 2001.

*Note added on 1/31/2001 - PCN2001-05 has been released to detail product traceability and availability.*

**Response:** No response to this notification is required. Requests for additional data or support should be made to your local Xilinx FAE, or email [pcn@xilinx.com](mailto:pcn@xilinx.com).