Radiation-Hardened, Space-Grade Virtex-5QV Family Overview

DS192 (v1.4) November 12, 2014 **Product Specification**

General Description

The only reprogrammable and highest density radiation-hardened (RH) FPGA, the space-grade Virtex®-5QV FPGA provides RH by design technology to meet the requirements of space applications that demand high-performance as well as high reliability. For years, ASICs were the only solution available to system designers of high-performance space applications with long development and fabrication times as well as high non-recurring engineering (NRE) costs. The Virtex-5QV FPGA combines unparalleled density, performance, and radiation hardening with the flexibility of reconfigurability without the high risk of ASICs.

The Virtex-5QV device provides the compelling set of performance, features, and solutions for the radiation-hardened systems market. Using the second generation Advanced Silicon Modular Block (ASMBL™) column-based architecture, the Virtex-5QV FPGA contains an array of features to address the needs of a wide variety of advanced logic designs and many dedicated system-level blocks, including powerful 36 Kb block RAM and FIFOs, second-generation 25 x 18 DSP slices, SelectIO™ technology with built-in digitally controlled impedance, ChipSync™ source-synchronous interface blocks, enhanced clock management tiles with integrated digital clock managers (DCMs), phase-locked-loop (PLL) clock generators, and advanced configuration options. Additional features include power-optimized, high-speed serial transceiver blocks for enhanced serial connectivity, PCI Express® compliant integrated Endpoint blocks, and tri-mode Ethernet Media Access Controllers (MACs). These features allow advanced logic designers to build the highest levels of connectivity and performance into their FPGA-based systems. Built on a proven 65-nm copper process technology, the Virtex-5QV FPGA is a modern programmable alternative to custom ASIC technology. The Virtex-5QV FPGA offers the latest solution for addressing the needs of critical space missions where design changes can be accommodated late in the program or through reprogrammability, even after launch.

A Virtex-5QV FPGA provides exceptional hardness to single-event upsets (SEUs), total immunity to single-event latch-ups (SELs), total ionizing doses (TIDs) of over 1 Mrad(Si), and datapath protection from single-event transients (SETs). Compatibility with the commercial and defense-grade Virtex-5 FPGAs allows for low-cost, rapid prototyping and easy design migration to flight hardware without the need for PCB changes.

Table 1: **Virtex-5QV FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)				DSP48E Slices(2)	Block RAM Blocks			CMTs (4)	Endpoint Blocks for PCI Express	Ethernet MACs(5)	Max RocketIO GTX Transceivers (6)	Total I/O Banks (7)	Max User I/O(8)
	Logic Cells	Array (Row x Col)	CLB Slices (1)	Max Distributed RAM (Kb)		18 Kb (3)	36 Kb	Max (Kb)						
XQR5VFX130	131,072	200 x 56	20,480	1,580	320	596	298	10,728	6	3	6	18	24	836

Notes:
1. Virtex-5QV FPGA CLB slices are organized differently from previous generations. Each CLB slice contains four LUTs and four flip-flops (previously it was two LUTs and two flip-flops.)
2. Each DSP48E slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. This table lists separate Ethernet MACs per device.
6. RocketIO™ GTX transceivers are designed to run from 150 Mb/s to 4.25 Gb/s.
7. Includes configuration Bank 0.
8. This number does not include RocketIO transceivers.

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Summary of Radiation-Hardened Virtex-5QV Device Features

- The only reprogrammable RH FPGA in the industry
- Highest density RH FPGA
- Full V-Grade manufacturing and process flow
- High signal-integrity ceramic flip-chip column grid array packaging
- Guaranteed operation over full military temperature range (–55°C to +125°C)
- Guaranteed 1 Mrad(Si) total ionizing dose per method 1019
- Guaranteed SEE latch-up immunity to LET >100 MeV per mg-cm^2
- Radiation-Hardened By Design (RHBD) technology
- SEU Hardened Configuration Memory Cells and control logic
  - Configuration Memory Orbital Upset Rate (GEO): 3.8E-10 errors/bit/day
  - Configuration Control Logic Single-Event Functional Interrupt (SEFI) Orbital Upset Frequency (GEO): less than once every 10,000 years
- SEU and SET Hardened CLB flip-flops
- SEU Hardened IOB flip-flops and DCI control
- Embedded error detection and correction (EDAC) and autonomous writeback for high-performance Block Memory SEU Mitigation
- Fully characterized for space radiation effects in heavy ion and proton environments
- Most advanced, high-performance, optimal-utilization, FPGA logic
  - Real 6-input look-up table (LUT) technology
  - Dual 5-LUT option
  - Improved reduced-hop routing
  - 64-bit distributed RAM option
  - SRL32/Dual SRL16 option
  - Powerful clock management tile (CMT) clocking
  - Digital Clock Manager (DCM) blocks for zero delay buffering, frequency synthesis, and clock phase shifting
  - PLL blocks for input jitter filtering, zero delay buffering, frequency synthesis, and phase-matched clock division
- 36 Kb block RAM/FIFOs
  - True dual-port RAM blocks
  - Enhanced optional programmable FIFO logic
  - Programmable
    - True dual-port widths up to x36
    - Simple dual-port widths up to x72
  - Built-in optional error-correction circuitry
  - Optionally program each block as two independent 18 Kb blocks
- High-performance parallel SelectIO technology
  - 1.2 to 3.3V I/O operation
  - Source-synchronous interfacing using ChipSync technology
  - Digitally controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support

- Advanced DSP48E slices
  - 25 x 18, twos complement, multiplication
  - Optional adder, subtracter, and accumulator
  - Optional pipelining
  - Optional bitwise logical functionality
  - Dedicated cascade connections
- Flexible configuration options
  - SPI and Parallel flash interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Auto bus width detection capability
- Off-chip thermal monitoring capability
- Integrated Endpoint blocks for PCI Express
  - Compliant with the PCI Express Base Specification v1.1
  - x1, x4, or x8 lane support per block
  - Works in conjunction with RocketIO transceivers
- Tri-mode 10/100/1000 Mb/s Ethernet MACs
  - RocketIO GTX transceivers can be used as PHY or connect to external PHY using many programmable Media Independent Interface (MII) options
- RocketIO GTX transceivers 150 Mb/s to 4.25 Gb/s
- 65 nm copper CMOS process technology
- 1.0V core voltage

Radiation-Hardness Assurance

The radiation-hardened, space-grade Virtex-5QV FPGAs are guaranteed for total ionizing dose (TID) life and single-event latch-up (SEL) immunity. Extensive single-event upset (SEU) characterization is performed and reported by the Xilinx Radiation Test Consortium (XRTC).

Total Ionizing Dose

Each wafer lot is sampled and tested per Method 1019 to assure that device performance meets or exceeds the guaranteed DC electrical specification requirements, as well as AC and timing parameters at maximum guaranteed total dose levels.

Single-Event Latch-Up

The radiation-hardened Virtex-5QV FPGA technology incorporates a thin epitaxial layer in the wafer manufacturing process for latch-up immunity assurance. The qualified mask set is verified in a heavy ion environment under vacuum, and tested at maximum V_{CC} and maximum operating temperature, to a fluence exceeding 1E8 particles/cm^2.

Single-Event Upset

The Virtex-5QV FPGA incorporates rad-hard-by-design technology to harden storage elements and control logic to SEU. Experiments are conducted in heavy ion and proton environments to measure and document the susceptibility and consequence of SEU(s). An industry consortium oversees and validates the test methods, empirical data collected, and resulting analysis. Conclusions are published on the website as well as international conferences. The Xilinx Radiation Test Consortium reports are available at http://www.xilinx.com/esp/aerospace-defense/space/xrtc.htm.

Table 2 shows the error rates in GEO-Synchronous orbit for the configuration memory cell array and configuration control logic. Additional SEU characterization is available for all user features such as block memory, user registers, DSP blocks, clocking, and I/O structures in the Consortium Report.

Table 2: **Radiation Tolerances**

Symbol	Description	Min	Typical	Max	Units
TID	Total ionizing dose: Method 1019, dose rate 300 rad(Si)/sec	1	–	–	Mrad(Si)
SEL	Single-event latch-up immunity: Heavy ion linear energy transfer (LET) threshold	100	–	–	LET (MeV-cm^2/mg)
SEFI	Single-event functional interrupt GEO 36,000 km typical day	–	2.76E-07	–	Upsets/device/day
SEU_{CFG}	Single-event Upset in Configuration Memory: GEO 36,000 km typical day. Total bits: 35M	–	3.80E-10	–	Upsets/bit/day

Radiation-Hardened By Design Technology

The Virtex-5QV FPGA is built with radiation-hardened by design (RHBD) technology to provide intrinsic hardness from SEU and SET to select elements of the device. For user options and uses of the following features, refer to the Virtex-5QV FPGA User Guide Addendum (contact your local FAE for more information). For complete SEU testing, analysis, and orbital rates, refer to the Consortium Report from the Xilinx Radiation Test Consortium (XRTC) at http://www.xilinx.com/esp/aerospace-defense/space/xrtc.htm.

Configuration Memory RHBD Latches

The Virtex-5QV FPGA configuration memory, which controls all programmable aspects of the device, has been implemented with RHBD dual-node latches that provide nearly 1000 times the SEU hardness of the standard cell latches in the commercial device. Additionally, the RHBD configuration latch is nearly impervious to upset by proton interaction.

Configuration and JTAG Control Logic Hardening

The Virtex-5QV FPGA configuration control logic and JTAG controller have been hardened to SEU and SET with embedded triple module redundancy. Each control register is implemented with independent and redundant error detection and correction circuits for autonomous state correction. This mitigation combination eliminates most single event functional interrupts (SEFIs) and reduced orbital SEFI rates to approximately less than once every 10,000 years in a typical GEO environment.

Configuration Logic Block RHBD User Registers and SET Filters

Each configuration logic block (CLB) in the Virtex-5QV FPGA contains eight user registers. Each register is implemented with RHBD dual-node latches in a *target-initiator* configuration and thus provides the same protection from static SEU as with the configuration latches. Additionally, protection from SET during dynamic operation is provided by transient filters on the inputs of each register. The SET filters provide up to 800 ps of glitch filtration on the data, clock, clock enable, and set/reset input paths of each register.

Input/Output Block RHBD User Registers

The Virtex-5QV FPGA input/output blocks (IOBs) have RBHD dual-node latch registers in all ISERDES, OSERDES, ILOGIC, and OLOGIC blocks. RHBD registers in the IOBs do not have SET filters. Transient filtration is available on CLB registers only. For more information on SelectIO resources, refer to UG190, *Virtex-5 FPGA User Guide*.

Digitally Controlled Impedance Hardening

The Virtex-5QV FPGA digitally controlled impedance (DCI) logic controller is hardened to SEU and SET with embedded triple module redundancy. Each control register is implemented with independent and redundant error detection and correction circuits for autonomous state correction. This mitigation combination provides the first hardened DCI feature. For more information on the DCI feature, refer to UG190, *Virtex-5 FPGA User Guide*.

Integrated Block RAM Embedded Error Detection and Correction

The Virtex-5QV FPGA block RAM contains an integrated ECC and writeback function to autonomously detect and correct SEU in block memory content. The writeback feature delivers high system reliability without the expense of additional support circuitry. For more information on this feature, refer to UG190, *Virtex-5 FPGA User Guide*.

System Blocks within the Virtex-5QV FPGA

Virtex-5QV FPGA Logic

- On average, one speed grade improvement over space-grade Virtex-4QV devices
- Cascadable 32-bit variable shift registers or 64-bit distributed memory capability
- Superior routing architecture with enhanced diagonal routing supports block-to-block connectivity with minimal hops
- Up to 130,000 logic cells including:
  - Up to 87,920 internal fabric flip-flops with clock enable (XQR5VFX130)
  - Up to 87,920 real 6-input LUTs with greater than 5 million total LUT bits
  - Two outputs for dual 5-LUT mode give enhanced utilization
  - Logic expanding multiplexers and I/O registers

Clock Technology

- 450 MHz system performance
- Up to six CMTs
  - Each CMT contains two DCMs and one PLL—up to 18 total clock generators
  - Flexible DCM-to-PLL or PLL-to-DCM cascade
  - Precision clock deskew and phase shift
  - Flexible frequency synthesis
  - Multiple operating modes to ease performance trade-off decisions
  - Improved maximum input/output frequency
  - Fine-grained phase shifting resolution
  - Input jitter filtering
  - Low-power operation
  - Wide phase shift range
- Differential clock tree structure for optimized low-jitter clocking and precise duty cycle
- 32 global clock networks
- Regional, I/O, and local clocks in addition to global clocks

SelectIO Technology

- Up to 836 user I/Os
- Wide selection of I/O standards from 1.2V to 3.3V
- Extremely high performance
  - Up to 800 Mb/s HSTL and SSTL (on all single-ended I/Os)
  - Up to 1.0 Gb/s LVDS (on all differential I/O pairs)
- True differential termination on-chip
- Same edge capture at input and output I/Os
- Extensive memory interface support

Integrated Block Memory

- Up to 360 MHz performance
- Up to 10.5 Mb of integrated block memory, assuming Mb = 2^{20} bits
- 36 Kb blocks with optional dual 18 Kb mode
- True dual-port RAM cells
- Independent port width selection (x1 to x72)
  - Up to x36 total per port for true dual port operation
  - Up to x72 total per port for simple dual port operation (one Read port and one Write port)
  - Memory bits plus parity/sideband memory support for x9, x18, x36, and x72 widths
  - Configurations from 32K x 1 to 512 x 72 (8K x 4 to 512 x 72 for FIFO operation)
- Multirate FIFO support logic
  - Full and Empty flag with fully programmable Almost Full and Almost Empty flags
- Synchronous FIFO support without Flag uncertainty
- Optional pipeline stages for higher performance
- Byte-write capability
- Dedicated cascade routing to form 64K x 1 memory without using FPGA routing
- Integrated optional ECC for high-reliability memory requirements
- Special reduced-power design for 18 Kb (and below) operation

DSP48E Slices

- Up to 360 MHz performance
- 25 x 18 twos complement multiplication
- Optional pipeline stages for enhanced performance
- Optional 48-bit accumulator for multiply accumulate (MACC) operation with optional accumulator cascade to 96 bits
- Integrated adder for complex-multiply or multiply-add operation
- Optional bitwise logical operation modes
- Independent C registers per slice
- Fully cascadable in a DSP column without external routing resources

ChipSync Source-Synchronous Interfacing Logic

- Works in conjunction with SelectIO technology to simplify source-synchronous interfaces
- Per-bit deskew capability built into all I/O blocks (variable delay line on all inputs and outputs)
- Dedicated I/O and regional clocking resources (pins and trees)
- Built-in data serializer/deserializer logic with corresponding clock divider support in all I/Os
- Networking/telecommunication interfaces up to 1.0 Gb/s per I/O

DCI Active I/O Termination

- Optional series or parallel termination
- Temperature and voltage compensation
- Makes board layout much easier
  - Reduces resistors
  - Places termination in the ideal location, at the signal source or destination

Configuration

- Support for platform Flash, standard SPI Flash, or standard parallel NOR Flash configuration
- Bitstream support with dedicated fallback reconfiguration logic
- 256-bit AES bitstream decryption provides intellectual property security and prevents design copying
- Improved bitstream error detection/correction capability
- Auto bus width detection capability
- Partial Reconfiguration via ICAP port

Ruggedized Flip-Chip Packaging

- Optimized packaging technology for proven superior signal integrity
  - Minimized inductive loops from signal to return
  - Optimal signal-to-PWR/GND ratios
- Reduces SSO induced noise by up to 7X compared to wire-bond BGA packages
- Packaging protects against tin whiskering and rugged environments

65 nm Copper CMOS Process

- 1.0V core voltage
- 12-layer metal provides maximum routing capability and accommodates dedicated block immersion
- Triple-oxide technology for proven reduced static power consumption

Integrated Endpoint Block for PCI Express Compliance

- Works in conjunction with RocketIO GTX transceivers to deliver full Endpoint functionality for PCI Express with minimal FPGA logic utilization.
- Compliant with the PCI Express Base Specification v1.1
- Endpoint block for PCI Express or Legacy PCI Express
- x8, x4, or x1 lane width
- Power management support
- Block RAMs used for buffering
- Fully buffered transmit and receive
- Management interface to access PCI Express configuration space and internal configuration
- Supports the full range of maximum payload sizes
- Up to 6 x 32 bit or 3 x 64 bit BARs (or a combination of 32 bit and 64 bit)

Tri-Mode Ethernet Media Access Controller

- Designed to the IEEE Std 802.3-2002
- Operates at 10, 100, and 1,000 Mb/s
- Supports tri-mode auto-negotiation
- Receive address filter (five address entries)
- Fully monolithic 1000BASE-X solution with RocketIO GTX transceivers
- Supports multiple external PHY connections (RGMII, GMII, etc.) interfaces through soft logic and SelectIO resources
- Supports connection to external PHY device through SGMII using soft logic and RocketIO GTX transceivers
- Receive and transmit statistics available through separate interface
- Separate host and client interfaces
- Support for jumbo frames

- Support for VLAN
- Flexible, user-configurable host interface
- Supports IEEE Std 802.3ah-2004 unidirectional mode

RocketIO GTX Transceivers

- Full-duplex serial transceiver capable of 150 Mb/s to 4.25 Gb/s baud rates
- 8B/10B encoding and programmable gearbox to support 64B/66B and 64B/67B encoding, user-defined FPGA logic, or no encoding options
- Channel bonding support
- CRC generation and checking
- Programmable pre-emphasis or pre-equalization for the transmitter
- Programmable termination and voltage swing
- Programmable continuous time equalization for the receiver
- Programmable decision feedback equalization for the receiver
- Receiver signal detect and loss of signal indicator
- User dynamic reconfiguration using secondary configuration bus
- OOB support (SATA)
- Electrical idle, beaconing, receiver detection, and PCI Express spread-spectrum clocking support
- Low-power operation at all line rates

Architectural Description

Virtex-5QV FPGA Array Overview

Virtex-5QV devices are user-programmable gate arrays with various configurable elements and embedded cores optimized for high-density and high-performance system designs. Virtex-5QV devices implement the following functionality:

- I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by programmable I/O blocks (IOBs). The IOBs can be connected to very flexible ChipSync logic for enhanced source-synchronous interfacing. Source-synchronous optimizations include per-bit deskew (on both input and output signals), data serializers/deserializers, clock dividers, and dedicated I/O and local clocking resources.
- Configurable Logic Blocks (CLBs), the basic logic elements for Xilinx® FPGAs, provide combinatorial and synchronous logic as well as distributed memory and SRL32 shift register capability. Virtex-5QV FPGA CLBs are based on real 6-input LUT technology and provide superior capabilities and performance compared to previous generations of programmable logic.
- Block RAM modules provide flexible 36 Kb true dual-port RAM that are cascadable to form larger memory blocks. In addition, Virtex-5QV FPGA block RAMs contain optional programmable FIFO logic for increased device utilization. Each block RAM can also be configured as two independent 18 Kb true dual-port RAM blocks, providing memory granularity for designs needing smaller RAM blocks.
- Cascadable embedded DSP48E slices with 25 x 18 twos complement multipliers and 48-bit adder/subtracter/accumulator provide massively parallel DSP algorithm support. In addition, each DSP48E slice can be used to perform bitwise logical functions.
- CMT blocks provide the most flexible, highest-performance clocking for FPGAs. Each CMT contains two DCM blocks (self-calibrating, fully digital), and one PLL block (self-calibrating, analog) for clock distribution delay compensation, clock multiplication/division, coarse-/fine-grained clock phase shifting, and input clock jitter filtering.
- Integrated Endpoint blocks for PCI Express designs providing x1, x4, or x8 PCI Express Endpoint functionality. When used in conjunction with RocketIO transceivers, a complete Endpoint for PCI Express can be implemented with minimal FPGA logic utilization.

- 10/100/1000 Mb/s Ethernet media-access control blocks offer Ethernet capability.
- GTX transceivers capable of running up to 4.25 Gb/s. Each GTX transceiver supports full-duplex, clock-and-data recovery.

The general routing matrix (GRM) provides an array of routing switches between each internal component. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs. In Virtex-5QV devices, the routing connections are optimized to support CLB interconnection in the fewest number of “hops.” Reducing hops greatly increases post place-and-route (PAR) design performance.

All programmable elements, including the routing resources, are controlled by values stored in static storage elements. These values are loaded into the FPGA during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-5QV FPGA Features

This section briefly describes the features of the Virtex-5QV family of FPGAs.

Input/Output Blocks (SelectIO Resources)

IOBs are programmable and can be categorized as follows:

- Programmable single-ended or differential (LVDS) operation
- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources
- Built-in data serializer/deserializer

The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:

- LVTTL
- LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, and 1.2V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- HSTL 1.2V (Class 1)
- SSTL 1.8V and 2.5V (Class I and II)

The Digitally Controlled Impedance (DCI) I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support these differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- HyperTransport™ technology
- Differential HSTL 1.5V and 1.8V (Class I and II)
- Differential SSTL 1.8V and 2.5V (Class I and II)
- RSDS (2.5V point-to-point)

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a range of signal delays. This is especially useful for synchronizing signal edges in source-synchronous interfaces.

General-purpose I/O in select locations (eight per bank) are designed to be “regional clock capable” I/O by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

Data serializer/deserializer capability is added to every I/O to support source-synchronous interfaces. A serial-to-parallel converter with associated clock divider is included in the input path, and a parallel-to-serial converter in the output path.

An in-depth guide to the Virtex-5QV FPGA IOB is found in UG194, *Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide*.

Configurable Logic Blocks

A Virtex-5QV FPGA CLB resource is made up of two slices. Each slice is equivalent and contains:

- Four function generators
- Four storage elements
- Arithmetic logic gates
- Large multiplexers
- Fast carry look-ahead chain

The function generators are configurable as 6-input LUTs or dual-output 5-input LUTs. SLICEMs in some CLBs can be configured to operate as 32-bit shift registers (or 16-bit x 2 shift registers) or as 64-bit distributed RAM. In addition, the four storage elements can be configured as either edge-triggered D-type flip-flops or level sensitive latches. Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

The Virtex-5QV FPGA CLBs are further discussed in UG190, *Virtex-5 FPGA User Guide*.

Block RAM

The 36 Kb true dual-port RAM block resources are programmable from 32K x 1 to 512 x 72, in various depth and width configurations. In addition, each 36 Kb block can also be configured to operate as two, independent 18-Kb dual-port RAM blocks.

Each port is totally synchronous and independent, offering three “read-during-write” modes. Block RAM is cascadable to implement large embedded storage blocks. Additionally, backend pipeline registers, clock control circuitry, built-in FIFO support, ECC, and byte write enable features are also provided as options.

The block RAM feature in Virtex-5QV devices is further described in UG190,*Virtex-5 FPGA User Guide*.

Global Clocking

The CMTs and global-clock multiplexer buffers provide a complete solution for designing high-speed clock networks.

Each CMT contains two DCMs and one PLL. The DCMs and PLLs can be used independently or extensively cascaded. Up to six CMT blocks are available, providing up to 18 total clock generator elements.

Each DCM provides familiar clock generation capability. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90°, 180°, and 270° phase-shifted versions of the output clocks. Fine-grained phase shifting offers higher-resolution phase adjustment with fraction of the clock period increments. Flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency.

To augment the DCM capability, Virtex-5QV FPGA CMTs also contain a PLL. This block provides reference clock jitter filtering and further frequency synthesis options.

Virtex-5QV devices have 32 global-clock MUX buffers. The clock tree is designed to be differential. Differential clocking helps reduce jitter and duty cycle distortion.

DSP48E Slices

DSP48E slice resources contain a 25 x 18 twos complement multiplier and a 48-bit adder/subtracter/accumulator. Each DSP48E slice also contains extensive cascade capability to efficiently implement high-speed DSP algorithms.

The Virtex-5QV FPGA DSP48E slice features are further discussed in UG193, *Virtex-5 FPGA XtremeDSP Design Considerations User Guide*.

Routing Resources

All components in Virtex-5QV devices use the same interconnect scheme and the same access to the global routing matrix. In addition, the CLB-to-CLB routing is designed to offer a complete set of connectivity in as few hops as possible. Timing models are shared, greatly improving the predictability of the performance for high-speed designs.

Boundary Scan

Boundary-Scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-5QV devices, complying with IEEE standards 1149.1 and 1532.

Configuration

Virtex-5QV devices are configured by loading the bitstream into internal configuration memory using one of these modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE Std 1532 and 1149)
- SPI mode (Serial Peripheral Interface standard Flash)
- BPI-up/BPI-down modes (Byte-wide Peripheral interface standard x8 or x16 NOR Flash)

In addition, Virtex-5QV devices also support these configuration options:

- 256-bit AES bitstream decryption for IP protection
- Multi-bitstream management (MBM) for cold/warm boot support
- Parallel configuration bus width auto-detection
- Parallel daisy chain
- Configuration CRC and ECC support for the most robust, flexible device integrity checking

Virtex-5QV device configuration is further discussed in UG191, *Virtex-5 FPGA Configuration Guide*.

Tri-Mode (10/100/1000 Mb/s) Ethernet MACs

Virtex-5QV devices contain up to eight embedded Ethernet MACs, two per Ethernet MAC block. The blocks have the following characteristics:

- Designed to the IEEE Std 802.3-2002 specification
- UNH-compliance tested
- RGMII/GMII Interface with SelectIO or SGMII interface when used with RocketIO GTX transceivers
- Half or full duplex
- Supports Jumbo frames
- 1000BASE-X PCS/PMA: When used with RocketIO GTX transceivers, can provide complete 1000BASE-X implementation on-chip
- DCR-bus connection to microprocessors

Integrated Endpoint Blocks for PCI Express

Virtex-5QV devices contain up to four integrated Endpoint blocks. These blocks implement Transaction Layer, Data Link Layer, and Physical Layer functions to provide complete PCI Express Endpoint functionality with minimal FPGA logic utilization. The blocks have the following characteristics:

- Compliant with the PCI Express Base Specification 1.1
- Works in conjunction with GTX transceivers to provide complete endpoint functionality
- 1, 4, or 8 lane support per block

RocketIO GTX Transceivers

Eight to 24 channel RocketIO GTX transceivers are capable of running 150 Mb/s to 4.25 Gb/s.

- Full Clock and Data Recovery
- 8/16/32-bit or 10/20/40-bit datapath support
- Optional 8B/10B encoding, gearbox for programmable 64B/66B or 64B/67B encoding, or FPGA-based encode/decode
- Integrated FIFO/Elastic Buffer
- Channel bonding and clock correction support
- Dual embedded 32-bit CRC generation/checking
- Integrated programmable character detection
- Programmable de-emphasis (also known as transmitter equalization)
- Programmable transmitter output swings
- Programmable receiver equalization
- Programmable receiver termination
- Embedded support for:
  - Serial ATA: OOB signalling
  - PCI Express: Beaconing, electrical idle, and receiver detection
- Built-in PRBS generator/checker

Virtex-5QV FPGA RocketIO GTX transceivers are further discussed in UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*. All performance values in this document supersede those in the *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Intellectual Property Cores

Xilinx offers IP cores for commonly used complex functions including DSP, bus interfaces, processors, and processor peripherals. Using Xilinx LogiCORE™ products and cores from third party AllianceCORE participants, customers can shorten development time, reduce design risk, and obtain superior performance for their designs. Additionally, the CORE Generator™ system allows customers to implement IP cores into Virtex-5QV FPGAs with predictable and repeatable performance. It offers a simple user interface to generate parameter-based cores optimized for our FPGAs.

The System Generator for DSP tool allows system architects to quickly model and implement DSP functions using handcrafted IP and features an interface to third-party system level DSP design tools. System Generator for DSP implements many of the high-performance DSP cores supporting Virtex-5QV FPGAs including the Xilinx Forward Error Correction Solution with Interleaver/De-interleaver, Reed-Solomon encoder/decoders, and Viterbi decoders. These are ideal for creating highly-flexible, concatenated codecs to support the communications market.

Using Virtex-5QV FPGA RocketIO transceivers, industry-leading connectivity and networking IP cores include leading-edge PCI Express, Serial RapidIO, Fibre Channel, and 10 Gb Ethernet cores can be implemented. The Xilinx SPI-4.2 IP core utilizes Virtex-5QV FPGA ChipSync technology to implement dynamic phase alignment for high-performance source-synchronous operation. Xilinx also provides PCI cores for advanced system-synchronous operation.

The MicroBlaze™ 32-bit processor core provides the industry's fastest soft processing solution for building complex systems for the networking, telecommunication, data communication, embedded, and consumer markets. The MicroBlaze processor features a RISC architecture with Harvard-style separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory. A standard set of peripherals are also CoreConnect enabled to offer MicroBlaze processor designers compatibility and reuse.

All IP cores for Virtex-5QV FPGAs are found on the Xilinx IP Center Internet portal presenting the latest intellectual property cores and reference designs using Smart Search for faster access.

Virtex-5 FPGA LogiCORE Endpoint Block Plus Wrapper for PCI Express

This is the recommended wrapper to configure the integrated Endpoint block for PCI Express delivered through the CORE Generator system. It provides many ease-of-use features and optimal configuration for Endpoint application simplifying the design process and reducing the time-to-market. Access to the core, including bitstream generation capability can be obtained through registration at no extra charge.

Application Notes and Reference Designs

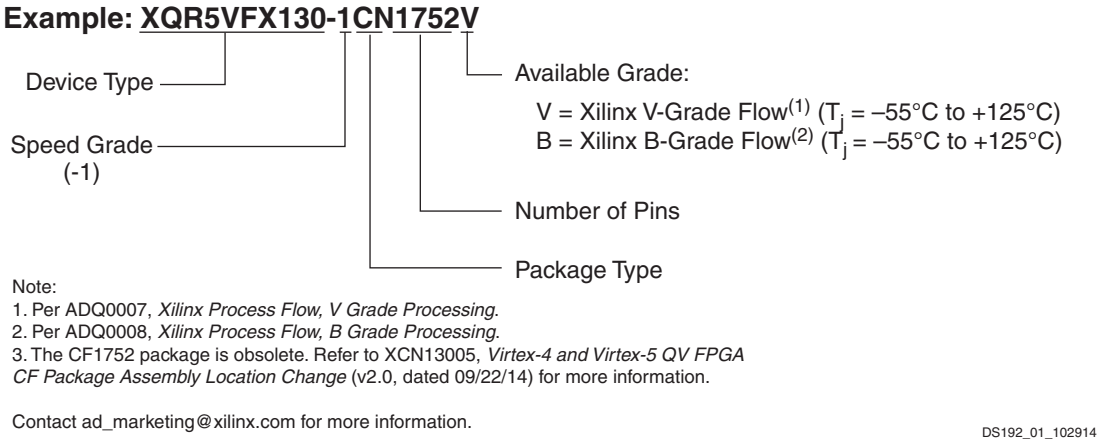
Refer to the Xilinx website for application notes and reference designs written specifically for the Virtex-5QV family.

Virtex-5QV Device and Package Combinations and Maximum I/Os

Table 3: **Virtex-5QV Device and Package Combinations and Maximum Available I/Os**

Package	CF1752 and CN1752	
Size (mm)	45 x 45	
Device	GTX Transceivers	I/O
XQR5VFX130	18	836

Virtex-5QV FPGA Ordering Information



Note:
1. Per ADQ0007, *Xilinx Process Flow, V Grade Processing*.
2. Per ADQ0008, *Xilinx Process Flow, B Grade Processing*.
3. The CF1752 package is obsolete. Refer to XCN13005, *Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change* (v2.0, dated 09/22/14) for more information.

Contact ad_marketing@xilinx.com for more information.

Figure 1: **Virtex-5QV FPGA Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/19/10	1.0	Initial Xilinx release.
08/30/10	1.1	Updated Radiation-Hardness Assurance introduction.
07/11/11	1.2	Updated the data sheet to Preliminary Product Specification on page 1 and revised General Description for overall clarity. Revised dose rate latch-up immunity on page 2. Updated TID to 1 Mrad(Si) throughout data sheet including Table 2. Updated the Integrated Block Memory performance section. Corrected the size of the package in Table 3. Updated Notice of Disclaimer.
03/08/12	1.3	Updated the overview to Product Specification on page 1. Updated max GTX transceiver speed to 4.25 Gb/s throughout overview. Updated Table 2, Virtex-5QV FPGA Logic, SelectIO Technology, ChipSync Source-Synchronous Interfacing Logic, and Figure 1.
11/12/14	1.4	Updated Table 3 and Figure 1.

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Virtex-5QV FPGA Documentation

Complete and up-to-date documentation of the Virtex-5 family of FPGAs is available on the Xilinx website. In addition to the most recent *Radiation-Hardened, Space-Grade Virtex-5QV Device Overview*, these files are also available for download:

Radiation-Hardened, Space-Grade Virtex-5QV FPGA Data Sheet: DC and Switching Characteristics (DS692)

This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5QV device.

Virtex-5QV FPGA Packaging and Pinout Specification (UG520)

This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

Virtex-5 FPGA User Guide (UG190)

This guide includes chapters on:

- Clocking Resources
- Clock Management Technology (CMT)
- Phase-Locked Loops (PLL)
- Block RAM
- Configurable Logic Blocks (CLBs)
- SelectIO Resources
- SelectIO Logic Resources
- Advanced SelectIO Logic Resources

Virtex-5 FPGA XtremeDSP Design Considerations User Guide (UG193)

This guide describes the DSP48E slice and includes reference designs for using DSP48E math functions and various filters.

Virtex-5 FPGA Configuration Guide (UG191)

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, Boundary-Scan and JTAG configuration, and reconfiguration techniques.

Virtex-5 FPGA PCB Designer's Guide (UG203)

This guide provides information on PCB design for Virtex-5QV devices, with a focus on strategies for making design decisions at the PCB and interface level.

Virtex-5 FPGA RocketIO GTX Transceiver User Guide (UG198)

This guide describes the RocketIO GTX transceivers available in the Virtex-5QV FPGAs.

Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide (UG194)

This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5QV FPGAs.

Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide (UG197)

This guide describes the integrated Endpoint blocks in the Virtex-5QV FPGAs that are PCI Express compliant.