Agilent Trace Core 2 (ATC2) (v1.04a)

DS650 June 22, 2011 **Product Specification**

Introduction

The Agilent Trace Core 2 (ATC2) is a customizable debug capture core that is specially designed to work with the latest generation logic analyzers from Agilent Technologies. The ATC2 core provides external Agilent logic analyzers access to internal FPGA design nets.

Features

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IP Facts Table					
Core Specifics					
Supported Device Family (1)	Kintex™-7(2), Virtex®-7(2), Virtex-6(3), Virtex-5, Virtex-4, Spartan®-6(4), Spartan-3/XA, Spartan-3A/3AN/3A DSP/XA, Spartan-3E/XA				
Supported User Interfaces	Not applicable.				
Provided with Core					
	Resources				**Frequency**
Configuration (5)	LUTs	FFs	DSP Slices	Block RAMs	Max Freq
Configuration 1	108	77	0	0	196.336 MHz
Configuration 2	1536	145	0	0	227.40 MHz
Configuration 3	267	107	0	0	195.261 MHz
Documentation	Product Specification, User Guide				
Design Files	Netlist				
Example Design	Verilog/VHDL				
Test Bench	Not Provided				
Constraints File	Xilinx Constraints File				
Simulation Model	Not Provided				
Additional Items	Signal Description File (.cdc)				
Tested Design Tools (6)					
Design Entry Tools	CORE Generatror tool, System Generator, XPS				
Simulation	Not provided				
Synthesis Tools	Not provided				
Support					
Provided by Xilinx, Inc.					

Notes:

1. For a complete listing of supported devices, see the release notes for this core.
2. For more information, see DS180 7 Series FPGAs Overview.
3. For more information, see the DS150 Virtex-6 Family Overview Product Specification.
4. For more information, see DS160 Spartan-6 Family Overview Product Specification.
5. For configuration details, see Table 4, page 8.
6. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Applications

The ATC2 core is designed to be used in any application that requires verification or debugging using the ChipScope Pro software and an external Agilent Logic Analyzer.

Functional Description

Communication with the ATC2 core is conducted using a connection to the JTAG port via the ICON core, as shown in Figure 1.

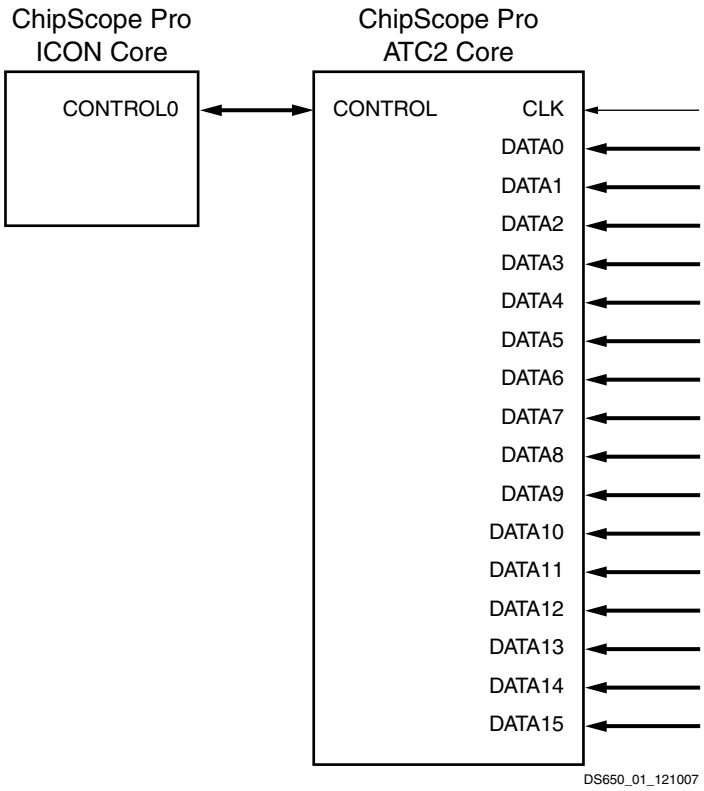

Figure 1: **ATC2 Core Connection to ICON Core**

The data path of the ATC2 core consists of:

- Up to 64 run-time selectable input signal banks that connect to the user's FPGA design.
- Up to 128 output data pins that connect to an Agilent logic analyzer's probe connectors.
- Optional 2x time-division multiplexing (TDM) available on each output data pin that can be used to double the width of each individual signal bank from 128 to 256 bits.
- Supports both asynchronous timing and synchronous state capture modes.
- Supports any valid I/O standard, drive strength, and output slew rate on each output data pin on an individual pin-by-pin basis.
- Supports any Agilent Technologies probe connection technology.

The maximum number of data probe points available at run time is calculated as:

(64 data ports) * (128 bits per data port) * (2x TDM) = 16,384 probe points.

Core Data Capture and Run-Time Control

The external Agilent logic analyzer is used to trigger on and capture the data that passes through the ATC2 core. which allows the user to take full advantage of the complex triggering, deep trace memory, and system-level data correlation features of the Agilent logic analyzer. In addition, the analyzer provides increased visibility of internal design nodes provided by the ATC2 core and is also used to control the run-time selection of the active data port by communicating with the ATC2 core via a JTAG port connection.

CORE Generator

The CORE Generator tool provides the ability to define and generate a customized ATC2 core for adding external Agilent logic analyzer capture capabilities to the HDL designs. The user can customize the number of pins (and their characteristics) to be used for external capture as well as how many input data ports are needed. The user can also customize the type of capture mode (state or timing) to be used as well as the TDM compression mode (1x or 2x).

After the CORE Generator tool validates the parameters you defined, it generates an XST netlist (*.ngc) and other files specific to the HDL language and synthesis tool associated with the CORE Generator project. The can easily generate the netlist and code examples for use in normal FPGA design flows.

In the Debug & Verification > ChipScope Pro IP category of the Xilinx CORE Generator tool, select ATC2 (ChipScope Pro - Agilent Trace Core 2) and click the Customize and Generate link in the right side of the window.

ATC2 Core Acquisition and State Parameters

The CORE Generator tool is used to set up the ATC2 core acquisition and state parameters.

Entering the Component Name

The Component Name field can consist of any combination of alpha-numeric characters in addition to the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Generating an Example Design

The ATC2 core generator normally generates standard Xilinx CORE Generator output files only, such as netlist and instantiation template files. If, in addition, you want the Xilinx CORE Generator tool to generate an example design that uses the ATC2 core, select the Generate Example Design checkbox. The example design contains everything necessary to implement the design, including source code and implementation script files.

Selecting the Acquisition Mode

The acquisition mode of the ATC2 core can be set to either to Timing - Asynchronous Sampling mode for asynchronous data capture or State - Synchronous Sampling mode for synchronous data capture to the CLK input signal. In State mode, the data path through the ATC2 core uses pipeline flip-flops that are clocked on the CLK input port signal. In Timing mode, the data path through the ATC2 core is composed purely of combinational logic all the way to the output pins. Also, in Timing mode, the ATCK pin is used as an extra data pin.

Max Frequency Range

The Max Frequency Range parameter is used to specify the maximum frequency range in which you expect to operate the ATC2 core. The implementation of the ATC2 core will be optimized for the maximum frequency range selection. The valid maximum frequency ranges are 0-100 MHz, 101-200 MHz, 201-300 MHz, and 301-500 MHz. The maximum frequency range selection only has an affect on core implementation when the acquisition mode is set to State - Synchronous Sampling.

TDM Rate

The ATC2 core does not use on-chip memory resources to store the captured trace data. Instead, it transmits the data to be captured by an Agilent logic analyzer that is attached to the FPGA pins using a special probe connector. The data can be transmitted out the device pins at the same rate as the incoming DATA port (TDM Rate = 1x) or twice the rate as the DATA port (TDM Rate = 2x). The TDM rate can be set to "2x" only when the acquisition mode is set to State - Synchronous Sampling.

ATC2 Core Pin and Signal Parameters

After you have set up the ATC2 core acquisition and state parameters, click Next. This takes you to the screen in the CORE Generator tool that is used to set up the ATC2 pin and signal parameters.

Enable Auto Setup

The Enable Auto Setup option is used to enable a feature that allows the Agilent Logic Analyzer to automatically set up the appropriate ATC2 pin to Logic Analyzer pod connections. This feature also allows the Agilent Logic Analyzer to automatically determine the optimal phase and voltage sampling offsets for each ATC2 pin. This feature is enabled by default.

Enable Always On Mode

The Enable Always On Mode parameter forces an ATC2 core always to enable its internal logic and output buffers. The "Always On" mode ensures that signal bank 0 is driven out to the ATD pins upon FPGA device configuration. This mode makes it possible to capture events that immediately follow device configuration without having to first set up the ATC2 core manually. This feature is disabled by default and is only available when the acquisition mode is set to Timing - Asynchronous Sampling mode.

ATD Pin Count

The ATC2 core can implement any number of ATD output pins in the range of 4 through 64.

Driver Endpoint Type

The Driver Endpoint Type setting is used to control whether single-ended or differential output drivers are used on the ATCK and ATD output pins. All ATCK and ATD pins must use the same driver endpoint type.

Pin Edit Mode

The pin edit mode is a time saving feature that allows you to change the IO Standard, Drive and Slew Rate pin parameters on individual pins or together as a group of pins. Selecting ATD drivers same as ATCK allows you to change the ATCK pin parameters and forces all ATD pins to the same settings. Selecting ATD drivers different than ATCK allows you to edit the parameters of each pin independently from one another. You need to set unique pin locations for each individual pin regardless of the Pin Edit Mode parameter setting.

Signal Bank Count

The ATC2 core contains an internal, run-time selectable data signal bank multiplexer. The Signal Bank Count setting is used to denote the number of data input ports or signal banks the multiplexer will implement. The valid Signal Bank Count values are 1, 2, 4, 8, 16, 32, and 64.

Signal Bank Width

The width of each input signal bank data port of the ATC2 core depends on the capture mode and the TDM rate. In State mode, the width of each signal bank data port is equal to (ATD pin count) * (TDM rate). In Timing mode, the

width of each signal bank data port is equal to (ATD pin count + 1) * (TDM rate) since the ATCK pin is used as an extra data pin.

ATC2 Core ATCK and ATD Pin Parameters

After you have set up the ATC2 core pin and signal parameters, click Next. This takes you to the screen in the CORE Generator tool that is used to set up the ATCK and ATD pin parameters.

The output clock (ATCK) and data (ATD) pins are instantiated inside the ATC2 core for your convenience. This means that although you do not have to manually bring the ATCK and ATD pins through every level of hierarchy to the top-level of your design, you do need to specify the location and other characteristics of these pins in the CORE Generator. These pin attributes are then added to the *.ncf file of the ATC2 core. Using the settings in the Pin Parameters table, you can control the location, I/O standard, output drive and slew rate of each individual ATCK and ATD pin.

Pin Name

The ATC2 core has two types of output pins: ATCK and ATD. The ATCK pin is used as a clock pin when the capture mode is set to State and is used as a data pin when the capture mode is set to Timing. The ATD pins are always used as data pins. The names of the pins cannot be changed.

Pin Loc

The Pin Loc column is used to set the location of the ATCK or ATD pin.

IO Standard

The IO Standard column is used to set the I/O standard of each individual ATCK or ATD pin. The I/O standards that are available for selection depend on the device family and driver endpoint type. The names of the I/O standards are the same as those in the IOSTANDARD section of the Constraints Guide in the Xilinx Software Documentation.

Drive

The Drive column setting denotes the maximum output drive current of the pin driver and ranges from 2 to 24 mA, depending on the IO Standard selection.

Slew Rate

The Slew Rate column can be set to either FAST or SLOW for each individual ATCK or ATD pin.

Generating the Core

After entering the ATC2 core parameters, click Finish to create the ATC2 core files. While the ATC2 core is being generated, a progress indicator appears. Depending on the host computer system, it might take several minutes for the ATC2 core generation to complete. After the ATC2 core has been generated, a list of files that are generated will appear in a separate Readme File window.

Using the ATC2 Core

To instantiate the example ATC2 core HDL files into your design, use the following guidelines to connect the ATC2 core port signals to various signals in your design:

- Connect the ATC2 core's CONTROL port signal to an unused control port of the ICON core instance in the design
- Connect all unused bits of the ATC2 core's asynchronous and synchronous input signals to a "0". This prevents the mapper from removing the unused trigger and/or data signals and also avoids any DRC errors during the implementation process
- For best results, make sure the State mode input data port signals are synchronous to the ATC2 clock signal (CLK); this is not important for Timing mode input data port signals.

Ports and Parameters

Ports

The ATC2 Interface ports are listed and described in Table 1.

Table 1: **ATC2 Interface Ports**

Port Name	Direction	Description
CLK	IN	Design clock needed to synchronize the data in state mode. Optional (depends on state_synchronous parameter).
CONTROL[35:0]	INOUT	Control bus to ICON core. Mandatory.
DATA<*n*>[<*m*>-1:0]	IN	Data signal input bank number <*n*> of width <*m*>. Optional, except for <*n*> = 0, which is mandatory (depends on parameter signal_bank_count = <*n*>+1, where <*n*> ranges from 0 through 63).

Parameters

The ATC2 XCO parameters are listed and described in Table 2

Table 2: **ATC2 XCO Parameters**

Parameter Name	Allowable Values	Default Value	Description
atck_drive	N/A	N/A	Drive strength for ATCK pin.
atck_io_standard	N/A	N/A	IO standard for ATCK pin.
atck_pin_loc	any alphanumeric	none	Pin location for ATCK pin.
atck_slew_rate	fast, slow	fast	slew rate for ATCK pin.
atd_drivers	same_as_atck, different_than_atck	same_as_atck	Whether to use atck settings for all data pins (same_as_atck) or individual settings for data pins (different_than_ atck)
atd_pin_count	4-64	8	Number of data pins to use.
atd<*n*>_drive	N/A	N/A	Drive strength for data pin <*n*>.
atd<*n*>_io_standard	N/A	N/A	IO standard for data pin <*n*>.
atd<*n*>_pin_loc	any alphanumeric	none	Pin location for data pin <*n*>.
atd<*n*>_slew_rate	fast, slow	fast	slew rate for data pin <*n*>.

XCO Parameters

The ATC2 XCO parameters are displayed in Table 3.

Table 3: **ATC2 XCO Parameters**

Parameter Name	Allowable Values	Default Value	Description
atck_drive	N/A (1)	N/A (1)	Drive strength for ATCK pin.
atck_io_standard	N/A (1)	N/A (1)	IO standard for ATCK pin.
atck_pin_loc	any alphanumeric	none	Pin location for ATCK pin.
atck_slew_rate	fast, slow	fast	slew rate for ATCK pin.
atd_drivers	same_as_atck, different_than_atck	same_as_atck	Whether to use atck settings for all data pins (same_as_atck) or individual settings for data pins (different_than_atck)
atd_pin_count	4-64	8	Number of data pins to use.
atd<*n*>_drive	N/A (1)	N/A (1)	Drive strength for data pin <*n*>.
atd<*n*>_io_standard	N/A (1)	N/A (1)	IO standard for data pin <*n*>.
atd<*n*>_pin_loc	any alphanumeric	none	Pin location for data pin <*n*>.
atd<*n*>_slew_rate	fast, slow	fast	slew rate for data pin <*n*>.
component_name	String with A-z, 0-9, and _ (underscore)	atc2	Name of component instance.
driver_endpoint_type	single-ended, differential	single-ended	Type of output driver to use. Applies to all pins.
enable_always_on_mode	true, false	false	Enables measurement immediately after FPGA configuration.
enable_auto_setup	true, false	true	Include circuitry that will use a test pattern to properly align the data.
max_frequency_range	0-100_mhz, 101-200_mhz, 201-300_mhz, 301-500_mhz	0-100_mhz	Sets the core operating range. This is used in generating the core and during instrument setup.
signal_bank_count	1, 2, 4, 8, 16, 32, 64	1	Number of signal banks.
tdm_rate	1x, 2x	1x	Time Division Multiplexing rate, either 1x at design speed or 2x multiplexing.

Notes:

1. The I/O standards available will be different depending on the selected FPGA device family. Refer to the data sheet of the appropriate FPGA device family for details. Also, different drive strength selections are available based on the selected I/O standard.

Restrictions

A maximum of 15 ATC2 cores can be used in a single design.

Performance and Resource Utilization

The configuration number and associated device is shown in Table 4.

Table 4: **Configuration Details**

Configuration Number	Device	Description
Config1	Xc7v585t-2ffg1157	Signal Bank count - 2, pin count -8
Config2	Xc7v585t-3ffg1157	Signal Bank count - 64, pin count -64
Config3	Xc7v585t-2ffg1157	Signal Bank count - 16, pin count -32

Verification

Xilinx has verified the ATC2 core in a proprietary test environment, using an internally developed bus functional model.

References

1. More information on the ChipScope Pro software and cores is available in the Software and Cores User Guide, located at http://www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE® Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Embedded Edition software (EDK).

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	1.0	Release 10.1 (Initial Xilinx release).
04/25/08	1.1	Release 10.1, Service Pack 1 changes.
09/19/08	1.2	Release 10.1, Service Pack 3 changes.
04/07/09	2.0	Release 11.1
06/24/09	2.1	Release 11.2
6/22/11	2.2	Updated to v1.04a for the 13.2 release.

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