Video Broadcaster v1.00a

DS880 October 16, 2012 **Product Specification**

Introduction

The Xilinx LogiCORE™ IP Video Broadcaster core provides a flexible block for replicating a single inbound AXI4-Stream interface into multiple outbound AXI4-Stream interfaces. Support for up to 16 outbound AXI4-Stream interfaces is provided. AXI4-Stream data widths from 8 to 64 are also supported.

Features

- AXI4-Stream data interfaces with Video protocol support
- Configurable for up to 16 outbound video interfaces
- Supports `tdata` width from 8 to 64, in 8-bit increments

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000 (2), Artix™-7, Virtex®-7, Kintex™-7, Virtex-6, Spartan®-6
Supported User Interfaces	AXI4-Stream(3)
Resources	N/A
Provided with Core	
Design Files	Verilog Source Code
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Verilog Source Code
Supported S/W Driver(4)	N/A
Tested Design Flows(5)	
Design Entry	ISE Design Suite Embedded Edition v14.3
Simulation	Mentor Graphics ModelSim, Xilinx® ISim
Synthesis	Xilinx Synthesis Technology (XST)
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see Embedded Edition Derivative Device Support.
2. Supported in ISE Design Suite implementations only.
3. Video protocol as defined in the *Video IP: AXI Feature Adoption* section of (UG761) *AXI Reference Guide* [Ref 1].
4. Standalone driver details can be found in the EDK or SDK directory (<*install_directory*>/doc/usenglish/xilinx_drivers.htm). Linux OS and driver support information is available from //wiki.xilinx.com.
5. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The Video Broadcaster core simply replicates all the inbound traffic to the core onto the multiple outbound interfaces as shown in Figure 1.

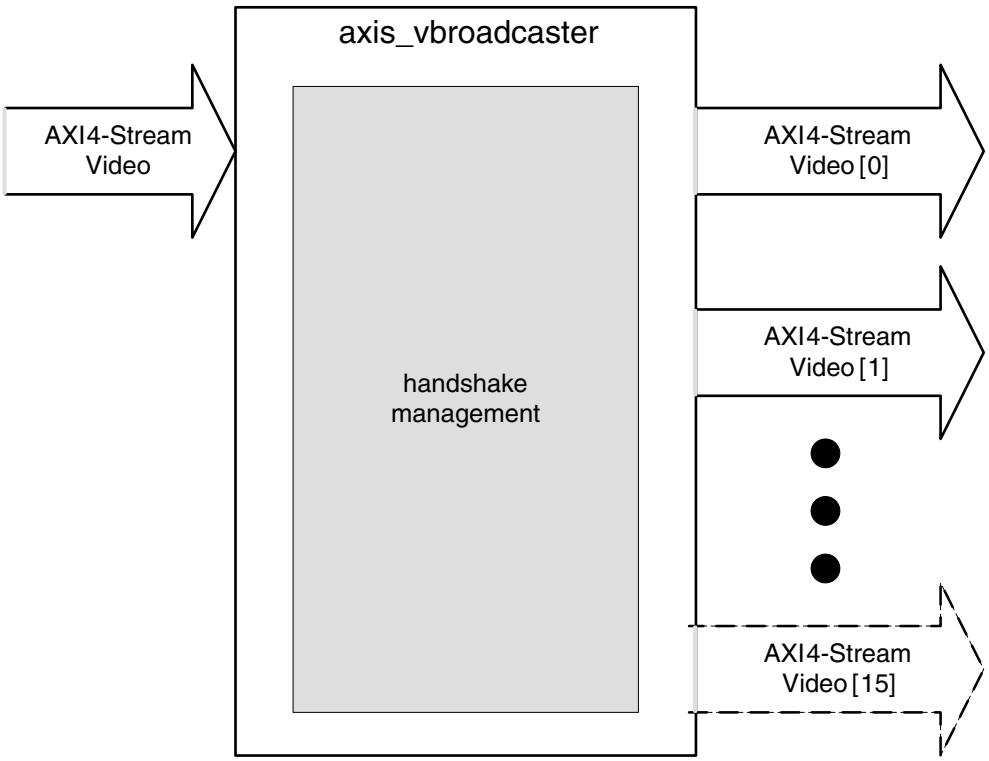

Figure 1: **Video Broadcaster Core**

The Video Broadcaster core is compliant with the AXI4-Stream Video Protocol standard. Refer to the *Video IP: AXI Feature Adoption* section of the *AXI Reference Guide (UG761)* [Ref 1]for additional information.

Applications

- AXI4-Stream Video Protocol channel replication

Functional Description

The Video Broadcaster core performs handshake management and ensures that all the outbound interfaces have completed their `TREADY/TVALID` handshakes before completing the inbound handshake as shown in Figure 2.

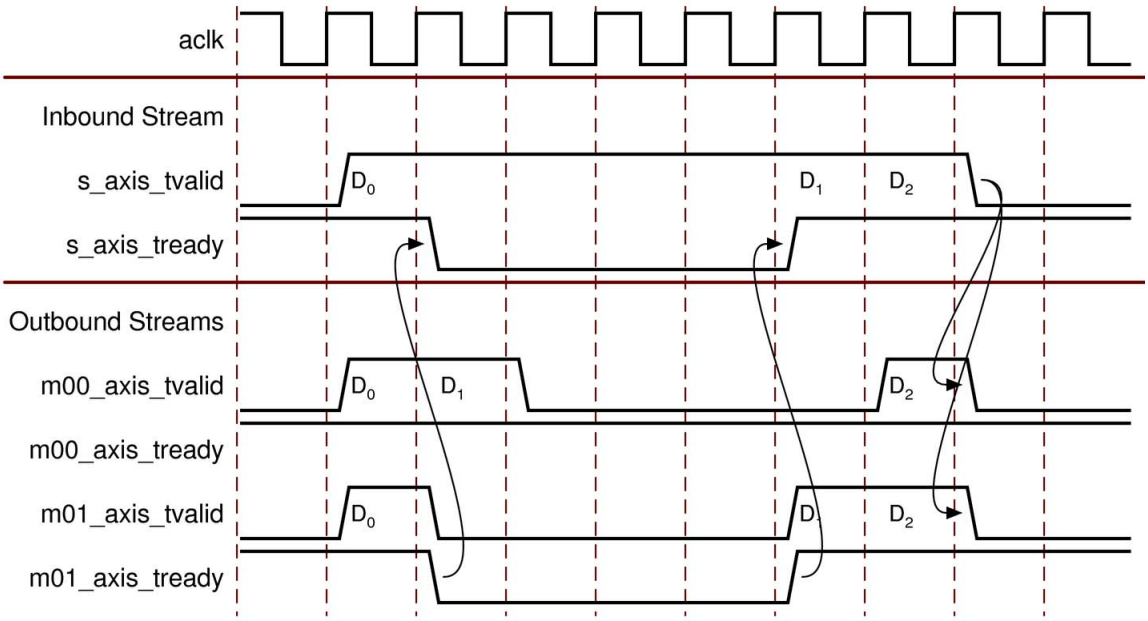

Figure 2: **Handshake Management**

Latency

The Video Broadcaster core has a combinational inbound valid to outbound valid path and no latency is introduced. When not all outbound interfaces are ready, inbound back pressure is applied.

Throughput

The Video Broadcaster core reduces throughput relative to the inbound and outbound channels. It throttles the inbound channel based on the outbound availability. If all outbound channels are always ready, there is not any reduction in throughput.

Parameterization

Table 1 describes the core parameters.

Table 1: **Video Broadcaster Parameters**

Parameter Name	Default Value	Allowable Values	Description
C_AXIS_TDATA_WIDTH	32	8,16,24,32,40,48,56,64	Width of the each of the TDATA ports
C_NUM_MI_SLOTS	2	2 - 16	Number of Video Master slots on which the inbound video is replicated.

Core Interfaces

Port Descriptions

The Video Broadcaster core is compliant with the AXI4-Stream Video Protocol standard. Figure 3 illustrates an I/O diagram of the Video Broadcaster core.

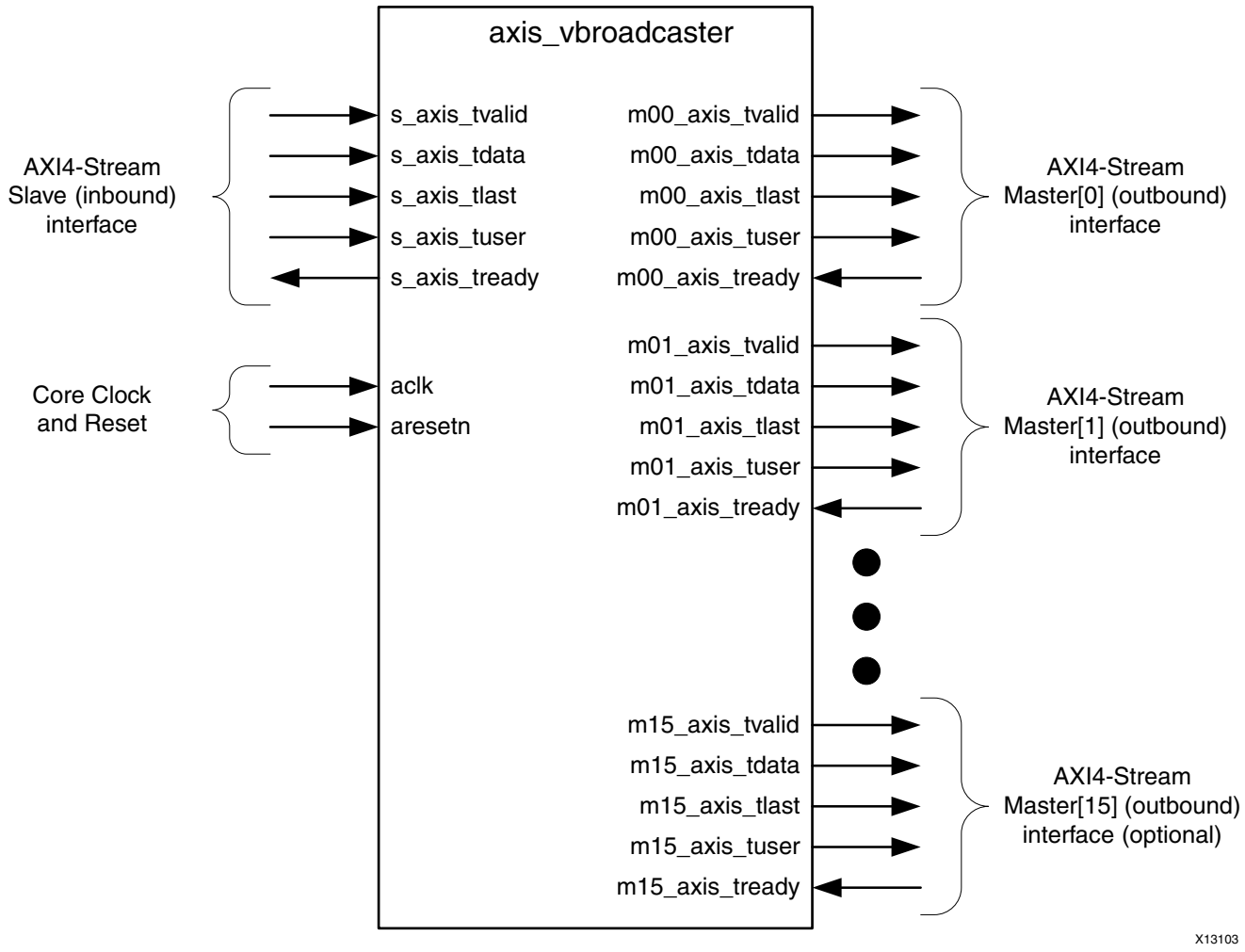

Figure 3: **Video Broadcaster Core Top-Level Signaling Interface**

Common Interface Signals

Table 2 summarizes the signals which are either shared by, or not part of the dedicated AXI4-Stream data control interfaces.

Table 2: **Common Interface Signals**

Signal Name	Direction	Width	Description
aclk	In	1	Video core clock
aresetn	In	1	Video core Active Low synchronous reset

The `aclk` and `aresetn` signals are shared between the core and the AXI4-Stream data interfaces.

aclk

The AXI4-Stream interface must be synchronous to the core clock signal `aclk`. All AXI4-Stream interface's input signals are sampled on the rising edge of `aclk`. All AXI4-Stream output signal's changes occur after the rising edge of `aclk`.

aresetn

The aresetn signal must be synchronous to the aclk and must be held low for a minimum of 32 clock cycles of the slowest clock.

Data Interface

The Video Broadcaster core receives and transmits data using AXI4-Stream interfaces that implement a video protocol as defined in the *Video IP: AXI Feature Adoption* section of the *AXI Reference Guide (UG761)* [Ref 1].

AXI4-Stream Signal Names and Descriptions

Table 3 describes the AXI4-Stream inbound signal names and descriptions.

Table 3: **AXI4-Stream Data Interface Signal Descriptions**

Signal Name	Direction	Width	Description
s_axis_tdata	In	8,16,24,32,40,48,56,64	Input Video Data
s_axis_tvalid	In	1	Input Video Valid Signal
s_axis_tready	Out	1	Input Ready
s_axis_tuser	In	1	Input Video Start Of Frame
s_axis_tlast	In	1	Input Video End Of Line

Table 4 describes the AXI4-Stream outbound signal names and descriptions.

Table 4: **AXI4-Stream Data Interface Signal Descriptions**

Signal Name	Direction	Width	Description
m[nn]_axis_tdata	Out	8,16,24,32,40,48,56,64	Interface [nn] Output Video Data
m[nn]_axis_tvalid	Out	1	Interface [nn] Output Video Valid
m[nn]_axis_tready	In	1	Interface [nn] Output Video Ready
m[nn]_axis_tuser	Out	1	Interface [nn] Output Video Start of Frame
m[nn]_axis_tlast	Out	1	Interface [nn] Output Video End of Line

Note: The number of outbound interfaces is configurable via the C_NUM_MI_SLOTS parameter. Each of the outbound interfaces must be identical and the "[nn]" designation indicates the port.

Video Data

The AXI4-Stream interface specification restricts TDATA widths to integer multiples of 8 bits. The Video Broadcaster *_axis_tdata is packed and padded to multiples of 8 bits as necessary. Zero padding the most significant bits is only necessary for 10 and 12 bit wide data.

READY/VALID Handshake

A valid transfer occurs whenever READY, VALID, and aresetn are high at the rising edge of aclk, as seen in Figure 4. During valid transfers, DATA only carries active video data. Blank periods and ancillary data packets are not transferred through the AXI4-Stream video protocol.

Guidelines on Driving s_axis_tvalid

Once s_axis_tvalid is asserted, no interface signals (except the Video Broadcaster core driving s_axis_tready) may change value until the transaction completes (s_axis_tready and s_axis_tvalid are high on the rising edge of aclk). Once asserted, s_axis_tvalid may only be de-asserted after a transaction has completed. Transactions may not be retracted or aborted. In any cycle following a transaction, s_axis_tvalid can either be de-asserted or remain asserted to initiate a new transfer.

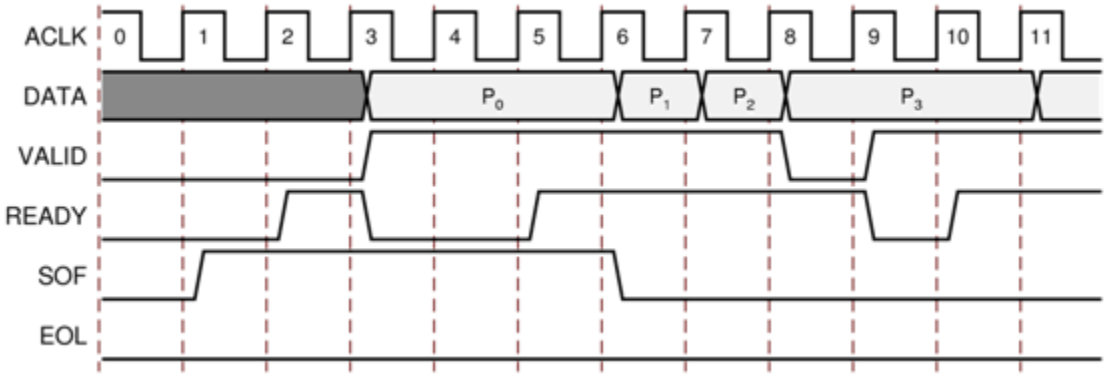

Figure 4: **Example of READY/VALID Handshake, Start of a New Frame**

Guidelines on Driving m[nn]_axis_tready

The m[nn]_axis_tready signal may be asserted before, during or after the cycle in which the Video Broadcaster core asserted m[nn]_axis_tvalid. The assertion of m[nn]_axis_tready may be dependent on the value of m[nn]_axis_tvalid. A slave that can immediately accept data qualified by m[nn]_axis_tvalid, should pre-assert its m[nn]_axis_tready signal until data is received. Alternatively, m[nn]_axis_tready can be registered and driven the cycle following VALID assertion. It is recommended that the AXI4-Stream slave should drive READY independently, or pre-assert READY to minimize latency.

Start of Frame Signals - m[nn]_axis_tuser, s_axis_tuser

The Start-Of-Frame (SOF) signal, physically transmitted over the AXI4-Stream TUSER signal, marks the first pixel of a video frame. The SOF pulse is 1 valid transaction wide, and must coincide with the first pixel of the frame, as seen in Figure 4. The SOF signal serves as a frame synchronization signal, which allows downstream cores to re-initialize and detect the first pixel of a frame. The SOF signal may be asserted an arbitrary number of aclk cycles before the first pixel value is presented on DATA, as long as a VALID/READY is not asserted.

End of Line Signals - m[nn]_axis_tlast, s_axis_tlast

The End-Of-Line (EOL) signal, physically transmitted over the AXI4-Stream TLAST signal, marks the last pixel of a line. The EOL pulse is 1 valid transaction wide, and must coincide with the last pixel of a scan-line.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE Design Suite Embedded Edition tools under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

References

1. UG761 AXI Reference Guide

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/16/2012	1.0	Initial Xilinx release.

Notice of Disclaimer