

Introduction

The Chipscope PLB IBA core is a specialized Bus Analyzer core designed to debug embedded systems that contain the IBM CoreConnect Processor Local Bus (PLB). The Chipscope PLB IBA core in EDK is based on Tcl script that generates a HDL wrapper to the PLB IBA and calls the Chipscope Core Generator to generate the netlist based on user parameters.

Features

- Multiple Match Units for Trigger and Data capture
- Each Match Unit can be enabled and configured independently
- The Match Units for the PLB IBA are
 - PLB Control signals
 - PLB Address Units
 - PLB Read Data Unit
 - PLB Write Data Units
 - PLB Master Units (based on no of masters)
 - PLB Slave Units (based on no of slaves)
- Generic Trigger/Data Unit with selectable width
- For more information refer to the Chipscope Pro Software and Cores User Manual in the Chipscope installation

Chipscope PLB IBA Parameters

To create a Chipscope PLB IBA uniquely tailored for your system and to optimize performance, specific features can be parameterized on the PLB IBA. **Table 1** describes the features that can be parameterized. For a detailed description of the PLB IBA core, see the *Chipscope Pro Software and Cores User Manual* in the Chipscope installation

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-II Pro™, Virtex-II™, Virtex™, Virtex™-E, Spartan™-III, Spartan™-IIE, Spartan™-II	
Version of Core	chipscope_plb_iba	v1.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL/EDIF	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 6.2i or later	
Verification	Chipscope Pro 6.2i or later	
Simulation	N/A	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Table 1: Chipscope PLB IBA Parameters

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Number of Data Samples captured for every trigger match	C_NUM_DATA_SAMPLES	Integer (512, 1024, 2048, 4096, 8192, 16384)	512	integer
Enable the Trigger out signal iba_trig_out which will be asserted when IBA gets triggered	C_ENABLE_TRIGGER_OUT	Integer 1 = Enable Trigger out 0 = Disable Trigger out	0	integer
Target Family	C_FAMILY	Xilinx FPGA families	virtex2	strings
Number of Match Units enabled for <XYZ> Unit Ex : PLB Control Signals	C_<XYZ>_UNITS Ex : C_CONTROL_UNITS	Integer (0-16) 0 = Disable Unit 1-16 = Number of Match Units	0	integer
Counter Width for Match Unit <XYZ> Ex : PLB Control signals Match Unit	C_<XYZ>_UNIT_COUNTER_WIDTH Ex : C_CONTROL_UNIT_COUNTER_WIDTH	Integer (0-32) 0 - Disable Match Counter 1-32 - Match Counter Width (Refer Chipscope Manual)	0	integer
Match Type for Match Unit <XYZ> Ex : PLB Control signals Match Unit	C_<XYZ>_UNIT_MATCH_TYPE Ex : C_CONTROL_UNIT_MATCH_TYPE	"basic", "basic with edges", "extended", "extended with edges", "range", "range with edges" (Refer Chipscope Manual)	"basic"	string
PLB Control Unit	C_CONTROL_UNITS	Integer (0-16)	1	integer
PLB Address Unit	C_ADDR_UNITS	Integer (0-16)	1	integer
Generic Trigger Unit	C_GENERIC_TRIGGER_UNITS	Integer (0-16)	0	integer
Generic Trigger Input Width	C_GENERIC_TRIGGER_IN_WIDTH	Integer	0	integer
PLB Write Data Unit	C_WRDATA_UNITS	Integer (0-16)	0	integer
PLB Read Data Unit	C_RDDATA_UNITS	Integer (0-16)	0	integer
PLB Master (0-16) Unit	C_MASTER<n>_UNITS	Integer (0-16)	0	integer
PLB Slave (0-16) Unit	C_SLAVE<n>_UNITS	Integer (0-16)	0	integer

Chipscope PLB IBA I/O Signals

The I/O signals for the Chipscope PLB IBA are listed in [Table 2](#).

Table 2: Chipscope PLB IBA I/O Signals

Signal Name	Match Unit	Interface	I/O	Description
chipscope_icon_control	N/A	N/A	I[35:0]	ICON Control signals
iba_trig_in	GENERIC	N/A	I	Generic Trigger Inputs
iba_trig_out	GENERIC	N/A	O	IBA Trigger Output
PLB_Clk	CONTROL	MON_PLB	I	PLB Clock
PLB_Rst	CONTROL	MON_PLB	I	PLB Reset
PLB_Abort	CONTROL	MON_PLB	I	PLB abort bus request indicator
PLB_BE	CONTROL	MON_PLB	I	PLB Byte Enable
PLB_BusLock	CONTROL	MON_PLB	I	PLB Bus Lock
PLB_MasterID	CONTROL	MON_PLB	I	PLB Current Master Identifier
PLB_MSize	CONTROL	MON_PLB	I	PLB data bus port width indicator
PLB_PAVValid	CONTROL	MON_PLB	I	PLB primary address valid indicator
PLB_SAVValid	CONTROL	MON_PLB	I	PLB secondary address valid indicator
PLB_RdPrim	CONTROL	MON_PLB	I	PLB secondary to primary read request indicator
PLB_WrPrim	CONTROL	MON_PLB	I	PLB secondary to primary write request indicator
PLB_RNW	CONTROL	MON_PLB	I	PLB read not write
PLB_Size	CONTROL	MON_PLB	I	PLB transfer size
PLB_ABus	ADDR	MON_PLB	I	PLB address bus
PLB_WrDBus	WRDATA	MON_PLB	I	PLB write data bus
SI_RdDBus	RDDATA	MON_PLB	I	PLB read data bus
PLB_MAddrAck	MASTER<n>	MON_PLB	I	PLB master n address acknowledge
PLB_MBusy	MASTER<n>	MON_PLB	I	PLB master n slave busy indicator
PLB_MErr	MASTER<n>	MON_PLB	I	PLB master n slave error indicator
PLB_MRdDAck	MASTER<n>	MON_PLB	I	PLB master n read data acknowledge
PLB_MRdWdAddr	MASTER<n>	MON_PLB	I	PLB master n read word address
PLB_MRearbitrate	MASTER<n>	MON_PLB	I	PLB master n bus rearbitrate indicator
PLB_MSSize	MASTER<n>	MON_PLB	I	PLB master n slave data bus port width
PLB_MWrDAck	MASTER<n>	MON_PLB	I	PLB master n write data acknowledge
M_Abort	MASTER<n>	MON_PLB	I	Master n abort bus request indicator
M_BE	MASTER<n>	MON_PLB	I	Master n byte enables
M_BusLock	MASTER<n>	MON_PLB	I	Master n bus lock
M_MSize	MASTER<n>	MON_PLB	I	Master n data bus port width

Table 2: Chipscope PLB IBA I/O Signals (Continued)

Signal Name	Match Unit	Interface	I/O	Description
M_Priority	MASTER<n>	MON_PLB	I	Master n bus request priority
M_Request	MASTER<n>	MON_PLB	I	Master n bus request
M_RNW	MASTER<n>	MON_PLB	I	Master n read not write
M_Size	MASTER<n>	MON_PLB	I	Master n transfer size
SI_AddrAck	SLAVE<n>	MON_PLB		Slave address acknowledge
SI_RdDAck	SLAVE<n>	MON_PLB		Slave read data acknowledge
SI_RdWdAddr	SLAVE<n>	MON_PLB		Slave read word address
SI_Rearbitrate	SLAVE<n>	MON_PLB		Slave rearbitrate bus indicator
SI_SSize	SLAVE<n>	MON_PLB		Slave data bus port size indicator
SI_Wait	SLAVE<n>	MON_PLB		Slave wait indicator
SI_WrComp	SLAVE<n>	MON_PLB		Slave write transfer complete indicator
SI_WrDAck	SLAVE<n>	MON_PLB		Slave write data acknowledge

Target Technology

The intended target technology is all Xilinx FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/16/04	1.0	Initial release.