

Introduction

Chipscope VIO (Virtual IO) core is a customizable core that can both monitor and drive internal FPGA signals in real time. The Chipscope VIO core in EDK is based on Tcl script that generates a HDL wrapper for the VIO and calls the Chipscope Core Generator to generate the netlist based on user parameters.

Features

- Asynchronous inputs unit
- Synchronous inputs unit
- Asynchronous outputs unit
- Synchronous outputs unit
- Each unit can be enabled and the widths configured separately

For more information, see the *Chipscope Pro Software and Cores User Manual* in the Chipscope Installation.

VIO Parameters

To obtain a Chipscope VIO uniquely tailored for your system, certain features can be parameterized on the VIO. This feature lets you configure a design that utilizes only the resources required by your system, resulting in the best possible performance. **Table 1** describes the Chipscope VIO features that can be parameterized.

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-II Pro™, Virtex-II™, Virtex™, Virtex™-E, Spartan™-III, Spartan™-IIE, Spartan™-II	
Version of Core	chipscope_vio	v1.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL/EDIF	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 6.2i or later	
Verification	Chipscope Pro 6.2i or later	
Simulation	N/A	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Table 1: Chipscope VIO Parameters

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Enable the Asynchronous Input Unit	C_ASYNC_INPUT_ENABLE	Integer 1 = Enable Unit 0 = Disable Unit	0	integer
Asynchronous Input Width	C_ASYNC_INPUT_WIDTH	Integer (1-256)	8	integer
Enable the Asynchronous Output Unit	C_ASYNC_OUTPUT_ENABLE	Integer 1 = Enable Unit 0 = Disable Unit	0	integer
Asynchronous Output Width	C_ASYNC_OUTPUT_WIDTH	Integer (1-256)	8	integer
Enable the Synchronous Input Unit	C_SYNC_INPUT_ENABLE	Integer 1 = Enable Unit 0 = Disable Unit	0	integer
Synchronous Input Width	C_SYNC_INPUT_WIDTH	Integer (1-256)	8	integer
Enable the Synchronous Output Unit	C_SYNC_OUTPUT_ENABLE	Integer 1 = Enable Unit 0 = Disable Unit	0	integer
Synchronous Output Width	C_SYNC_OUTPUT_WIDTH	Integer (1-256)	8	integer
Whether Synchronous Clock is Rising or Falling edge	C_RISING_CLOCK_EDGE	Integer 1 = Rising edge 0 = Falling edge	1	integer
Enable the use of SRL16	C_USE_SRL16	Integer 1 = Use SRL16 0 = Do not use SRL16	1	integer
Target Family	C_FAMILY	Xilinx FPGA families	virtex2	strings

Chipscope VIO I/O Signals

The I/O signals for the Chipscope VIO are listed in [Table 2](#).

Table 2: Chipscope VIO I/O Signals

Signal Name	I/O	Description
chipscope_icon_control	I[0:35]	Chipscope ICON signals
async_in	I	Asynchronous Input
async_out	O	Asynchronous Output

Table 2: Chipscope VIO I/O Signals (Continued)

Signal Name	I/O	Description
clk	I	Clock for Synchronous Input/Output
sync_in	I	Synchronous Input
sync_out	O	Synchronous Output

Target Technology

The intended target technology is all Xilinx FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/16/04	1.0	Initial release.