

Introduction

The Clock Generator module provides clocks according to clock requirements.

Features

- Automatic instantiation of Digital Clock Manager (DCM) modules and their connections
- Automatic instantiation of PLL modules and their connections
- Automatic BUFG insertion
- Automatic DCM and PLL reset sequence determination and connection

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Spartan™-3, Spartan-3E, Spartan-3A, Spartan-3A DSP, Virtex™-II, Virtex-II Pro, Virtex-4, Virtex-5	
Version of core	v2.00.a	
Resources Used		
	Min	Max
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
DCMs	0	4
PLLs	0	2
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs & application notes	None	
Additional Items	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 10.1i or later	
Verification	N/A	
Simulation	NCSim 5.7 or higher	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

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Functional Description

The block diagram for the Clock Generator module is shown in [Figure 1](#)

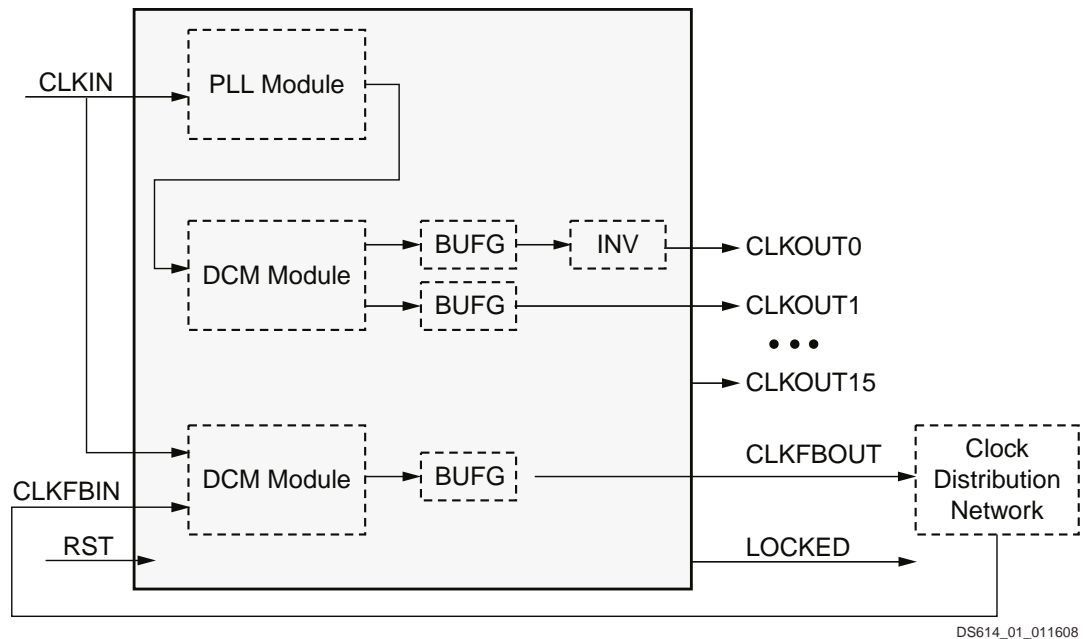


Figure 1: Clock Generator Block Diagram

The Clock Generator module provides clock signals according to system wide clock requirements. The sub-system is composed of DCM modules, PLL modules, BUFGs, clock inverters, and reset logics.

The Clock Generator module supports the following clock requirements:

- One input reference clock
- One feedback clock for clock deskew
- Up to 16 output clocks, whose frequency range refer to DCM and PLL primitives
- Fixed phase shift (0 to 359 degrees) for output clocks
- Grouping output clocks for reducing skew between these clocks. The grouped clocks will be the output of the same DCM, PLL or PLL with deskew adjust. The grouping requirement may be ignored
- Supports device families: Spartan-3, Spartan-3E, Spartan-3A, Spartan-3A DSP, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-5. Input and output clock frequency range check according to device family selection using the slowest speed grade
- Supports both active high and active low external reset

If clock requirements can not be meet, then the LOCKED output signal remains inactive and the output clocks are undetermined.

Clock Generator I/O Signals

The interface signals for the Clock Generator module are listed and described in [Table 1](#).

Table 1: Clock Generator Signal Descriptions

Signal Name	I/O	Initial State	Description
RST	I		If C_EXT_RESET_HIGH = 0, an inverter is inserted; otherwise, this signal is connected to the reset port of the DCM.
CLKIN	I		Connect to DCM or CLKIN of PLL, if used.
CLKFBIN	I		Connect to CLKFB of a DCM, if used
CLKOUT0 - 15	O	Low	Connect to the clock output port of a DCM. A BUFG is inserted; a clock inverter may be inserted.
CLKFBOUT	O	Low	Connect to the CLK0 port of a DCM, if used, a BUFG is inserted.
LOCKED	O	Low	LOCKED = High indicates all required clocks are stable.

Design Parameters

The parameters defined for the Clock Generator module are listed and described in [Table 2](#).

Table 2: Clock Generator Parameters

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_CLKIN_FREQ	Frequency (Hz) of CLKIN	natural	0	integer
C_CLKIN_BUF	Insert BUFG for CLKIN	TRUE, FALSE	FALSE	boolean
C_CLKFBIN_FREQ	Frequency (Hz) of CLKFBIN	natural	0	integer
C_CLKFBIN_BUF	Insert BUFG for CLKFBIN	TRUE, FALSE	FALSE	boolean
C_CLKOUT _{<i>i</i>} _FREQ	<i>i</i> =0,...,15, frequency (Hz) of CLKOUT _{<i>i</i>}	natural	0	integer
C_CLKOUT _{<i>i</i>} _PHASE	<i>i</i> =0,...,15, phase shift of CLKOUT _{<i>i</i>}	0 to 359	0	integer
C_CLKOUT _{<i>i</i>} _GROUP	<i>i</i> =0,...,15, group name of CLKOUT _{<i>i</i>}	NONE, DCM0, DCM1, DCM2, DCM3, PLL0, PLL0_ADJUST, PLL1, PLL1_ADJUST	NONE	string
C_CLKOUT _{<i>i</i>} _BUF	<i>i</i> =0,...,15, if TRUE, insert BUFG for CLKOUT _{<i>i</i>}	TRUE, FALSE	TRUE	boolean
C_CLKFBOUT_FREQ	Frequency (Hz) of CLKFBOUT	natural	0	integer

Table 2: Clock Generator Parameters (Contd)

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_CLKFBOUT_BUF	Insert BUFG for CLKFBOUT i	TRUE, FALSE	TRUE	boolean
C_EXT_RESET_HIGH	External reset active high	0, 1	0	integer
C_FAMILY	Target architecture family for design	Spartan-3, Spartan-3E, Spartan-3A, Spartan-3A DSP, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-5	Virtex5	string

The parameters to describe the internal view of Clock Generator module are listed and described in [Table 3](#).

Table 3: Clock Generator Parameters (low level internal view)

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_CLK_GEN	All required CLKOUTs clocks are generated by DCM or PLL	0, 1	0	integer
C_CLKOUT i _MODULE	$i=0,\dots,15$, module connected to CLKOUT i	NONE, CLKGEN, DCM0-3, PLL0-1	NONE	string
C_CLKOUT i _PORT	$i=0,\dots,15$, port connected to CLKOUT i , (use <i>port_nameB</i> if BUFG is inserted)	NONE, CLKIN, CLKFBIN, CLKOUT0-5(B), CLKFBOUT(B), CLK0(B), CLK90(B), CLK180(B), CLK270(B), CLKDV(B), CLKDV180(B), CLK2X(B), CLK2X180(B), CLKFX(B), CLKFX180(B)	NONE	string
C_CLKFBOUT_MODULE	Module connected to CLKFBOUT	Same as C_CLKOUT i _MODULE	NONE	string
C_CLKFBOUT_PORT	Port connected to CLKFBOUT	Same as C_CLKOUT i _PORT	NONE	string
C_NUM_DCM	Number of DCMs instanced in Clock Generator module	0, 1, 2, 3, 4	0	integer
C_DCM i _DFS_FREQUENCY_MODE	$i=0,\dots,3$, C_DFS_FREQUENCY of DCM i	Same as DCM primitive	LOW	string
C_DCM i _DLL_FREQUENCY_MODE	$i=0,\dots,3$, C_DLL_FREQUENCY of DCM i	Same as DCM primitive	LOW	string

Table 3: Clock Generator Parameters (low level internal view) (Contd)

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_DCM _i _CLK_FEEDBACK	$i=0,\dots,3$, C_CLK_FEEDBACK of DCM _{<i>i</i>}	Same as DCM primitive	1X	string
C_DCM _i _CLKOUT_PHASE_SHIFT	$i=0,\dots,3$, C_CLKOUT_PHASE_SHIFT of DCM _{<i>i</i>}	Same as DCM primitive	NONE	string
C_DCM _i _PHASE_SHIFT	$i=0,\dots,3$, C_PHASE_SHIFT of DCM _{<i>i</i>}	Same as DCM primitive	0	integer
C_DCM _i _CLKFX_MULTIPLY	$i=0,\dots,3$, C_CLKFX_MULTIPLY of DCM _{<i>i</i>}	Same as DCM primitive	4	integer
C_DCM _i _CLKFX_DIVIDE	$i=0,\dots,3$, C_CLKFX_DIVIDE of DCM _{<i>i</i>}	Same as DCM primitive	1	integer
C_DCM _i _CLKDV_DIVIDE	$i=0,\dots,3$, C_CLKDV_DIVIDE of DCM _{<i>i</i>}	Same as DCM primitive	2.0	real
C_DCM _i _CLK0_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLK0	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLK90_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLK90	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLK180_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLK180	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLK270_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLK270	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLKDV_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLKDV	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLKDV180_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLKDV180	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLK2X_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLK2X	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLK2X180_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLK2X180	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLKFX_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLKFX	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLKFX180_BUF	$i=0,\dots,3$, if TRUE, a BUFG is inserted for DCM _{<i>i</i>} CLKFX180	TRUE, FALSE	FALSE	boolean
C_DCM _i _CLKIN_MODULE	$i=0,\dots,3$, module connect to CLKIN of DCM _{<i>i</i>}	Same as C_CLKOUT _{<i>i</i>} _MODULE	NONE	string
C_DCM _i _CLKIN_PORT	$i=0,\dots,3$, port connect to CLKIN of DCM _{<i>i</i>}	Same as C_CLKOUT _{<i>i</i>} _PORT	NONE	string

Table 3: Clock Generator Parameters (low level internal view) (Contd)

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_DCM _i _CLKFB_MODULE	$i=0,\dots,3$, module connect to CLKFB of DCM _{<i>i</i>}	Same as C_CLKOUT _{<i>i</i>} _MODULE	NONE	string
C_DCM _i _CLKFB_PORT	$i=0,\dots,3$, port connect to CLKFB of DCM _{<i>i</i>}	Same as C_CLKOUT _{<i>i</i>} _PORT	NONE	string
C_DCM _i _RST_MODULE	$i=0,\dots,3$, module connect to RST of DCM _{<i>i</i>}	Same as C_CLKOUT _{<i>i</i>} _MODULE	NONE	string
C_NUM_PLL	Number of PLLs instanced in Clock Generator module	0, 1, 2	0	integer
C_PLL _{<i>i</i>} _DIVCLK_DIVIDE	$i=0,1$, C_DIVCLK_DIVIDE of PLL _{<i>i</i>}	Same as PLL primitive	1	integer
C_PLL _{<i>i</i>} _CLKFBOUT_MULT	$i=0,\dots,3$, C_CLKFBOUT_MULT of PLL _{<i>i</i>}	Same as PLL primitive	1	integer
C_PLL _{<i>i</i>} _CLKFBOUT_PHASE	$i=0,1$, C_CLKFBOUT_PHASE of PLL _{<i>i</i>}	Same as PLL primitive	0	integer
C_PLL _{<i>i</i>} _CLKIN1_PERIOD	$i=0,1$, C_CLKIN1_PERIOD of PLL _{<i>i</i>}	Same as PLL primitive	0.0	real
C_PLL _{<i>i</i>} _CLKOUT0_DIVIDE	$i=0,1$, C_CLKOUT0_DIVIDE of PLL _{<i>i</i>}	Same as PLL primitive	1	integer
C_PLL _{<i>i</i>} _CLKOUT0_PHASE	$i=0,1$, C_CLKOUT0_PHASE of PLL _{<i>i</i>}	Same as PLL primitive	0	integer
C_PLL _{<i>i</i>} _CLKOUT0_DESKEW_ADJUST	$i=0,1$, C_CLKOUT0_DESKEW_ADJUST of PLL _{<i>i</i>}	Same as PLL primitive	NONE	string
C_PLL _{<i>i</i>} _CLKOUT1_DIVIDE	$i=0,1$, C_CLKOUT1_DIVIDE of PLL _{<i>i</i>}	Same as PLL primitive	1	integer
C_PLL _{<i>i</i>} _CLKOUT1_PHASE	$i=0,1$, C_CLKOUT1_PHASE of PLL _{<i>i</i>}	Same as PLL primitive	0	integer
C_PLL _{<i>i</i>} _CLKOUT1_DESKEW_ADJUST	$i=0,1$, C_CLKOUT1_DESKEW_ADJUST of PLL _{<i>i</i>}	Same as PLL primitive	NONE	string
C_PLL _{<i>i</i>} _CLKOUT2_DIVIDE	$i=0,1$, C_CLKOUT2_DIVIDE of PLL _{<i>i</i>}	Same as PLL primitive	1	integer
C_PLL _{<i>i</i>} _CLKOUT2_PHASE	$i=0,1$, C_CLKOUT2_PHASE of PLL _{<i>i</i>}	Same as PLL primitive	0	integer
C_PLL _{<i>i</i>} _CLKOUT2_DESKEW_ADJUST	$i=0,1$, C_CLKOUT2_DESKEW_ADJUST of PLL _{<i>i</i>}	Same as PLL primitive	NONE	string
C_PLL _{<i>i</i>} _CLKOUT3_DIVIDE	$i=0,1$, C_CLKOUT3_DIVIDE of PLL _{<i>i</i>}	Same as PLL primitive	1	integer
C_PLL _{<i>i</i>} _CLKOUT3_PHASE	$i=0,1$, C_CLKOUT3_PHASE of PLL _{<i>i</i>}	Same as PLL primitive	0	integer

Table 3: Clock Generator Parameters (low level internal view) (Contd)

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_PLL <i>i</i> _CLKOUT3_DESKEW_ADJUST	$i=0,1$, C_CLKOUT3_DESKEW_ADJUST of PLL <i>i</i>	Same as PLL primitive	NONE	string
C_PLL <i>i</i> _CLKOUT4_DIVIDE	$i=0,1$, C_CLKOUT4_DIVIDE of PLL <i>i</i>	Same as PLL primitive	1	integer
C_PLL <i>i</i> _CLKOUT4_PHASE	$i=0,1$, C_CLKOUT4_PHASE of PLL <i>i</i>	Same as PLL primitive	0	integer
C_PLL <i>i</i> _CLKOUT4_DESKEW_ADJUST	$i=0,1$, C_CLKOUT4_DESKEW_ADJUST of PLL <i>i</i>	Same as PLL primitive	NONE	string
C_PLL <i>i</i> _CLKOUT5_DIVIDE	$i=0,1$, C_CLKOUT5_DIVIDE of PLL <i>i</i>	Same as PLL primitive	1	integer
C_PLL <i>i</i> _CLKOUT5_PHASE	$i=0,1$, C_CLKOUT5_PHASE of PLL <i>i</i>	Same as PLL primitive	0	integer
C_PLL <i>i</i> _CLKOUT5_DESKEW_ADJUST	$i=0,1$, C_CLKOUT5_DESKEW_ADJUST of PLL <i>i</i>	Same as PLL primitive	NONE	string
C_PLL <i>i</i> _CLKFBOUT_DESKEW_ADJUST	$i=0,1$, C_CLKFBOUT_DESKEW_ADJUST of PLL <i>i</i>	Same as PLL primitive	NONE	string
C_PLL <i>i</i> _CLKOUT0_BUF	$i=0,1$, if TRUE, a BUFG is inserted for PLL <i>i</i> CLKOUT0	TRUE, FALSE	FALSE	boolean
C_PLL <i>i</i> _CLKOUT1_BUF	$i=0,1$, if TRUE, a BUFG is inserted for PLL <i>i</i> CLKOUT1	TRUE, FALSE	FALSE	boolean
C_PLL <i>i</i> _CLKOUT2_BUF	$i=0,1$, if TRUE, a BUFG is inserted for PLL <i>i</i> CLKOUT2	TRUE, FALSE	FALSE	boolean
C_PLL <i>i</i> _CLKOUT3_BUF	$i=0,1$, if TRUE, a BUFG is inserted for PLL <i>i</i> CLKOUT3	TRUE, FALSE	FALSE	boolean
C_PLL <i>i</i> _CLKOUT4_BUF	$i=0,1$, if TRUE, a BUFG is inserted for PLL <i>i</i> CLKOUT4	TRUE, FALSE	FALSE	boolean
C_PLL <i>i</i> _CLKOUT5_BUF	$i=0,1$, if TRUE, a BUFG is inserted for PLL <i>i</i> CLKOUT5	TRUE, FALSE	FALSE	boolean
C_PLL <i>i</i> _CLKIN1_MODULE	$i=0,1$, module connect to CLKIN1 of PLL <i>i</i>	Same as C_CLKOUT <i>i</i> _MODULE	NONE	string
C_PLL <i>i</i> _CLKIN1_PORT	$i=0,1$, port connect to CLKIN1 of PLL <i>i</i>	Same as C_CLKOUT <i>i</i> _PORT	NONE	string

Table 3: Clock Generator Parameters (low level internal view) (Contd)

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_PLL <i>i</i> _CLKFBIN_MODULE	$i=0,1$, module connect to CLKFBIN of PLL <i>i</i>	Same as C_CLKOUT <i>i</i> _MODULE	NONE	string
C_PLL <i>i</i> _CLKFBIN_PORT	$i=0,1$, port connect to CLKFBIN of PLL <i>i</i>	Same as C_CLKOUT <i>i</i> _PORT	NONE	string
C_PLL <i>i</i> _RST_MODULE	$i=0,1$, module connect to RST of PLL <i>i</i>	Same as C_CLKOUT <i>i</i> _MODULE	NONE	string

The value of parameters in Table 3 are generated automatically from value of parameters in Table 2.

Parameter - Port Dependencies

The table below contains the affects of setting various parameters

Table 4: Clock Generator Parameter-Port Dependencies

Parameter	Port	Description
C_CLKIN_FREQ	CLKIN	0 - CLKIN is not used
C_CLKFBIN_FREQ	CLKFBIN, CLKFBOUT	0 - CLKFBIN is not used, has to be equal to C_CLKFBOUT_FREQ
C_CLKOUT <i>i</i> _FREQ	CLKOUT <i>i</i> ($i=0,\dots,15$)	0 - CLKOUT <i>i</i> is not used
C_CLKOUT <i>i</i> _PHASE	CLKOUT <i>i</i> ($i=0,\dots,15$)	
C_CLKOUT <i>i</i> _GROUP	CLKOUT <i>i</i> ($i=0,\dots,15$)	NONE - CLKOUT <i>i</i> has no group requirement
C_CLKOUT <i>i</i> _BUF	CLKOUT <i>i</i> ($i=0,\dots,15$)	Set to FALSE if C_CLKOUT <i>i</i> _FREQ is 0
C_CLKFBOUT_FREQ	CLKFBIN, CLKFBOUT	0 - CLKFBOUT is not used, has to be equal to C_CLKFBIN_FREQ

Clock Generator Register Descriptions

Not Applicable.

Clock Generator Interrupt Descriptions

Not Applicable.

Design Implementation

Target Technology

The intended target technology is an FPGA in one of the following families: Spartan-3, Spartan-3E, Spartan-3A, Spartan-3A DSP, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-5.

Device Utilization and Performance Benchmarks

The device utilization depends on the number of output clocks used and the value of the parameters of each output clock. Up to four DCM modules and two PLL modules may be instanced with BUFGs, clock inverters, and reset logics. See respective FPGA family user guide for details on DCM, PLL and BUFG primitive performance and available resources.

For virtex5 family, up to 2 PLLs and 1 DCM (used only for external feedback clock) will be used; and for all other families, up to 4 DCMs (no PLL) will be used in one Clock Generator v2.00.a module.

Specification Exceptions

Not Applicable.

Reference Documents

None.

Revision History

Date	Version	Revision
6/4/07	1.0	Initial Xilinx release.
1/16/08	2.0	PLL support included.