

## Introduction

The FIT core is a peripheral that generates a strobe (interrupt) signal at fixed intervals and is not attached to any bus. The Fixed Interval Timer (FIT) generates an interrupt every C\_NO\_CLOCKS. The interrupt signal is held high for one clock cycle. The core begins operation immediately after FPGA configuration unless the clock is held or a reset is connected to the FIT.

## Features

- Configurable number of clock cycles between interrupts
- Configurable inaccuracy in clock intervals between interrupts
- Optional reset

| LogiCORE™ IP Facts                       |   |      |     |            |
|--|---|------|-----|------------|
| Core Specifics                           |   |      |     |            |
| Supported Device Family                  | See <a href="#">EDK Supported Device Families</a> . |      |     |            |
| Version of Core                          | v1.01a  |      |     |            |
| Resources Used                           | I/O   | LUTs | FFs | Block RAMs |
|  | n   | n    | n   | n          |
| Special Features                         | N/A   |      |     |            |
| Provided with Core                       |   |      |     |            |
| Documentation                            | Product Specification                               |      |     |            |
| Design File Formats                      | VHDL  |      |     |            |
| Constraints File                         | N/A   |      |     |            |
| Verification                             | N/A   |      |     |            |
| Instantiation Template                   | N/A   |      |     |            |
| Additional Items                         | N/A   |      |     |            |
| Design Tool Requirements                 |   |      |     |            |
| Xilinx Implementation Tools              | See <a href="#">Tools</a> for requirements.         |      |     |            |
| Verification                             |   |      |     |            |
| Simulation                               |   |      |     |            |
| Synthesis                                |   |      |     |            |
| Support                                  |   |      |     |            |
| Provided by <a href="#">Xilinx, Inc.</a> |   |      |     |            |

## FIT Parameters

Table 1: FIT Parameters

| Parameter Name   | Feature/Description   | Allowable Values                                | Default Value | Tool Assigned | VHDL Type |
|------------------|---|---|---------------|---------------|-----------|
| C_FAMILY         | Device Family   | See <a href="#">C_FAMILY parameter values</a> . |               | Yes           | string    |
| C_NO_CLOCKS      | The number of clock cycles between strobes  | >1  | 6216          | No            | integer   |
| C_INACCURACY     | The allowed inaccuracy in the number of clock cycles between strobes. Expressed in per thousands. | ≥0  | 0             | No            | integer   |
| C_EXT_RESET_HIGH | Level of reset  | 0 = active low<br>1 = active high               | 1             | No            | integer   |

### Allowable Parameter Combinations

There are no restrictions on allowable parameter combinations. The core tries to implement the counter in the most efficient way using SRL16 primitives. But for certain values of C\_NO\_CLOCKS, the core can not implement the timer using the SRL16. In this case, a normal bit counter will be implemented. To use SRL16, the value of C\_NO\_CLOCKS must be able to be factored into values between 2 and 128. 128 uses 7 SRL16 primitives, which is the same as the 7 LUTs a normal counter would use and thus after that point it is no longer more efficient to use the SRL16. To enable the use of SRL16 as compared to bit counters, an inaccuracy can be set using the parameter C\_INACCURACY. The inaccuracy value specifies the range of valid clock intervals that can be generated. The core then tests each value in this range to check if it can be factorized.

### FIT I/O Signals

The I/O signals for the FIT are listed in [Table 2](#).

Table 2: FIT I/O Signals

| Signal Name | Interface | I/O | Initial State | Description      |
|-------------|-----------|-----|---------------|------------------|
| Clk         | N/A       | I   | N/A           | Clock            |
| Rst         | N/A       | I   | N/A           | Optional reset   |
| Interrupt   | N/A       | O   | 0             | Interrupt signal |

The Rst port can be left unconnected or tied to ground and less resources will be used. The reset logic when using the SRL16 doubles the resource usage, but in most cases this will still be smaller than using a normal bit counter. When using the counter the reset logic adds 1 LUT. When resetting the SRL16 the reset signal must be asserted for 17 cycles. When resetting the bit counter the reset must only be asserted for one cycle.

### Parameter - Port Dependencies

Not Applicable.

### FIT Register Descriptions

Not applicable.

## FIT Interrupt Descriptions

The FIT generates an interrupt every C\_NO\_CLOCKS. The interrupt signal is held high for one clock cycle. The core begins operation immediately after FPGA configuration if the reset is not connected. If the reset is connected and asserted the FIT begins operation after the reset is released. To reset the SRL16 primitives the reset must be asserted for a minimum of 17 cycles. To reset the bit counter implementation the reset need only be asserted for one clock cycle.



Figure 1: FIT block diagram

## Design Implementation

### Design Tools

The FIT design is generated by the EDK tools.

XST is the synthesis tool used for synthesizing the FIT. The NGC netlist output from XST is then input to the Xilinx Foundation® tool suite for actual device implementation.

### Target Technology

The intended target technology is an FPGA listed in [EDK Supported Device Families](#).

### Device Utilization and Performance Benchmarks

The device utilization depends on the configured parameter values. For optimal device utilization the C\_NO\_CLOCKS should factor into numbers less than or equal to 16 and the reset should not be used.

## Specification Exceptions

Not applicable.

## Reference Documents

Not applicable.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Revision History

The following table shows the revision history for this document:

| Date     | Version | Description of Revisions  |
|----------|---------|---|
| 02/11/03 | 1.0     | Initial Release   |
| 01/26/04 | 1.1     | Update to copyright and trademarks  |
| 08/03/04 | 1.2     | Converted document format   |
| 8/17/04  | 1.3     | Updated for Gmm; updated trademarks and supported device family list  |
| 9/28/04  | 1.4     | Updated for fit_timer_v1_01_a   |
| 4/2/05   | 1.5     | Updated for EDK 7.1.1 SP1; updated supported device family listing.   |
| 04/24/09 | 1.6     | Replaced references to supported device families and tool name(s) with hyperlink to PDF file; converted to current DS template. |

## Notice of Disclaimer

Xilinx is providing this product documentation, hereinafter "Information," to you "AS IS" with no warranty of any kind, express or implied. Xilinx makes no representation that the Information, or any particular implementation thereof, is free from any claims of infringement. You are responsible for obtaining any rights you may require for any implementation based on the Information. All specifications are subject to change without notice. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY WHATSOEVER WITH RESPECT TO THE ADEQUACY OF THE INFORMATION OR ANY IMPLEMENTATION BASED THEREON, INCLUDING BUT NOT LIMITED TO ANY WARRANTIES OR REPRESENTATIONS THAT THIS IMPLEMENTATION IS FREE FROM CLAIMS OF INFRINGEMENT AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Except as stated herein, none of the Information may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx.