

Introduction

The FIT core is a peripheral that generates a strobe (interrupt) signal at fixed intervals and is not attached to any bus. The Fixed Interval Timer (FIT) generates an interrupt every C_NO_CLOCKS. The interrupt signal is held high for one clock cycle. The core begins operation immediately after FPGA configuration unless the clock is held or a reset is connected to the FIT.

Features

- Configurable number of clock cycles between interrupts
- Configurable inaccuracy in clock intervals between interrupts
- Optional reset

LogiCORE™ IP Facts				
Core Specifics				
Supported Device Family ⁽¹⁾	Zynq™-7000 ⁽²⁾ , Kintex™-7, Virtex®-7, Artix™-7, Virtex-6, Spartan®-6, Virtex-5, Virtex-4, Spartan-3			
Resources				
Configuration	LUTs	FFs	DSP Slices	Block RAMs
All	n	n	0	0
Provided with Core				
Documentation	Product Specification			
Design Files	ISE: VHDL Vivado: RTL			
Example Design	Not Provided			
Test Bench	Not Provided			
Constraints File	Not Provided			
Supported SW Driver	N/A			
Tested Design Tools⁽³⁾				
Design Entry Tools	Vivado™ Design Suite ⁽⁴⁾ Xilinx Platform Studio (XPS)			
Simulation	Mentor Graphics ModelSim			
Synthesis Tools	Xilinx Synthesis Technology (XST) Vivado Synthesis			
Support				
Provided by Xilinx @ www.xilinx.com/support				

1. For a complete list of supported derivative devices, see the [Embedded Edition Derivative Device Support](#).
2. Supported in ISE Design Suite implementations only.
3. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).
4. Supports 7 series devices only.

FIT Parameters

Table 1: FIT Parameters

Parameter Name	Feature /Description	Allowable Values	Default Value	Tool Assigned	VHDL Type
C_FAMILY	Device Family	aartix7, artix7, artix7l, aspartan3, aspartan3a, aspartan3adsp, aspartan3e, aspartan6, azynq, kintex7, kintex7l, qartix7, qartix7l, qkintex7, qkintex7l, qvirtex4, qvirtex5, qspartan6, qspartan6l, qvirtex4, qvirtex5, qvirtex6, qvirtex7, qvirtex7l, qzynq, spartan3, spartan3a, spartan3adsp, spartan3e, spartan6, spartan6l, virtex4, virtex5, virtex6, virtex6l, virtex7, virtex7l, zynq	virtex6	Yes	string
C_NO_CLOCKS	The number of clock cycles between stobes	3 - 2147483647	6216	No	integer
C_INACCURACY	The allowed inaccuracy in the number of clock cycles between stobes. Expressed in per thousands.	0 - 999	0	No	integer
C_EXT_RESET_HIGH	Level of reset	0 = active-Low 1 = active-High	1	No	integer

Allowable Parameter Combinations

There are no restrictions on allowable parameter combinations. The core tries to implement the counter in the most efficient way using SRL16 primitives. But for certain values of C_NO_CLOCKS, the core can not implement the timer using the SRL16. In this case, a normal bit counter is implemented. To use SRL16, the value of C_NO_CLOCKS must be able to be factored into values between 2 and 128. 128 uses 7 SRL16 primitives, which is the same as the 7 LUTs a normal counter would use and thus after that point it is no longer more efficient to use the SRL16. To enable the use of SRL16 as compared to bit counters, an inaccuracy can be set using the parameter C_INACCURACY. The inaccuracy value specifies the range of valid clock intervals that can be generated. The core then tests each value in this range to check if it can be factorized.

FIT I/O Signals

The I/O signals for the FIT are listed in [Table 2](#).

Table 2: FIT I/O Signals

Signal Name	Interface	I/O	Initial State	Description
Clk	N/A	I	N/A	Clock
Rst	N/A	I	N/A	Optional reset
Interrupt	N/A	O	0	Interrupt signal

The Rst port can be left unconnected or tied to ground and less resources will be used. The reset logic, when using the SRL16, doubles the resource usage, but in most cases this is still smaller than using a normal bit counter. When using the counter the reset logic adds 1 LUT. When resetting the SRL16 the reset signal must be asserted for 17 cycles. When resetting the bit counter the reset must only be asserted for one cycle.

Parameter - Port Dependencies

Not Applicable.

FIT Register Descriptions

Not applicable.

FIT Interrupt Descriptions

The FIT generates an interrupt every C_NO_CLOCKS. The interrupt signal is held high for one clock cycle. The core begins operation immediately after FPGA configuration if the reset is not connected. If the reset is connected and asserted the FIT begins operation after the reset is released. To reset the SRL16 primitives the reset must be asserted for a minimum of 17 cycles. To reset the bit counter implementation the reset need only be asserted for one clock cycle.

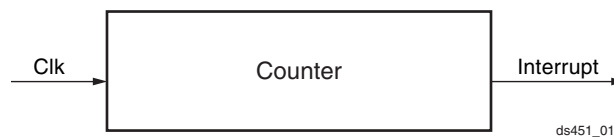


Figure 1: FIT Block Diagram

Design Implementation

Design Tools

The FIT design is generated by the EDK or Vivado tools.

XST or Vivado is the synthesis tool used for synthesizing the FIT. The netlist output from the synthesis tool is then input to the Xilinx Foundation® or the Vivado Design Suite for actual device implementation.

Target Technology

The target technology is an FPGA listed in the [Supported Device Family](#) field of the LogiCORE Facts table.

Device Utilization and Performance Benchmarks

The device utilization depends on the configured parameter values. For optimal device utilization the C_NO_CLOCKS should factor into numbers less than or equal to 16 and the reset should not be used.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite and ISE Design Suite Embedded Edition tools under the terms of the [Xilinx End User License](#). Information about this and other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Reference Documents

Not applicable.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/11/03	1.0	Initial Release
01/26/04	1.1	Update to copyright and trademarks
08/03/04	1.2	Converted document format
8/17/04	1.3	Updated for Gmm; updated trademarks and supported device family list
9/28/04	1.4	Updated for fit_timer_v1_01_a
4/2/05	1.5	Updated for EDK 7.1.1 SP1; updated supported device family listing.
04/24/09	1.6	Replaced references to supported device families and tool name(s) with hyperlink to PDF file; converted to current DS template.
04/19/10	1.7	Updated for fit_timer_v1_01_b
07/25/12	1.8	Updated for fit_timer_v1_01_c, with correction of simulation issue for C_NO_CLOCKS > 2 ³⁰ .

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