

Introduction

The customizable LogiCORE™ IP ChipScope™ Pro Integrated Bit Error Ratio Test (IBERT) core for 7 series FPGA GTZ transceivers is designed for evaluating and monitoring the GTZ transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTZ transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. This core can be used as a self-contained or open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core
- Provides a user-selectable number of 7 series FPGA GTZ transceivers
- Transceivers can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width
- Requires a system clock that can be sourced from a pin or one of the enabled GTZ transceivers

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	Virtex®-7
Supported User Interfaces	N/A
Resources	See Table 2 .
Provided with Core	
Documentation	Product Specification User Guide
Design Files	Vivado™: RTL
Example Design	Verilog/VHDL
Test Bench	Not Provided
Constraints File	Vivado: XDC
Simulation Model	Not Provided
Supported S/W Driver	Not Provided
Tested Design Flows⁽²⁾	
Design Entry	Vivado Design Suite 2012.4 ⁽³⁾
Simulation	Not Provided
Synthesis	Xilinx Synthesis Technology (XST)
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see the [Embedded Edition Derivative Device Support](#).
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).
3. Supports only 7 series devices.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of 7 series FPGA GTZ transceivers.

Functional Description

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration family for 7 series FPGA GTZ transceivers. Parameterizable to use different GTZ transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTZ transceiver desired, giving many different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels. In addition, the configuration and tuning of the GTZ transceivers is accessible through logic that communicates to the DRP port of the GTZ transceiver, in order to change attribute settings, as well as registers that control the values on the ports. At run-time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

GTZ Transceiver Features

The IBERT core is designed for Physical Medium Attachment (PMA) evaluation and demonstration. All the major PMA features of the GTZ transceiver are supported and controllable, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- Phase-Locked Loop (PLL) Divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including:

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each serial transceiver, two LC tank PLLs are present, one for RX, and one for TX. There are no shared PLLs amongst channels in the OCTAL.

[Figure 1](#) shows a GTZ OCTAL in a 7 series device. The GTZ channels has the serial transceiver and CPLL units.

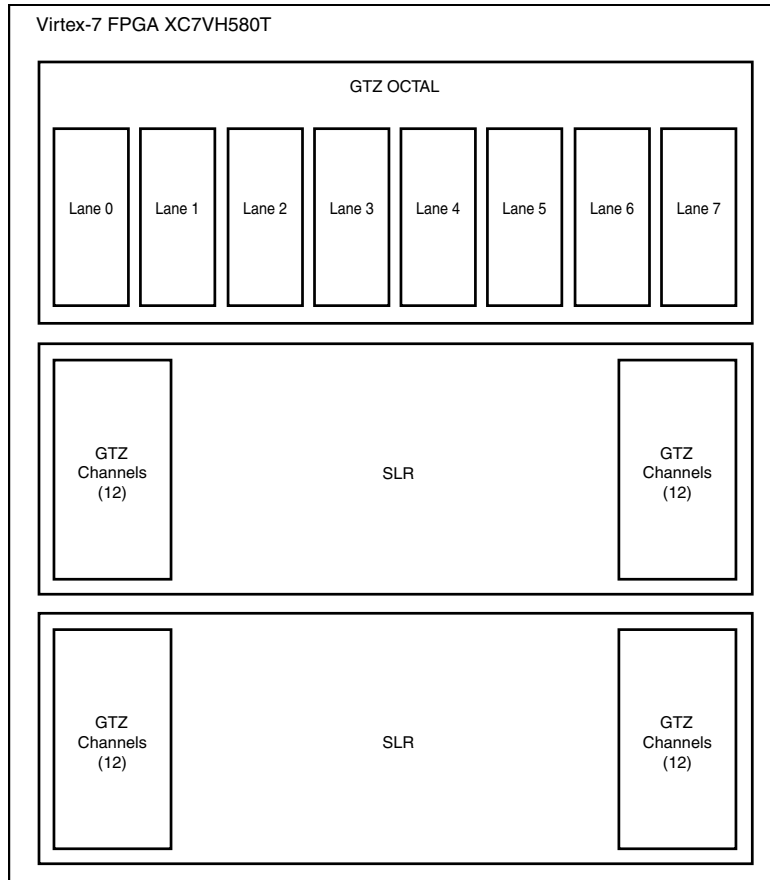


Figure 1: GTZ OCTAL in a Virtex-7 FPGA XC7VH580T

The serial transceiver REFCLK can be sourced from CPLL based on multiplexers as shown in Figure 2. This can be selected from the 7 series FPGA IBERT IP Catalog GUI.

Each OCTAL has two REFCLK inputs and attributes control which REFCLK is used for each channel. The IBERT 7 series GTZ core only supports one line rate per OCTAL.

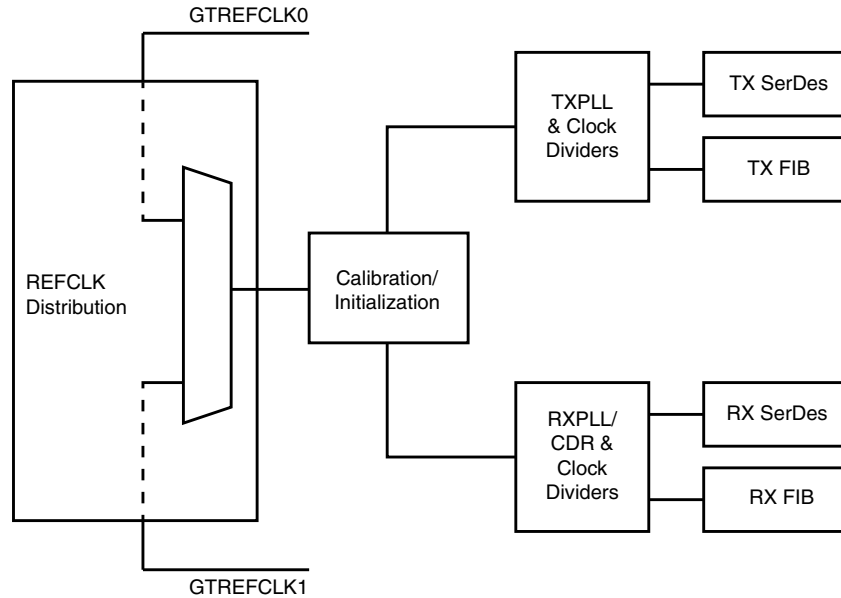


Figure 2: GTZ Internal Clocking Architecture

Pattern Generation and Checking

Each GTZ transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...), and Clk 10x(11111111110000000000...) patterns.

These patterns are optimized for the logic width that was selected at run time. The TX pattern and RX pattern are individually selected.

The Analyzer software displays a “link” signal until there are five consecutive cycles with errors. Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with errors, the ChipScope Pro Analyzer software disables the link signal. Internal counters accumulate the number of words and errors received.

DRP and Port Access

You can change GTZ transceiver ports and attribute values. The DRP interface logic allows the run-time software to monitor and change any attribute in the GTZ OCTAL. When applicable, readable and writable registers are also included that are connected to the many ports of the GTZ OCTAL. All are accessible at run-time using the ChipScope Analyzer tool.

Vivado IP Catalog

The Vivado IP Catalog allows you to define and generate a customized IBERT core to use to validate the transceivers of the device. You can customize the number of serial transceivers within the OCTAL that are power up, and the line rate and reference clock for the OCTAL.

Entering the Component Name

The Component Name field, stored as `component_name` in the generated XCO parameter file, can consist of any combination of alpha-numeric characters including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Generating an Example Design

The IBERT Vivado IP Catalog normally generates example design along with standard Xilinx Vivado IP Catalog output files, such as a netlist and instantiation template files. Example design and Implement scripts are generated under the folder with the component name.

Receiver Output Clock

The receiver clock probe enable is provided to pull out a recovered clock from any serial transceiver, if desired. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

GTZ Transceiver Naming Style

There are two conventions for naming the GTZ transceiver, based on the location in the serial transceiver tile in the device. M and n in X_mY_n naming convention indicate the X and Y coordinates of the serial transceiver location. M and n in serial transceiver m_n naming convention indicating serial transceiver number and quad associated.

System Clock

The IBERT core requires a free-running system clock for communication and other logic that is included in the core. This clock can be chosen at generation time to originate from an FPGA pin, or to be driven from the TXOUTCLK port of one of the GTZ transceivers. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT core design. If the system clock is running faster than 100 MHz, it is divided down internally using an Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints. Note that the clock source selected must be stable and free running after the FPGA is configured with the IBERT design. The system clock is used for core communication and as a reference for system measurements. Therefore, the clock source selected must remain operational and stable when using the IBERT core.

Line Rate Support

IBERT supports one line rate per OCTAL. A list of the supported line rates is available, and for each line rate, one or more reference clock rates are supported. The proper divider settings is specified for each line rate/refclk rate combination.

Serial Transceiver Location

Based on the total number of serial transceivers selected, provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device. Depending on the device selected, one or two OCTALs are available. The region shown in the panel indicates the location of the OCTAL in the device.

Reference Clock

The reference clock source should be provided for all the serial transceivers selected. The drop-down list provides you with possible sources based on local clocks in the same quad and shared clocks from north/south OCTALs.

Generating the Core

After entering the IBERT core parameters, click Generate to create the IBERT core files. After the IBERT core has been generated, a list of files that are generated appears in a separate window called "Readme <corename>."

IBERT Interface Ports

The I/O signals of the IBERT core consist only of the GTZ transceiver reference clocks, the GTZ transceiver transmit and receive pins, and a system clock (optional). [Table 1](#) lists the IBERT interface ports and their descriptions.

Table 1: Interface Ports

Port Name	Direction	Description
SYSCLK_I	In	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
TXN_0[7:0] TXP_0[7:0]	Out	Transmit differential pairs for each of the n GTZ transceivers used.
RXN_0[7:0] RXP_0[7:0]	In	Receive differential pairs for each of the n GTZ transceivers used.
GTREFCLK0N_I[1:0] GTREFCLK0P_I[1:0]	In	GTZ transceiver reference clocks 0 used. The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTZ transceivers can share clock inputs.
GTREFCLK1N_I[1:0] GTREFCLK1P_I[1:0]	In	GTZ transceiver reference clocks 1 used. The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTZ transceivers can share clock inputs.

Performance and Resource Utilization

[Table 2](#) shows the performance and resource utilization numbers generated for the various IBERT setup listed and targeted to XC7VH580T-HCG1155-2.

Table 2: Performance and Resource Utilization for XC7VH580T-HCG1155-2 Device

IBERT Setup			Resources			Performance
Line Rate (Gb/s)	Refclk Frequency (MHz)	No. of Octal	LUTs	Flip-Flops	Block RAMs	F _{Max} (MHz)
27.953	291.172	1	15,543	18,474	0	149.815
10.313	322.266	1	15,543	18,474	0	149.815

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

More information about the ChipScope Pro software and cores is available in the *Chipscope Pro Software and Cores User Guide*, located at www.xilinx.com.

For more information about the 7 series FPGA GTZ transceiver, see the *7 Series FPGAs GTZ Transceivers User Guide*, located at www.xilinx.com.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the IDS Embedded Edition Derivative Device Support web page (www.xilinx.com/ise/embedded/ddsupport.htm) for a complete list of supported derivative devices for this core.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite and ISE Design Suite Embedded Edition tools under the terms of the [Xilinx End User License](#).

Information about this and other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

List of Acronyms

Acronym	Spelled Out
CPRI	Common Packet Radio Interface
DFE	Decision Feedback Equalizer
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
IBERT	Integrated Bit Error Ratio Tester
I/O	Input/Output
ILA	Integrated Logic Analyzer
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
MHz	Mega Hertz
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop

Acronym	Spelled Out
PMA	Physical Medium Attachment
PRBS	Pseudo-random binary sequence
RAM	Random Access Memory
RX	Receive
TX	Transmit
XAUI	eXtended Attachment Unit Interface

Revision History

The following table shows a summary of changes to this document:

Date	Version	Revision
10/16/12	1.0	Initial Xilinx release
12/18/12	2.0	<ul style="list-style-type: none"> Support for Vivado 2012.4 added. Updated GTZ blocks in Figure 1. Updated descriptions in Table 2.

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