JESD204 PHY v1.0

LogiCORE IP Product Guide

Vivado Design Suite

PG198 October 1, 2014

XILINX
ALL PROGRAMMABLE™

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Appendix C: Additional Resources and Legal Notices

Introduction

The Xilinx® LogiCORE™ IP JESD204 PHY core implements a JESD204B physical interface to simplify sharing a single MGT channel between transmit and receive cores. This core is not intended to be used stand-alone and should only be used only in conjunction with the JESD204 core.

Note: This core is pre-production unless used by the JESD204 IP and is provided as stand-alone IP for use in the JESD204 IP example design only.

Features

- Designed to JEDEC® JESD204B [Ref 1]
- Supports 1 to 12 lane configurations
- Supports Subclass 0, 1 and 2
- Physical Layer functions provided
- Supports transceiver sharing between TX and RX cores

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™ Architecture, Zynq®-7000 All Programmable SoC, 7 Series
Supported User Interfaces	N/A
Resources	See Table 2-1, Table 2-2 and Table 2-3.
Provided with Core	
Design Files	RTL
Example Design	Verilog
Test Bench	Verilog
Constraints File	XDC
Simulation Model	Verilog
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The LogiCORE™ IP JESD204 PHY core implements a JESD204B Physical interface supporting line rates between 1 and 12.5 Gb/s on 1 to 12 lanes using GTX, GTH or GTP transceivers. (See the device data sheets listed in References for maximum line rates supported by each device and family.) The JESD204 PHY core can be configured with independent transmit and receive line rates.

Figure 1-1 shows a block diagram of the JESD204 PHY core with shared logic in the example design.

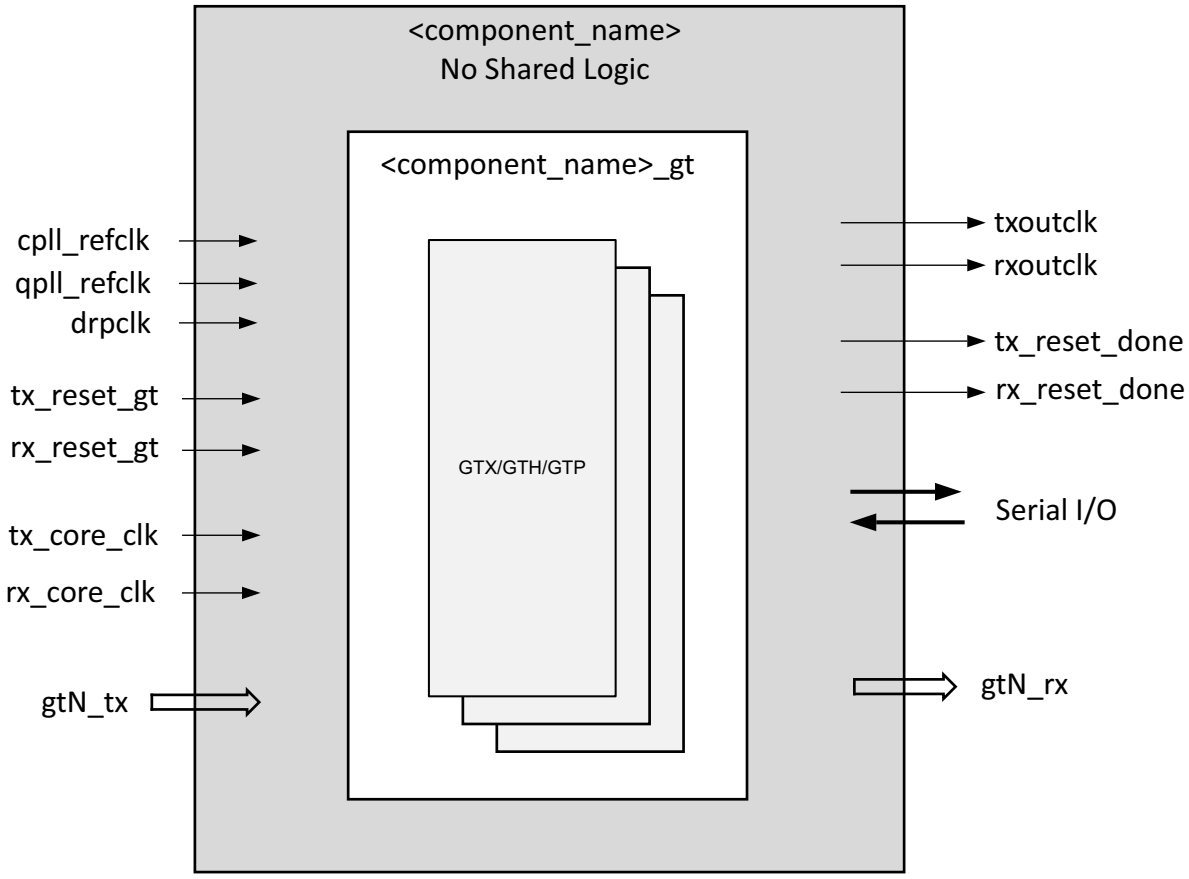

Figure 1-1: **JESD204 PHY Block Diagram: Shared Logic in Example Design**

Figure 1-2 shows a block diagram of the JESD204 PHY core with shared logic in the core.

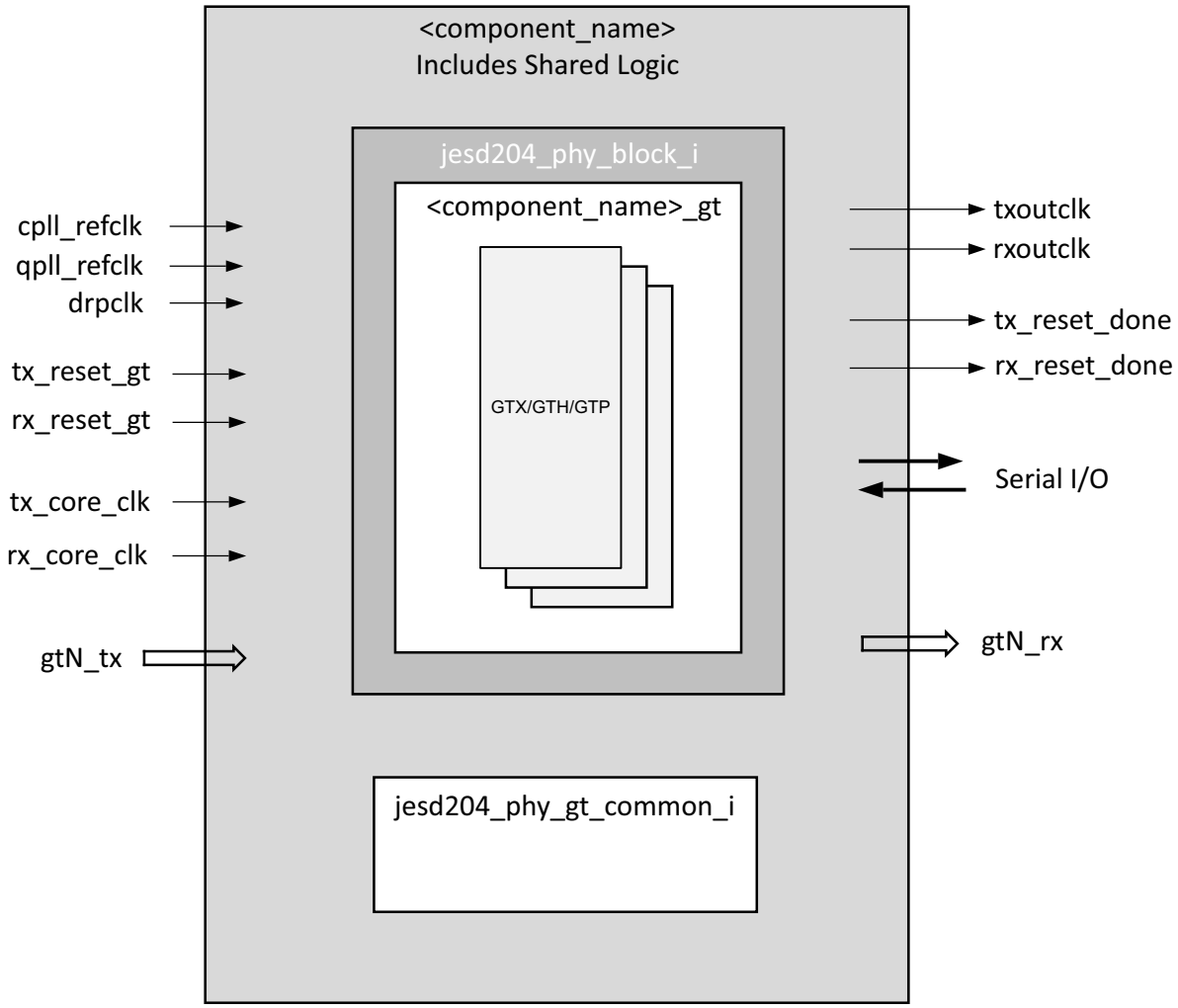

Figure 1-2: **JESD204 PHY Block Diagram: Shared Logic in Core**

When used in conjunction with the JESD204, the JESD204 PHY core is a fully-verified solution design delivered by using the Xilinx® Vivado® Design Suite. In addition, an example design is provided in Verilog. See The *JESD204 Product Guide* (PG066) for more details [Ref 2].

Applications

The JESD204 PHY core is a sub-core of the JESD204 core. See the *JESD204 Product Guide* (PG066) for application details [Ref 2]. Figure 1-3 shows a JESD204 PHY used in the JESD204 design.

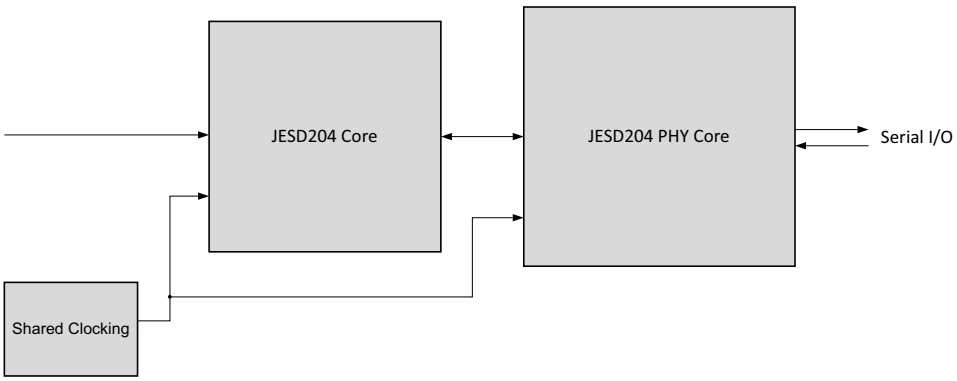

Figure 1-3: **JESD204 PHY used in JESD204 Solution**

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

This chapter details the resource utilization and ports for the JESD204 PHY core.

Performance

The core meets the performance spec of JESD204B. The maximum serial line rate is limited by the max GTX/GTP/GTH line rate for the chosen device. See the appropriate device data sheet listed in References in Appendix C.

Resource Utilization

Table 2-1, Table 2-2 and Table 2-3 provide approximate resource counts for the various core options.

Table 2-1: **Resource Utilization for GTXE2/GTHE2 Devices (XC7K325T FFG900 -2)**

Number of Transceivers	FF	LUTs	BUFG
1	351	223	5
2	402	262	5
3	455	302	5
4	506	338	5
5	559	377	5
6	610	413	5
7	663	455	5
8	714	494	5
9	767	531	5
10	818	567	5
11	871	608	5
12	922	648	5

Table 2-2: **Resource Utilization for GTPE2 Devices (XC7A200T FBG676 -2)**

Number of Transceivers	FF	LUTs	BUFG
1	406	276	6
2	531	377	6
3	656	476	6
4	781	577	6
5	906	676	6
6	1031	775	6
7	1156	876	6
8	1281	977	6

Table 2-3: **Resource Utilization for GTHE3 Devices (XCVU095 FFVD 1924 -2 E ES1)**

Number of Transceivers	FF	LUTs	BUFG	BUFG_GT
1	440	252	3	1
2	711	424	3	2
3	982	658	3	3
4	1253	854	3	4
5	1524	1050	3	5
6	1795	1246	3	6
7	2066	1447	3	7
8	2337	1643	3	8
9	2608	1839	3	9
10	2879	2035	3	10
11	3150	2231	3	11
12	3421	2432	3	12

Port Descriptions

This section contains details about the JESD204 PHY ports.

Clock and Reset Ports

The clock and reset ports available on the delivered core component depend on the Shared Logic selection when customizing the core. Table 2-4 lists the ports available regardless of core settings.

Table 2-4: **Common Clock and Reset Ports**

Signal Name	Direction	Description
Clocks		
tx_core_clock	In	JESD204 core logic clock used to drive txusrclk2 of transceiver. Frequency = serial line rate/40
rx_core_clock	In	JESD204 core logic clock used to drive rxusrclk2 of transceiver. Frequency = serial line rate/40
txoutclk	Out	Output clock from transceiver. Can be used as JESD204 core clock when in Subclass 0 mode.
rxoutclk	Out	Output clock from transceiver. Can be used as JESD204 core clock when in Subclass 0 mode.
Resets		
tx_reset_gt	In	Core asynchronous logic reset.
rx_reset_gt	In	Core asynchronous logic reset.

Table 2-5 lists the ports that are available only when using shared logic in the example design.

Table 2-5: **Clocks and Resets for Shared Logic in Example Design**

Signal Name[(1)]	Direction	Description
Clocks		
txusrclk	In	Present only on GTP devices. Input Clock to transceiver.
rxusrclk	In	Present only on GTP devices. Input Clock to transceiver.
commonM_qpll_clk_in	In	Clock input for the QPLL (Quad M). Always present.
commonM_qpll_refclk_in	In	Clock input for the QPLL (Quad M). Always present.
commonM_pll0_clk_in	In	Clock input for the PLL (Quad M). Only present when PLL0 is selected.
commonM_pll0_refclk_in	In	Clock input for the PLL (Quad M). Only present when PLL0 is selected.
commonM_pll1_clk_in	In	Clock input for the PLL (Quad M). Only present when PLL0 is selected.
commonM_pll1_refclk_in	In	Clock input for the PLL (Quad M). Only present when PLL1 is selected.
commonM_qpll0_clk_in	In	Clock input for the QPLL (Quad M). Only present when QPLL0 is selected.
commonM_qpll0_refclk_in	In	Clock input for the QPLL (Quad M). Only present when QPLL0 is selected.
commonM_qpll1_clk_in	In	Clock input for the QPLL (Quad M). Only present when QPLL1 is selected.
commonM_qpll1_refclk_in	In	Clock input for the QPLL (Quad M). Only present when QPLL1 is selected.

Table 2-5: **Clocks and Resets for Shared Logic in Example Design *(Cont'd)***

Signal Name[1]	Direction	Description
Resets		
qpll_reset_out	Out	Reset output from transceiver logic to reset Common Block. Present only when QPLL selected.
commonM_pll0_reset_out	Out	Reset output from transceiver logic used to reset Common Block. Only present when PLL0 selected.
commonM_pll1_reset_out	Out	Reset output from transceiver logic used to reset Common Block. Only present when PLL1 selected.
pll_reset_out	Out	Reset output from transceiver used to reset Common Block. Only present on UltraScale devices.
mmcm_reset	Out	Reset output from transceiver to reset MMCM. Only present for GTP devices.

1. M=Number of QUADs – 1

Table 2-6 lists the ports that are available only when using shared logic in the core.

Table 2-6: **Clocks for Shared Logic in Core**

Signal Name[1]	Direction	Description
Clocks		
commonM_qpll_clk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL enabled.
commonM_qpll_refclk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL enabled.
commonM_qpll_lock_out	Out	Lock output from the QPLL (Quad M). Only present when QPLL is enabled.
commonM_pll0_clk_out	Out	Clock output from the PLL (Quad M). Only present when PLL0 is enabled.
commonM_pll0_refclk_out	Out	Clock input from the PLL (Quad M). Only present when PLL0 is enabled.
commonM_pll0_lock_out	Out	Lock output from the PLL0 (Quad M). Only present when PLL0 is enabled.
commonM_pll1_clk_out	Out	Clock output from the PLL (Quad M). Only present when PLL0 is enabled.
commonM_pll1_refclk_out	Out	Clock output from the PLL (Quad M). Only present when PLL1 is enabled.
commonM_pll1_lock_out	Out	Lock output from the PLL1 (Quad M). Only present when PLL1 is enabled.
commonM_qpll0_clk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL0 is enabled.
commonM_qpll0_refclk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL0 is enabled.

Table 2-6: **Clocks for Shared Logic in Core *(Cont'd)***

Signal Name[1]	Direction	Description
commonM_qpll0_lock_out	Out	Lock output from the QPLL0 (Quad M). Only present when QPLL0 is enabled.
commonM_qpll1_clk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL1 is enabled.
commonM_qpll1_refclk_out	Out	Clock output from the QPLL (Quad M). Only present when QPLL1 is enabled.
commonM_qpll1_lock_out	Out	Lock output from the QPLL1 (Quad M). Only present when QPLL1 enabled.

1. M=Number of QUADs – 1

Transceiver Interface Ports - TX

The transceiver ports available on the delivered core component depend on the Shared Logic selection when customizing the core; see Table 2-7 or Table 2-8.

Table 2-7: **Transceiver Interface Ports - Shared Logic in Example Design**

Signal Name	Direction	Description
gt*N*_txdata[31:0]	In	TX data to transceiver. *N* = 0 ... [Lanes-1]
gt*N*_txcharisk[3:0]	In	TX Char is K to transceiver. *N* = 0 ... [Lanes-1]
gt_prbssel[2:0][1]	In	PRBS select to transceiver.

1. For UltraScale devices, the width of gt_prbssel is [3:0].

Table 2-8: **TX Core: Transceiver Interface Ports - Shared Logic in Core**

Signal Name	Direction	Description
txp_out[N:0]	Out	Positive differential serial data output N = (Lanes - 1)
txn_out[N:0]	Out	Negative differential serial data output N = (Lanes - 1)

Transceiver Interface Ports - RX

The transceiver ports available on the delivered core component depend on the Shared Logic selection when customizing the core; see Table 2-9 or Table 2-10.

Table 2-9: **Transceiver Interface Ports - Shared Logic in Example Design**

Signal Name	Direction	Description
gt*N*_rxdata[31:0]	Out	RX data from transceiver. *N* = 0 ... [Lanes-1]
gt*N*_rxcharisk[3:0]	Out	RX Char is K from transceiver. *N* = 0 ... [Lanes-1]
gt*N*_rxdisperr[3:0]	Out	RX disparity error from transceiver. *N* = 0 ... [Lanes-1]
gt*N*_rxnotintable[3:0]	Out	RX Not In Table from transceiver. *N* = 0 ... [Lanes-1]

Table 2-10: **RX Core: Transceiver Interface Ports - Shared Logic in Core**

Signal Name	Direction	Description
rxp_in[N:0]	In	Positive differential serial data input N = (Lanes - 1)
rxn_in[N:0]	In	Negative differential serial data input N = (Lanes - 1)

Transceiver Debug Interface

The transceiver debug interface (when present) provides access to transceiver control and status pins for debug purposes. See the appropriate transceiver user guide (*UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 5], *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 6] or *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 7]) for a detailed description of these pins. This interface is only present on the core when **Include Shared Logic in core** and **Additional transceiver control and status ports** options are selected when generating the core.

Table 2-11: **Optional Transceiver Debug Ports (7 Series Devices)**

Signal Name(1)(2)	Direction	Description
gtN_loopback[2:0]	In	Transceiver loopback: • 000: No loopback • 001: Near-End PCS Loopback • 010: Near-End PMA Loopback • 100: Far-End PMA Loopback • 110: Far-End PCS Loopback
gtN_txpostcursor[4:0]	In	Transmit Differential Driver control. (TX only)
gtN_txprecursor[4:0]	In	Transmit Differential Driver control. (TX only)
gtN_txdiffctrl[3:0]	In	Transmit Differential Driver control. (TX only)
gtN_txpolarity	In	Transmit polarity control. (TX only)
gtN_rxpolarity	In	Receive polarity control. (RX only)
gtN_cplllock_out	Out	Active-High signal indicating that the channel PLL has locked to the input reference clock
gtN_eyescandataerror_out	Out	Asserted when an EYESCAN error occurs
gtN_eyescanreset_in	In	This port is pulsed High to initiate the EYESCAN reset process
gtN_eyescantrigger_in	In	A High on this port causes an EYESCAN trigger event
gtN_rxbufreset_in	In	This port is driven High and then deasserted to start the RX elastic buffer reset process.
gtN_rxbufstatus_out[2:0]	Out	RX Elastic Buffer Status
gtN_rxbyteisaligned_out	Out	RX Byte Alignment Status
gtN_rxbyterealign_out	Out	RX Byte Alignment has changed
gtN_rxcdrhold_in	In	Hold the CDR control loop frozen

Table 2-11: **Optional Transceiver Debug Ports (7 Series Devices) *(Cont'd)***

Signal Name[1][2]	Direction	Description
gtN_rxcommadet_out	Out	RX Comma detect out
gtN_rxdfelpmreset_in	In	DFE reset
gtN_rxlpmen_in	In	LPM mode enable
gtN_rxmonitorout_out	Out	RX Monitor Out
gtN_rxmonitorsel_in	In	RX Monitor Out mode select
gtN_rxpcsreset_in	In	PCS Reset
gtN_rxpd_in[1:0]	In	RX Power Down
gtN_rxpmareset_in	In	PMA Reset
gtN_rxprbscntreset_in	In	RX PRBS Counter reset
gtN_rxprbserr_out	Out	RX PRBS Error detect
gtN_rxprbssel_in	In	RX PRBS Select
gtN_rxresetdone_out	Out	RX Reset Done.
gtN_rxstatus_out[2:0]	Out	Encodes RX status and error codes
gtN_txbufstatus_out[1:0]	Out	TX Elastic Buffer Status
gtN_txpcsreset_in	In	TX PCS Reset
gtN_txpd_in	In	TX Power Down
gtN_txpmareset_in	In	TX PMA Reset
gtN_txprbsforceerr_in	In	TX PRBS Force Error
gtN_txresetdone_out	Out	TX Reset Done
gtN_rxlpmhfhold_in	In	(GTP only) LPM mode control
gtN_rxlpmhfoverden_in	In	(GTP only) LPM mode control
gtN_rxlpmlfhold_in	In	(GTP only) LPM mode control

Notes:

1. N is the number of the transceiver channel.
2. If you are migrating from a 7 series to an UltraScale architecture-based device, the prefixes of the optional transceiver debug ports for single-lane cores are changed from `gt0`, `gt1` to `gt`, and the postfix `_in` and `_out` are dropped. For multi-lane cores, the prefixes of the optional transceiver debug ports `gt(n)` are aggregated into a single port (see Table 2-12).

Table 2-12: **Optional Transceiver Debug Ports (UltraScale Architecture-Based Devices)**

Signal Name[1]	Direction	Description
gtN_drpaddr [8:0]	In	DRP address bus
gtN_drpdi [15:0]	In	Data bus for writing configuration data from the FPGA logic resources to the transceiver
gtN_drpen	In	DRP enable signal • 0: No read or write operation performed • 1: Enables a read or write operation

Table 2-12: **Optional Transceiver Debug Ports (UltraScale Architecture-Based Devices) *(Cont'd)***

Signal Name[(1)]	Direction	Description
gtN_drpwe	In	DRP write enable • 0: Read operation when DEN is 1 • 1: Write operation when DEN is 1
gtN_drpdo [15:0]	Out	Data bus for reading configuration data from the GTX/GTH transceiver to the FPGA logic resources.
gtN_drprdy	Out	Indicates operation is complete for write operations and data is valid for read operations
gt_txpmareset [(LANES-1):0]	In	This port is pulsed High to start the TX PMA reset process
gt_txpcsreset [(LANES-1):0]	In	This port is pulsed High to start the TX PCS reset process
gt_txresetdone [(LANES-1):0]	Out	A High on this port indicates that the TX reset process has completed
gt_rxpmareset [(LANES-1):0]	In	This port is pulsed High to start the RX PMA reset process
gt_rxpcsreset [(LANES-1):0]	In	This port is pulsed High to start the RX PCS reset process
gt_rxbufreset [(LANES-1):0]	In	This port is driven High and then deasserted to start the RX elastic buffer reset process
gt_rxpmaresetdone [(LANES-1):0]	Out	A High on this port indicates that the RX PMA reset process has completed
gt_rxresetdone [(LANES-1):0]	Out	A High on this port indicates that the RX reset process has completed
gt_txbufstatus [(LANES*2)-1:0]	Out	Elastic Buffer Status
gt_rxbufstatus [(LANES*3)-1:0]	Out	RX Elastic Buffer Status
gt_cplllock [(LANES-1):0]	Out	Active-High signal indicating that the channel PLL has locked to the input reference clock
gt_rxrate [(LANES*3)-1:0]	In	Link signaling rate control
gt_eyescantrigger [(LANES-1):0]	In	A High on this port causes an EYESCAN trigger event
gt_eyescanreset [(LANES-1):0]	In	This port is pulsed High to initiate the EYESCAN reset process
gt_eyescandataerror [(LANES-1):0]	Out	Asserted when an EYESCAN error occurs

Table 2-12: **Optional Transceiver Debug Ports (UltraScale Architecture-Based Devices) *(Cont'd)***

Signal Name[1]	Direction	Description
gt_loopback [(LANES*3)-1:0]	In	Transceiver loopback: • 000: No loopback • 001: Near-End PCS Loopback • 010: Near-End PMA Loopback • 100: Far-End PMA Loopback • 110: Far-End PCS Loopback
gt_rxpolarity [(LANES-1):0]	In	Set High to invert the incoming serial data
gt_txpolarity [(LANES-1):0]	In	Set High to invert the outgoing serial data
gt_rxdfelpmreset [(LANES-1):0]	In	Reset for the LPM and DFE datapath
gt_rxlpmen [(LANES-1):0]	In	Set to 1 to select the LPM datapath
gt_txprecursor [(LANES*5)-1:0]	In	Transmitter pre-cursor pre-emphasis control
gt_txpostcursor [(LANES*5)-1:0]	In	Transmitter post-cursor pre-emphasis control
gt_txdiffctrl [(LANES*4)-1:0]	In	Driver swing control
gt_txprbsforceerr [(LANES-1):0]	In	Set High to drive errors into the PRBS transmitter
gt_rxprbssel [(LANES*4)-1:0]	In	Receiver PRBS checker test pattern control
gt_rxprbserr [(LANES-1):0]	In	A High on this port indicates that PRBS errors have occurred
gt_rxprbscntreset [(LANES-1):0]	In	Reset the PRBS error counter
gt_rxcdrhold [(LANES-1):0]	In	Hold the CDR control loop frozen
gt_dmonitorout [(LANES*15-1):0]	Out	Digital Monitor Output Bus
gt_rxdisperr [(LANES*4-1):0]	Out	Receiver disparity error indicator
gt_rxnotintable [(LANES*4-1):0]	Out	Receiver not in table error indicator
gt_rxcommadet [(LANES-1):0]	Out	A High on this port indicates that the comma alignment block has detected a valid comma
gt_rxpd [(LANES-1):0]	In	RX Power Down
gt_txpd [(LANES-1):0]	In	TX Power Down

1. N is the number of the transceiver channel.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core. The JESD204 PHY core can be used in two modes:

- The JESD204 PHY core is instantiated automatically by the JESD204 core during generation. This is transparent, and all ports and parameters are controlled by the JESD204 IP. Using the IP in this mode requires no user intervention and is not described in this document; see the *JESD204 Product Guide* (PG066) for details about this mode [Ref 2]. This mode is fully supported for production systems except in UltraScale™ devices.
- The JESD204 PHY core is instantiated in the example design provided with the JESD204 IP as a stand-alone IP core. In this case, the JESD204 PHY IP top level is available directly for instantiation in designs, and the JESD204 PHY IP GUI is available. This chapter describes using the JESD204 PHY in this mode.

  Note: This mode is provided as an example only and is pre-production. It is not recommended for use in production systems in any device.

General Design Guidelines

This section includes tips about getting started withe the JESD204 PHY core.

Use the Example Design as a Starting Point

Each instance of the JESD204 PHY core created by the Vivado® Design Suite is delivered with an example design that can be implemented in an FPGA and simulated. This design can be used as a starting point for your own design or can be used to troubleshoot your application, if necessary.

See Chapter 5, Example Design for information about using and customizing the example designs for the JESD204 PHY core.

Degree of Difficulty

JESD204 designs are challenging to implement in any technology, and the degree of difficulty is further influenced by:

- Maximum system clock frequency
- Targeted device architecture
- Nature of your application

All JESD204 implementations require careful attention to system performance requirements. Pipelining, logic mapping, placement constraints, and logic duplication are all methods that help boost system performance.

Clocking

This section describes the options available for clocking the JESD204 PHY core and the transceiver(s). The following clocks are used in the JESD204 PHY core.

- **DRP Clock (UltraScale Devices Only)**: The GTHE3 UltraScale device transceiver requires an auxiliary clock for internal use and also for the reset state machines within the JESD204 PHY core. See the appropriate device family data sheet for the min and max DRP clock frequencies permitted.
- **Core Clock**: The JESD204 PHY core operates using a 32-bit (4-byte) datapath. The device clock for the core logic therefore runs at one quarter of the byte clock rate (1/40th of the serial line rate). For the JESD204 and JESD204 PHY cores, this is referred to as the core clock.
- **Reference Clock**: The GTP/GTX/GTH serial transceivers require a stable, low-jitter reference clock that has a device and speed grade dependant range. In some circumstances, the same source clock can supply both the reference clock and core clock. Two reference clocks are required if both CPLL and QPLL are selected in the GUI.

Resets

Separate resets are provided for transmit and receive directions. This enables the JESD204 PHY core to be used by a transmit JESD204 link and a receive JESD204 link independently. There is no system reset. The system reset will cause the JESD204 cores attached to the JESD204 PHY to reset the JESD204 PHY.

- **Transmit Reset**: The transmit reset input initiates a complete transceiver reset sequence for the transmit logic, and `tx_reset_done` is asserted when the reset sequence is complete.
- **Receive Reset**: The receive reset input initiates a complete transceiver reset sequence for the receive dlogic, and `rx_reset_done` is asserted when the reset sequence is complete.

Protocol Description

See the *JESD204 Product Guide* (PG066) for a full description of the protocol [Ref 2].

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado® Design Suite.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5].

Note: Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Configuration Tab

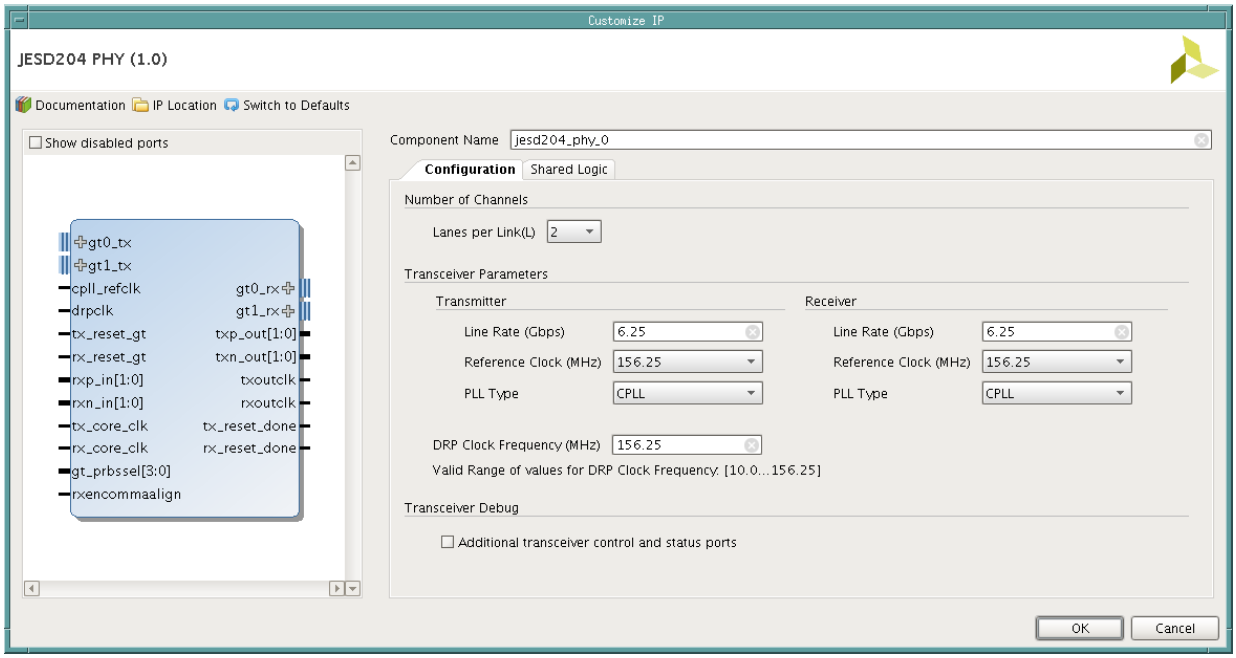

Figure 4-1: **Configuration Tab**

- **Number of Channels**:
  - **Lanes per Link**: The core supports 1 to 12 lanes. The number of transmit lanes always matches the number of receive lanes. For asymmetric interfaces, multiple cores can be generated and multiple PHY cores can be connected to a single JESD204 core.
- **Transceiver Parameters, Transmitter and Receiver**:
  - **Line Rate**: The serial line rate in Gbps can be selected for transmit and receive independently. The minimum rate is 1 Gbps and the maximum depends on the chosen device and speed grade.
  - **Reference Clock**: The reference clock must be selected from the drop-down list, which presents a list of valid reference clocks for the selected line rate. Independent reference clocks can only be selected if different PLLs are selected for transmit and receive.
  - **PLL Type**: Select the QPLL or CPLL for transmit and receive. See the appropriate device transceiver user guide for more details and limitations.
  - **DRP Clock Frequency**: The frequency of the DRP clock being applied to the core so reset delays can be adjusted be the reset state machines.
- **Transceiver Debug**: Select to include additional transceiver control and status ports for debugging purposes. See Transceiver Debug Interface in Chapter 2 for more information.

Shared Logic Tab

The JESD204 PHY can be generated with shared logic included in the core or with shared logic included with the example design. Shared logic should always be included in the core when using the JESD204 PHY with a JESD204 IP core.

User Parameters

Table 4-1 shows the relationship between the GUI fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl console).

Table 4-1: **GUI Parameter to User Parameter Relationship**(1)

GUI Parameter/Value	User Parameter/Value	Default Value
Lanes per Link	C_LANES	2
Line Rate		
Transmit	GT_Line_Rate	6.25
Receive	RX_GT_Line_Rate	6.25
Reference Clock		
Transmit	GT_REFCLK_FREQ	156.25
Receive	RX_GT_REFCLK_FREQ	156.25
PLL Type		
Transmit	C_PLL_SELECTION	0
Receive	RX_PLL_SELECTION	0
DRP Clock Frequency	DRPCLK_FREQ	10.0
Shared Logic	SupportLevel	1
Transceiver Debug	TransceiverControl	false

1. Parameters and default values will differ based on the selected device.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Constraining the Core

This section describes how to constrain a design containing the JESD204 core. This is accomplished by using the XDC delivered with the core at generation time. An additional XDC file is generated with the IP example design; only the core XDC file should be used in user designs.

Required Constraints

This section defines the constraint requirements for the core. Constraints are provided in several XDC files which are delivered with the core and the example design to give a starting point for constraints for the user design.

There are four XDC constraint files associated with this core:

- `<corename>_example_design.xdc`
- `<corename>_ooc.xdc`
- `<corename>.xdc`

The first is used only by the example design; the second file is used for Out Of Context support where this core can be synthesized without any wrappers; the third file is the main XDC file for this core.

Clock Frequencies

The reference clock and core clock frequency constraints vary depending on the selected line rate and reference clock when generating the core. See the generated XDC for details.

Clock Domains

There are also several paths where clock domains are crossed. These include the management interface. See the generated XDC file for details.

Clock Management

Reference clock and core clock resources require location constraints appropriate to your top level design.

Clock Placement

Reference clock input should be given location constraints appropriate to your top level design and to the placement of the transceivers.

Core clock input (if required) should be given location constraints appropriate to your top level design.

Banking

All ports should be given location constraints appropriate to your top level design within banking limits.

Transceiver Placement

Transceivers should be given location constraints appropriate to your design. In some cases, example transceiver location constraints can be found in the example design XDC file. For 7 series devices, the GT location constraints are in the transceiver's XDC file.

I/O Standard and Placement

All ports should be given I/O standard and location constraints appropriate to your top level design.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6].

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

The JESD204 PHY core is not intended to be used as a standalone solution. However, an example design does exist for the IP core. The example design is a lightweight harness that can operate in external TX to RX loopback or as independent RX/TX channel mode. See the example design provided with the JESD204 IP for a more detailed example of the use of the JESD204 PHY IP core [Ref 2].

To open the example design, right-click on the IP and select **Open IP Example Design** as shown in Figure 5-1.

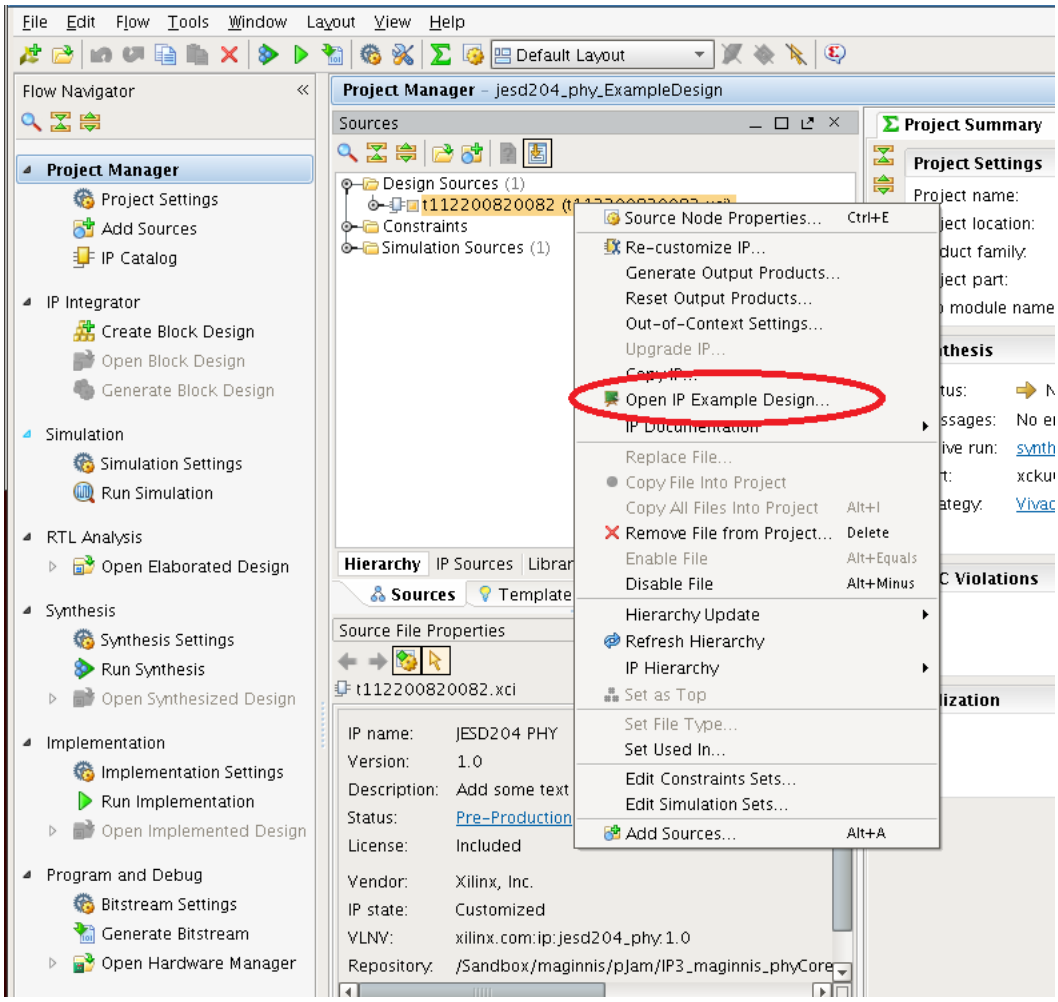

Figure 5-1: **Opening the Example Design**

The example design generates data internally for the TX path. This is checked externally and can also be fed back into the RX path, where a simple check function exists to verify the incoming data is 8'hBC.

The clks_in module places the appropriate clock buffers on the clock paths dependent on the technology chosen.

The sequencer is responsible for indicating when the example design can test the incoming data as well as sequencing the data that is transmitted. When both the RX and TX channels are out of reset, it sends out K28.5 symbols. These are followed by four /R/..../A/ frames mimicking what is seen on a JESD204 data interface. Note /Q/ and the 14 bytes of /Q/ data are not sent. They just increment counter values.

Figure 5-2 shows a block diagram for the example design.

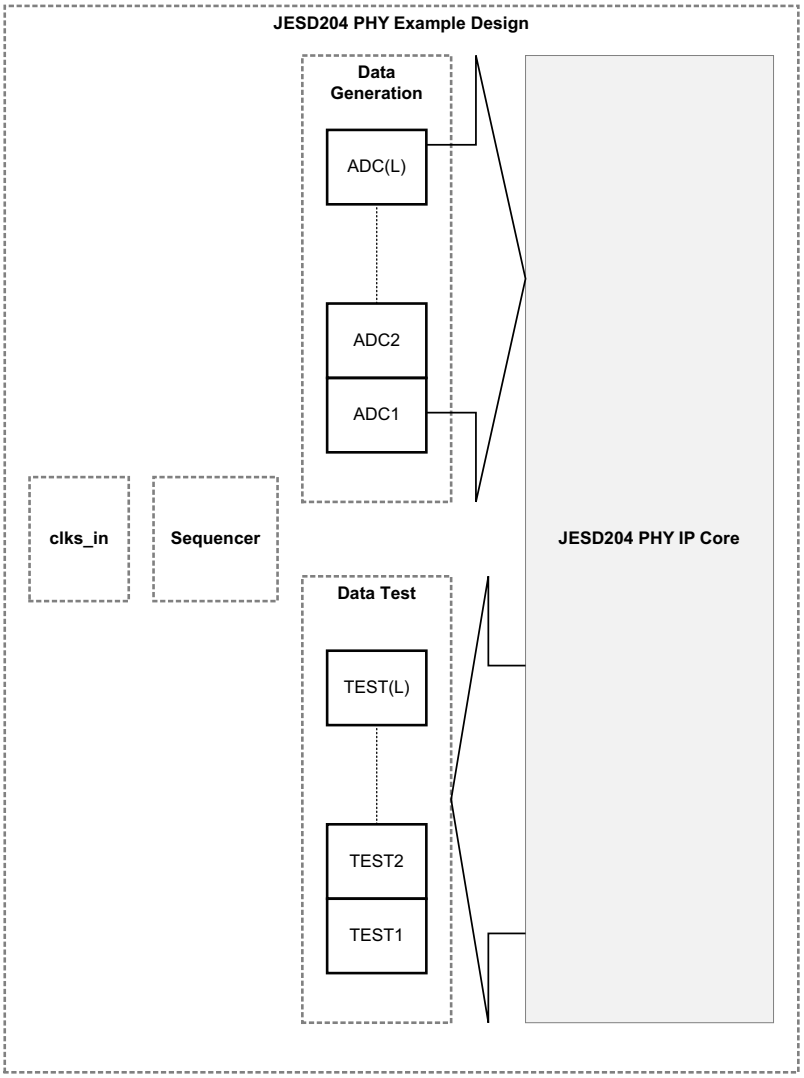

Figure 5-2: **Example Design Block Diagram**

Figure 5-3 and Figure 5-4 show the clock structure for different and identical PLL types, respectively.

TIP: *If different PLLs are selected for the RX and TX paths, the port names for refclk are named as "rx" and "tx". If they are the same, the port is named as "common."*

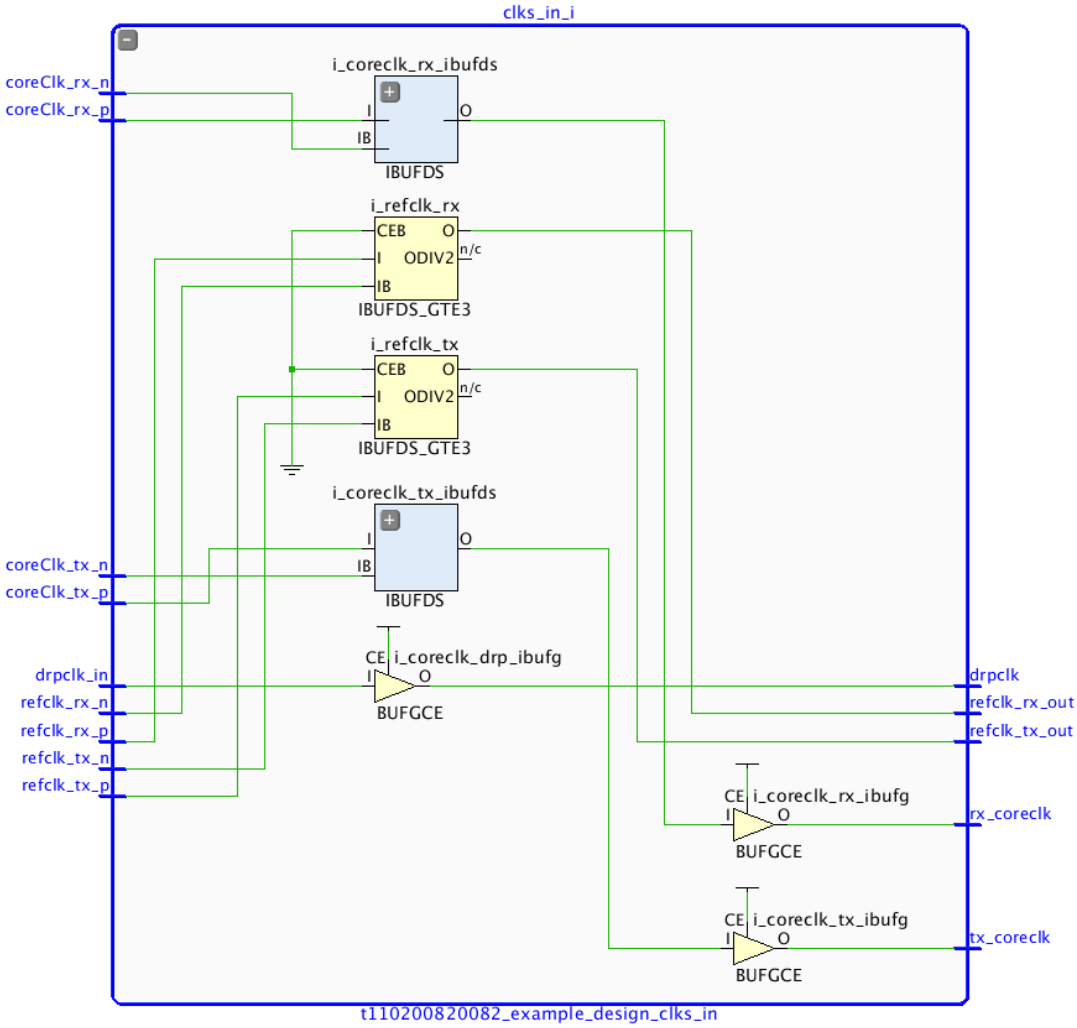

Figure 5-3: **Clock Structure with Different PLL Types**

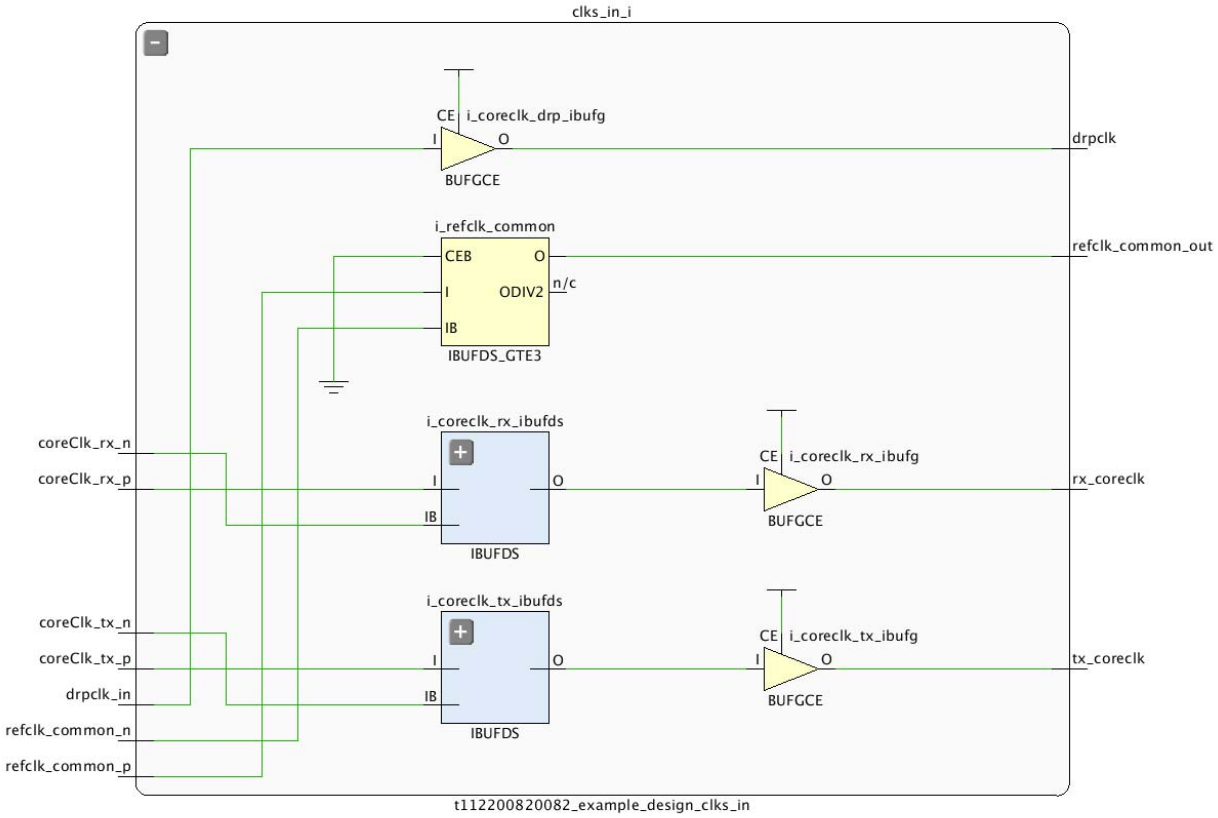

Figure 5-4: **Clock Structure with Same PLL Types**

Test Bench

This chapter contains information about the test bench provided in the Vivado® Design Suite. Figure 6-1 shows the test bench block diagram

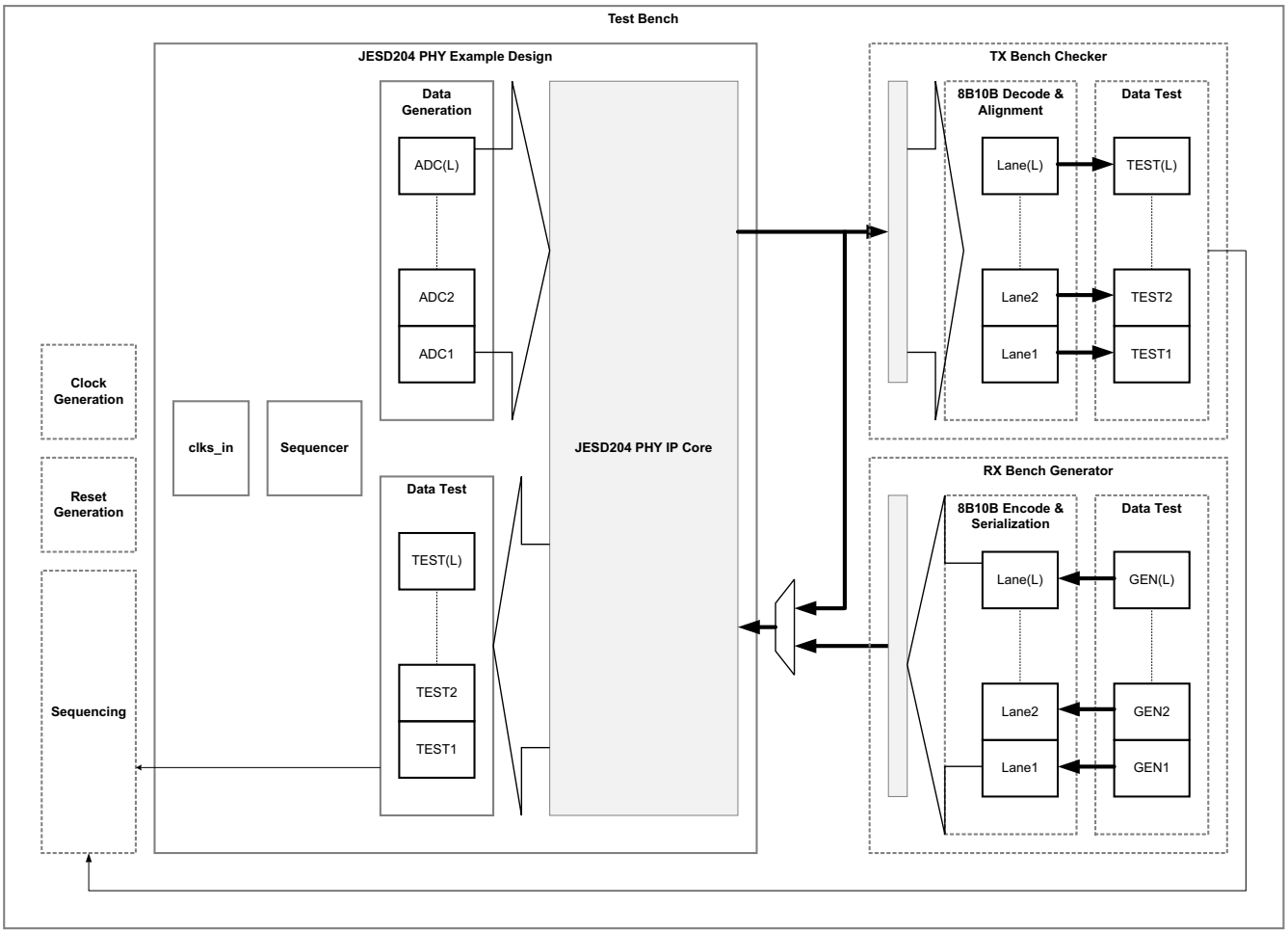

Figure 6-1: **Test Bench Block Diagram**

Hierarchy is used extensively to create per-lane stimulus and checker blocks which allow easier signal viewing in the waveform window.

The test bench provides all clocks required by the design. If the TX and RX line rates are equal, the loopback path is automatically selected for simulation at IP build time.

Several event messaging functions exist at the top level. These indicate when the lanes are out of reset and the bit rates used by the RX and TX channels. A timeout function is also included.

The data generation and testing functions exist in separate modules instantiated in the top level test bench. This enables clear navigation to a lane's data stream with the waveform viewer. The data stream starts when both the TX and RX paths are out of reset. K28.5 (/K/) symbols are transmitted to allow the transceivers to bit align.

An ILA-type sequence, consisting of just the K28.0 (/R/), K28.3 (/A/) and data, is sent to allow the test bench to align to a 32-bit boundary. The bench continues to run for a specified length of core clock cycles before finishing.

IMPORTANT: *To change any IP parameters, you must reconfigure the IP and regenerate the example design.*

Verification, Compliance, and Interoperability

The JESD204 core has been verified using both simulation and hardware testing.

Simulation

A highly parameterizable transaction-based simulation test suite has been used to verify the core. Tests include:

- scrambling and alignment
- loss and regain of synchronization
- frame transmission
- frame reception
- recovery from error conditions

Hardware Testing

The core has been used in many hardware test platforms within Xilinx and in interoperability testing with external hardware vendors.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the JESD204 PHY, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the JESD204 PHY. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx® Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the JESD204 PHY Core

AR: 61911

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Additional Resources.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Log in to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address JESD204 PHY design issues. It is important to know which tools are useful for debugging various situations.

Vivado Lab Tools

Vivado® lab tools insert logic analyzer and virtual I/O cores directly into your design. Vivado lab tools also allow you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 22].

Reference Boards

Various Xilinx development boards support theJESD204 PHY. These boards can be used to prototype designs and establish that the core can communicate with the system.

7 Series FPGA Evaluation Boards

- AC701
- KC705
- ZC706
- VC709

Simulation Debug

The simulation debug flow for Questa® SIM is illustrated in Figure B-1. A similar approach can be used with other simulators.

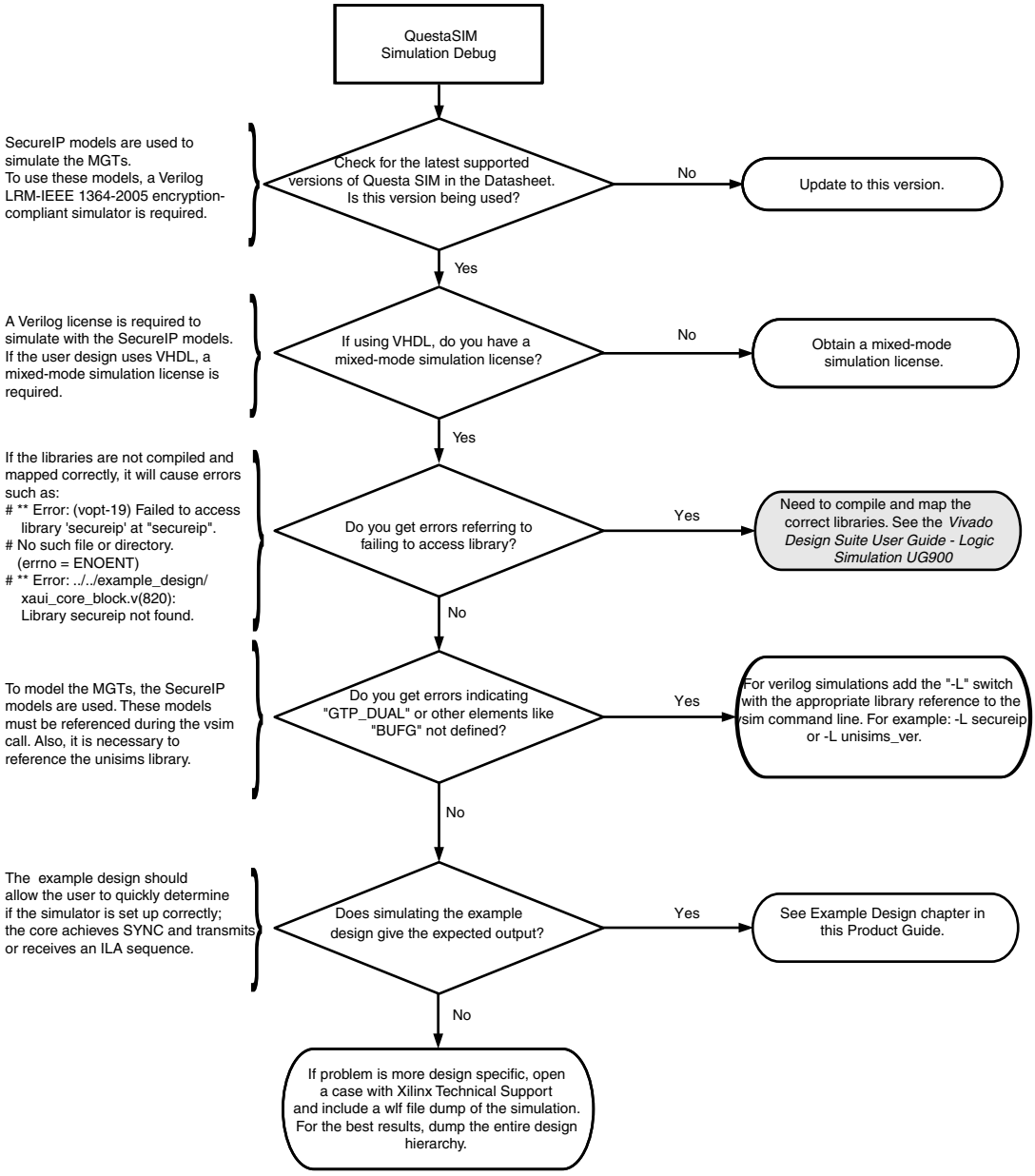

Figure B-1: **Questa SIM Debug Flow Diagram**

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado lab tools are a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the Vivado lab tools for debugging the specific problems.

General Checks

- Ensure that all the timing constraints for the core were met during implementation.
- Ensure that all clock sources are clean and in particular that the transceiver reference clocks meet the GTX/GTH/GTP transceiver requirements from the appropriate FPGA Data Sheet.
- Ensure that all GTX/GTH/GTP transceiver PLLs have obtained lock by monitoring the QPLLLOCK_OUT and/or CPLLLOCK_OUT port either using the Vivado lab tools or by routing the signals to a spare pin.
- Ensure that when regenerating a new GTX/GTH/GTP transceiver the reference clock of the new transceiver matches that of the design.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *Serial Interface for Data Converters* (JESD204B)
2. *JESD204 Product Guide* (PG066)
3. *Vivado® Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
4. *Vivado Design Suite User Guide: Designing with IP* (UG896)
5. *Vivado Design Suite User Guide: Getting Started* (UG910)
6. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
7. *ISE® to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
9. *Vivado Design Suite User Guide: Implementation* (UG904)
10. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
11. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
12. *7 Series FPGAs GTP Transceivers User Guide* (UG482)
13. *Artix-7 FPGAs Data Sheet* (DS181)
14. *Kintex-7 FPGAs Data Sheet* (DS182)
15. *Virtex-7 T and XT FPGAs Data Sheet* (DS183)
16. *Kintex UltraScale Architecture Data Sheet* (DS892)
17. *Virtex UltraScale Architecture Data Sheet* (DS893)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/01/2014	1.0	Initial Xilinx release.

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