LogiCORE IP 3GPP LTE Channel Estimator v2.0

PB022 (v2.0) November 18, 2015 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP 3GPP LTE Channel Estimator v2.0 implements AXI4-Stream compliant, channel estimation functionality suitable to support decoding of the Physical Uplink Shared Channel (PUSCH) in LTE eNodeB applications as defined in 3GPP TS 36.211 specification. It represents one IP component in the Xilinx broader LTE Baseband Targeted Design Platform (TDP).

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/chest_lte_eval/index.htm

Features

- Drop-in module for UltraScale architecture-based, Zynq-7000, Virtex-7, and Kintex-7 devices
- Support of channel estimation for 3GPP LTE Physical Uplink Shared Channel (PUSCH) with Single-Input, Single-Output (SISO) and Single-Input, Multiple-Output (SIMO) communication modes, Multi-User Multiple Input Multiple Output (MU-MIMO) communication modes
- Compliance with 3GPP-LTE TS 36.211 v9.0 (Release 9) standard specifications
- Parameterizable input/output data precision
- Bit accurate C language simulation model for system-level modeling

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™ Families, UltraScale™ Architecture, Zynq®-7000 All Programmable SoC, Virtex®-7, Kintex®-7
Supported User Interfaces	AXI4-Stream
Provided with Core	
Design Files	RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Bit Accurate C Model
Supported S/W Driver	Not Provided
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Applications

Base station applications implementing eNodeB following the LTE specifications (3GPP TS 36.211). The 3GPP LTE Channel Estimator core performs the channel estimation function required for decoding of the PUSCH uplink data transmission in SISO and MU-MIMO modes of communication.

Technical Support

Xilinx provides technical support at Xilinx Support web page for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the 3GPP LTE Channel Estimator product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
11/18/2015	2.0	Added support for UltraScale+ families.
06/04/2014	2.0	Initial Xilinx release. This document replaces XMP119.

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