LogiCORE IP 3GPP LTE MIMO Encoder v3.0

XMP026 January 18, 2012 **Product Brief**

Introduction

The Xilinx® 3GPP LTE MIMO Encoder v3.0 core implements multiple-input, multiple-output (MIMO) encoding for LTE eNodeB applications as defined in the 3GPP TS 36.211 v.9.1 specification [Ref 1]. It represents one IP component in the Xilinx broader LTE Baseband Platform.

Features

- AXI4-Stream compliant interfaces
- Implements layer mapping and pre-coding as defined in the 3GPP TS 36.211 v.9.1 specification [Ref 1]
- Supports both Transmit Diversity and Spatial Multiplexing encoding schemes
- Cyclic Delay Diversity option
- Supports 2 and 4 antennas
- Maximum theoretical throughput supported for systems with up to 20 MHz bandwidth
- Parameterizable input/output data precision
- Optimized for Xilinx high performance Virtex®-6 FPGAs

Applications

The 3GPP LTE MIMO Encoder v3.0 can be used for the following applications:

- Base station applications implementing eNodeB following the LTE specification [Ref 1]. The LTE MIMO Encoder v3.0 can perform the MIMO-encoding functions for downlink transmission.
- Applications that use any of the downlink MIMO-encoding schemes of the LTE specification [Ref 1].

Theory of Operation

The LTE MIMO Encoder is to be part of the eNodeB, the downlink baseband processing that encompasses layer mapping and pre-coding as defined in [Ref 1]. Figure 1 shows a high-level view of the functionality included in this product.

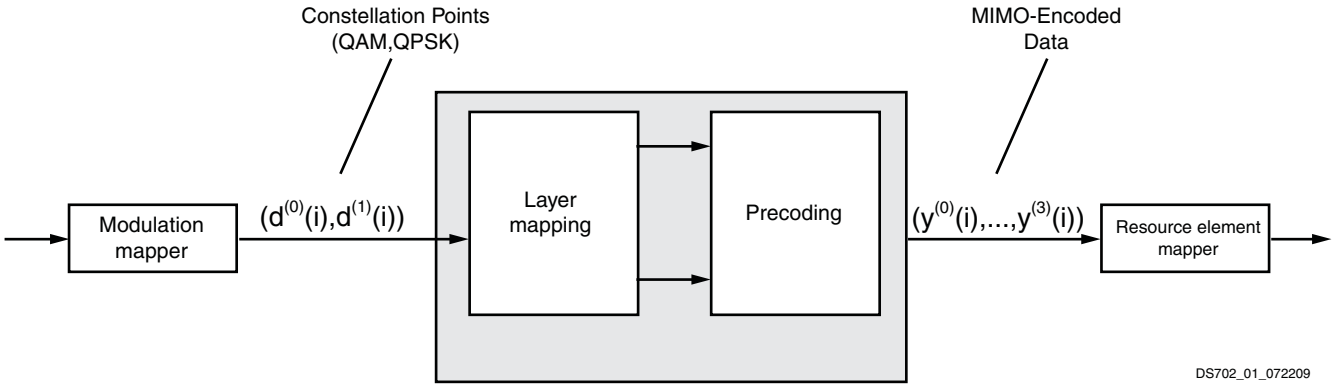

Figure 1: **LTE MIMO Encoder v3.0 Functionality**

C Model

The LTE 3GPP MIMO Encoder core has a bit-accurate C model designed for system modeling. The model is bit-accurate but not cycle-accurate, so it produces exactly the same output data as the core on a code-word by code-word basis. However, it does not model the core latency or interface signals.

The bit accurate behavioral C model of the LTE MIMO Encoder v3.0 and associated user guide are available to customers. The C model is provided as a dynamically linked library for Windows 32-bit and 64-bit Linux platforms. A README.txt file describes the contents of the installed directory structure and any further platform-specific installation instructions.

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_mimo_enc_eval/index.htm.

References

1. Third Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 9), 3GPP TS 36.211 V9.1.0 (2010-03).

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Refer to the IP Release Notes Guide (XTP025) for more information on this core. There will be a link to all DSP IP and then to the relevant core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License and the core is generated using the Xilinx ISE CORE Generator software. The CORE Generator software is shipped with the Xilinx ISE Design Suite software.

For full access to all core functionality in simulation and in hardware, you must purchase a license for the core. Please contact your local Xilinx sales representative for information on pricing and availability of Xilinx LogiCORE IP modules. Information about additional modules is also available at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/17/08	1.0	Xilinx initial release.
09/16/09	2.0	Updated for core version 2.0.
08/15/11	2.1	Updated to include web registration information.
01/18/12	3.0	Added a reference to 3GPP and updated Features section for core version 3.0.

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