Virtex-6 FPGA Memory Interface Solutions

DS186 January 18, 2012 **Product Specification**

Introduction

The Virtex®-6 FPGA memory interface solutions cores provide high-performance connections to DDR3 and DDR2 SDRAMs, QDRII+ SRAM, and RLDRAM II devices. For information about the QDRII+ SRAM, see QDRII+ SRAM, page 4. For information about RLDRAM II devices, see RLDRAM II, page 6.

DDR3 and DDR2 SDRAMs

This section discusses the features, applications, and functional description of Virtex-6 FPGA memory interface solutions in DDR3 and DDR2 SDRAMs. These solutions are available with an optional AXI4 slave interface.

DDR3 SDRAM Features

- 303–533 MHz (606–1066 Mb/s) performance for center column, single-rank interfaces up to 72 bits wide:
  - 400 MHz in a -1 commercial speed grade device
  - 533 MHz in a -2 commercial speed grade device
  - 533 MHz in a -3 commercial speed grade device
- 303 MHz (606 Mb/s) performance for dual-rank interfaces up to 72 bits wide
- Hardware validated
- Component support for interface widths up to 144 bits
- Single- and dual-rank UDIMM, SODIMM, and RDIMM support
- 2 Gb density device support (additional densities supported in the MIG tool using the Create Custom Part feature)
- 8-bank support
- x4, x8, and x16 device support
- 4:1 and 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 144 bits)
- 4-word, 8-word, and "On the Fly" (OTF) burst support

LogiCORE™ IP Facts Table

Core Specifics

Supported Device Family[1]	Virtex-6 FPGA							
Supported Memory	DDR2 Component, DIMM DDR3 Component, DIMM QDRII+ Component, RLDRAM II Component							
Performance (MHz)[2]	**Memory**		**FPGA Commercial Speed Grade**					
			-1		**-2**		**-3**	
			Min	**Max**	**Min**	**Max**	**Min**	**Max**
	DDR3 SDRAM	Component	303	400	303	533	303	533
		DIMM	303	400	303	533	303	533
	DDR2 SDRAM	Component	125	400	125	400	125	400
		RDIMM	125	400	125	400	125	400
	QDRII+ SRAM	Component	120	300	120	350	120	400
	RLDRAM II Memory	Component	175	350	175	400	175	500

Resources	**Product[3]**	**LUTs**	**Flip-Flops**	**BUFG**	**BUFIO**	**MMCM**	**Block RAM**
	Virtex-6 FPGA DDR3 SDRAM	5,889	5,882	3	9	1	0
	Virtex-6 FPGA DDR2 SDRAM	4,418	4,630	3	9	1	0
	Virtex-6 FPGA QDRII+ SRAM	2,887	3.460	3	4	1	RAMB18-2
	Virtex-6 FPGA RLDRAM II	3,282	3,774	3	4	1	RAMB36-5 RAMB18-5

Provided with Core

Documentation	Product Specification User Guide
Design Files	Verilog, VHDL
Example Design	Verilog, VHDL
Test Bench	Integrated test bench with memory model and a traffic generator
Constraints File	User constraints file (UCF)
Supported S/W Driver	N/A

Design Tool Requirements

HDL Synthesis[4]	XST v13.4, Synopsys Synplify Pro
Xilinx Implementation Tools	ISE® Design Suite v13.4
Simulation (Behavioral only)[4]	Mentor Graphics ModelSim

Support

Provided by Xilinx @ **www.xilinx.com/support**

Notes:

1. For a complete listing of supported devices, see the release notes for this core.
2. Maximum frequency listed. Implementations might be limited by FPGA column selection and interface data width. Consult the MIG tool and UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide* for more information.
3. This is a 72-bit design. Resource utilization can change depending on the options chosen, or memory device used, or both.
4. For the supported versions of the tools, see the *ISE Design Suite 13: Release Notes Guide*.

- Support for 5 to 9 cycles of column-address strobe (CAS) latency (CL)
- On-die termination (ODT) support
- Support for 5 to 8 cycles of CAS write latency (CWL)
- ZQ calibration – initial and periodic (configurable)
- ECC support
- Write leveling support for DDR3 (fly-by routing topology required for DDR3 component designs)
- JEDEC-compliant DDR3 initialization support
- Source code delivery in Verilog or VHDL
- 2:1 memory to FPGA logic interface clock ratio
- Two controller request processing modes:
  - Normal: reorder requests to optimize system throughput and latency
  - Strict: memory requests are processed in the order received
- Multiple controllers per FPGA supported through the Memory Interface Generator (MIG) tool

DDR2 SDRAM Features

- 125–400 MHz (250–800 Mb/s) performance for single-rank interfaces up to 72 bits wide:
  - 400 MHz in all commercial speed grades
- 150 MHz (300 Mb/s) performance for dual-rank interfaces up to 72 bits wide
- Hardware validated
- Component support for interface widths up to 144 bits
- Single-rank UDIMM, SODIMM, and RDIMM support
- 1 and 2 Gb device support (additional densities supported in the MIG tool using the Create Custom Part feature)
- 4- and 8-bank support
- x4, x8, and x16 device support
- 4:1 and 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 144 bits)
- 4- and 8-word burst support
- Support for 3 to 6 cycles of CL
- ODT support
- ECC support
- JEDEC-compliant DDR2 initialization support
- Source code delivery in Verilog or VHDL
- 2:1 memory to FPGA logic interface clock ratio
- Two controller request processing modes:
  - Normal: reorder requests to optimize system throughput and latency
  - Strict: memory requests are processed in the order received
- Multiple controllers per FPGA supported by running the MIG tool multiple times

AXI4 Slave Interface Features

- AXI4 slave-compliant memory-mapped interface.
- AXI4-Lite interface support for ECC control and status registers.
- 1:1 clock rate to the controller.
- AXI4 interface data width can be 32, 64, 128, or 256 bits wide to correspond with memory data width of 8, 16, 32, 64, or 72 bits.
- Parameterized address width support.
- Support for INCR burst up to 256 data beats.
- WRAP burst support.
- Optional narrow burst support. This can be excluded for optimized area.

Applications

Typical applications for the Virtex-6 FPGA memory interface solutions include the following:

- DDR2 SDRAM interfaces
- DDR3 SDRAM interfaces

Figure 1 shows a high-level block diagram of the Virtex-6 FPGA memory interface solution connecting a user design to a DDR2 or DDR3 SDRAM device. The physical layer (PHY) side of the design is connected to the DDR2 or DDR3 SDRAM device via FPGA I/O blocks (IOBs), and the user interface (UI) side is connected to the user design via FPGA logic. Alternatively, an AXI4 slave interface is available to connect to an AXI4 master (not shown in Figure 1). See UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide* for more details regarding the design.

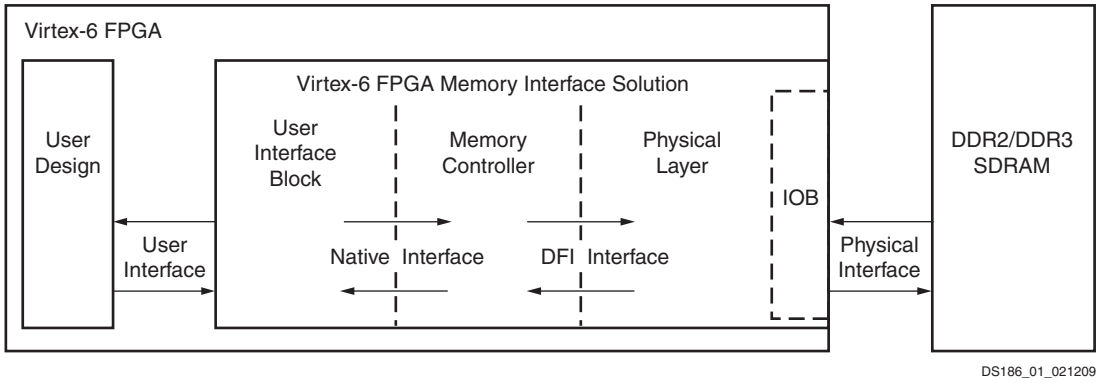

Figure 1: **DDR2/DDR3 SDRAM Memory Interface Solution**

Functional Description

As shown in Figure 1, the top-level functional blocks of the Virtex-6 FPGA memory interface solution include:

- The UI block:
  - Presents the user interface to a user design
  - Provides a simple and user-friendly alternative to the native interface
  - Buffers read and write data
  - Reorders read return data to match the request order

    - Presents a flat address space and translates it to the addressing required by the SDRAM
- The memory controller (MC) block:
    - Receives requests from the user design
    - Reorders requests to minimize dead states for maximum SDRAM performance
    - Manages SDRAM row/bank configuration
    - Performs high-level SDRAM management such as refresh and activate/precharge
- The PHY block:
    - Interfaces with the MC block over a simple interface and translates the signals into the actual signals sent to the SDRAM, and vice versa
    - Translates and synchronizes control and data over various clock domains
    - Initializes the SDRAM
    - Performs write leveling for DDR3 (fly-by routing topology required for component designs)
    - Interfaces with the MC to perform periodic timing calibration required to account for changing environmental conditions
    - Performs calibration to center align capture clocks with read data

Figure 1 also shows a user design connecting to the memory interface. An example user design is provided with the core. See UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide* for more details regarding the design.

QDRII+ SRAM

This section discusses the features, applications, and functional description of Virtex-6 FPGA memory interface solutions in QDRII+ SRAM.

Features

- QDRII+ SRAM device support
- 120–400 MHz performance:
    - 300 MHz in a -1 commercial speed grade device
    - 350 MHz in a -2 commercial speed grade device
    - 400 MHz in a -3 commercial speed grade device
- Hardware validated
- x18 and x36 memory width support
- Configurable data bus widths
- 4-word burst support
- Source code delivery in Verilog or VHDL
- 2:1 memory to FPGA logic interface clock ratio
- 2.0 and 2.5 cycle read latency support
- Fixed latency mode support
- Multiple controllers per FPGA supported through the MIG tool

See the *Virtex-6 FPGA Memory Interface Solutions User Guide* for more details regarding the features listed here.

Applications

QDRII+ SRAMs are the latest generation of QDR SRAM devices that offer high-speed data transfers on separate read and write buses on the rising and falling edges of the clock. These memory devices are used in high-performance systems as temporary data storage, such as:

- Look-up tables in networking systems
- Packet buffers in network switches
- Cache memory in high-speed computing
- Data buffers in high-performance testers

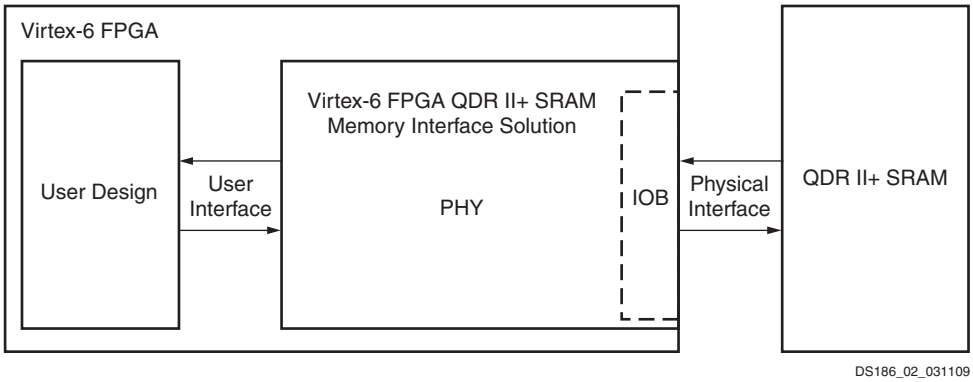

Figure 2: **QDRII+ SRAM Memory Interface Core**

Functional Description

As shown in Figure 2, the top-level functional block is composed of a PHY that interfaces to the user and to the QDRII+ SRAM device. The PHY block:

- Translates simple user read and write commands to conform to QDRII+ SRAM protocol
- Enables the user to provide up to one read and one write transaction per clock cycle for maximum throughput
- Performs calibration to center align clocks with data
- Returns data to the user with a corresponding valid signal
- Performs periodic timing calibration required to account for changing environmental conditions
- Translates and synchronizes over various clock domains
- Implements an optimized half-frequency design that eliminates the need for a memory controller

For more details regarding this functionality, see UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide* provided with the core.

RLDRAM II

This section discusses the features, applications, and functional description of Virtex-6 FPGA memory interface solutions in RLDRAM II devices.

Features

- RLDRAM II common I/O (CIO) memory device support
- 175–500 MHz performance for center column interfaces:
  - 350 MHz in a -1 commercial speed grade device
  - 400 MHz in a -2 commercial speed grade device
  - 500 MHz in a -3 commercial speed grade device
- Hardware validated
- x9, x18, and x36 memory width support
- Configurable data bus widths
- 4-word and 8-word burst support
- Configuration 1, 2, 3 support
- Address Multiplexing Mode support
- ODT support
- RLDRAM II initialization support
- Source code delivery in Verilog or VHDL
- 2:1 memory to FPGA logic interface clock ratio
- Fixed latency mode support
- Multiple controllers per FPGA supported by running the MIG tool multiple times.

See UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide* for more details regarding the features listed here.

Applications

Figure 3 shows a high-level block diagram of the Virtex-6 FPGA memory interface solution connecting a user design to an RLDRAM II device. The PHY side of the design is connected to the RLDRAM II device via FPGA IOBs, and the UI side is connected to the user design via FPGA logic. See the *Virtex-6 FPGA Memory Interface Solutions User Guide* for more details regarding the design.

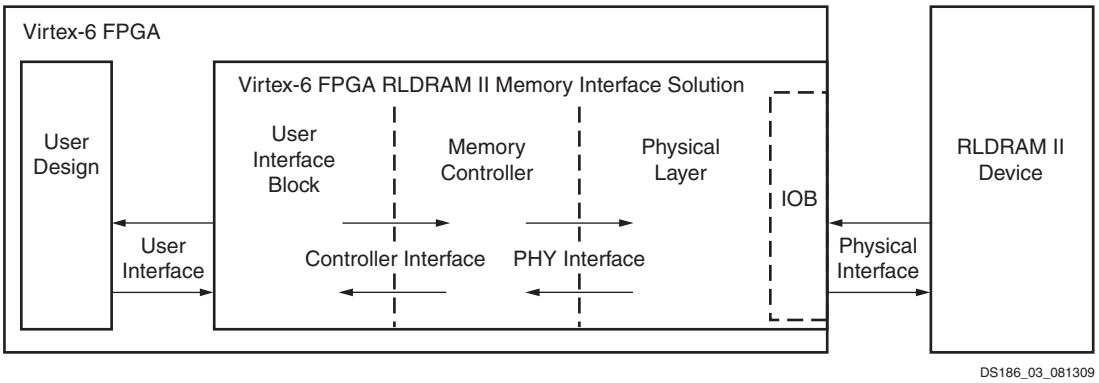

Figure 3: **RLDRAM II Memory Interface Core**

Functional Description

As shown in Figure 3, the top-level functional blocks of the RLDRAM II memory interface solution include:

- The UI block:
  - Presents the user interface to a user design
  - Buffers commands and write data
- The MC block:
  - Receives requests from the user design
  - Processes commands in order and adheres to memory specifications
  - Performs high-level SDRAM management such as refresh and controls bank access
- The PHY block:
  - Interfaces with the MC block over a simple interface and translates the signals into the actual signals sent to the SDRAM, and vice versa
  - Performs calibration to center align clocks with data
  - Returns data to the user with a corresponding valid signal
  - Performs periodic timing calibration required to account for changing environmental conditions
  - Translates and synchronizes over various clock domains

For more details regarding this functionality, see UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide* provided with the core.

General Specifications

See the *Virtex-6 FPGA Memory Interface Solutions User Guide* for more details regarding specific banking, pin location, and internal clock resource requirements.

Verification

The Virtex-6 FPGA memory interface solutions core has been verified in simulation. Verification tests include:

- Initialization sequence
- Read calibration
- Memory read operation
- Memory write operation
- Row/bank management

Additional Resources

The following material provides additional information related to this document:

1. JEDEC Standard JESD79-2F: DDR2 SDRAM Specification, JEDEC Solid State Technology Association
   http://www.jedec.org
2. JEDEC Standard JESD79-3E: DDR3 SDRAM, JEDEC Solid State Technology Association
   http://www.jedec.org

Xilinx MIG documentation can be located on the MIG Solution Center Documentation page:

- UG406, *Virtex-6 FPGA Memory Interface Solutions User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
09/16/09	1.1	• Added QDRII+ SRAM and RLDRAM II to LogiCORE™ IP Facts Table. • Updated DDR3 SDRAM Features, page 1, DDR2 SDRAM Features, page 2, and Features, page 4. • Added RLDRAM II, page 6.
12/02/09	1.2	• Updated speed grade and source code delivery information in Features sections of DDR3 and DDR2 SDRAMs, QDRII+ SRAM, and RLDRAM II. • Updated Core Specifics table.
04/19/10	1.3	• Updated LogiCORE™ IP Facts Table. • Updated DDR3 and DDR2 SDRAMs, QDRII+ SRAM, and RLDRAM II.
07/23/10	1.4	Updated DDR3 and DDR2 SDRAM resources, and ISE Design Suite and ModelSim versions in LogiCORE™ IP Facts Table. Removed x9 memory width support and added 2.0 and 2.5 cycle read latency support to Features, page 4.
09/21/10	1.5	MIG 3.6 release. Updated ISE Design Suite version in LogiCORE™ IP Facts Table. Added AXI4 Slave Interface Features, page 3. Added description of AXI4 to Applications, page 3. Removed CQ and CQ# from Features, page 4.
12/14/10	1.6	MIG 3.61 release. Removed parenthetical note about data pending characterization for single-rank interfaces from DDR3 SDRAM Features, DDR2 SDRAM Features, LogiCORE™ IP Facts Table, Features, page 4 and Features, page 6. Changed dual-rank performance from 250 Mb/s to 300 Mb/s in DDR2 SDRAM Features.
03/01/11	1.7	MIG 3.7 release with the ISE 13.1 software release. Added note 2 to LogiCORE™ IP Facts Table.
06/22/11	1.8	MIG 3.8 release with the ISE 13.2 software release.
10/19/11	1.9	MIG 3.9 release with the ISE 13.3 tool. • In AXI4 Slave Interface Features, added bulleted item about AXI4-Lite interface support and added 72 bits as one of the memory data widths. • In RLDRAM II Features, added address multiplexing mode support.
01/18/12	1.10	MIG 3.91 release with the ISE 13.4 tool release.

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