

Table 1: OPB SDRAM Controller Design Parameters

Grouping / Number	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type	
SDRAM Controller Features	G1	Include support for OPB bursts	C_INCLUDE_BURST_SUPPORT	0 = don't include logic to support OPB bursts 1 = include logic to support OPB bursts	1	integer
	G2	Use positive edge output registers for SDRAM interface signals	C_USE_POSEDGE_OUTPUTS	0 = don't use positive edge output registers (SDRAM interface signals clocked on negative edge) 1 = use positive edge output registers (SDRAM interface signals clocked on positive edge)	0	integer
	G3	Include pipeline stage to increase operating frequency (increases latency by 1 clock) ⁽¹⁾	C_INCLUDE_HIGHSPEED_PIPELINE	0 = don't include pipeline stage 1 = include pipeline stage	1	integer
	G4	Target FPGA family	C_FAMILY	spartan2 spartan2e spartan3 virtex virtex2 virtex2p virtex4	virtex2p	string
SDRAM Device Features	G5	Load Mode Register command cycle time (Tck)	C_SDRAM_TMRD		2	integer
	G6	Write Recovery Time (ps)	C_SDRAM_TWR		15000	integer
	G7	Read/Write command to Read/Write command (Tck)	C_SDRAM_TCCD		1	integer
	G8	Delay after ACTIVE command before PRECHARGE command (ps)	C_SDRAM_TRAS		40000	integer
	G9	Delay after ACTIVE command before another ACTIVE or AUTOREFRESH command (ps)	C_SDRAM_TRC		65000	integer

Table 1: OPB SDRAM Controller Design Parameters (Continued)

Grouping / Number	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type	
G10	Delay after AUTOREFRESH before another command(ps)	C_SDRAM_TRFC		75000	integer	
G11	Delay after ACTIVE command before READ/WRITE command(ps)	C_SDRAM_TRCD		20000	integer	
G12	Delay after ACTIVE command for a row before an ACTIVE command for another row (ps)	C_SDRAM_TRRD		15000	integer	
G13	Delay after a PRECHARGE command (ps)	C_SDRAM_TRP		20000	integer	
G14	Refresh command interval (ms)	C_SDRAM_TREF		64	integer	
G15	Number of Rows in a Refresh Period ⁽³⁾	C_SDRAM_REFRESH_NUMROWS	2048, 4096, 8192, 16384	8192	integer	
G16	CAS Latency	C_SDRAM_CAS_LAT	2,3	2	integer	
G17	Total data width of devices ⁽⁴⁾	C_SDRAM_DWIDTH	8, 16, 32	32	integer	
G18	SDRAM address width	C_SDRAM_AWIDTH	See note ⁽⁵⁾	13	integer	
G19	SDRAM column address width	C_SDRAM_COL_AWIDTH	See note ⁽⁵⁾	9	integer	
G20	SDRAM bank address width	C_SDRAM_BANK_AWIDTH	See note ⁽⁵⁾	2	integer	
Address Space	G21	Base Address	C_BASEADDR	Valid address ⁽⁶⁾	std_logic_vector	
	G22	High Address	C_HIGHADDR	Valid address ⁽⁶⁾	std_logic_vector	
OPB Bus Interface	G23	OPB Data bus width	C_OPB_DWIDTH	32	32	integer
	G24	OPB Address bus width	C_OPB_AWIDTH	32	32	integer
	G25	OPB clock period (ps)	C_OPB_CLK_PERIOD_PS			integer

Table 1: OPB SDRAM Controller Design Parameters (Continued)

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Auto-calculated parameters ⁽⁷⁾	G26	Average periodic refresh command interval (ps)	C_SDRAM_TREFI	C_SDRAM_TREF/C_SDRAM_REFRESH_NUMROWS	7800000	integer
	G27	SDRAM simulation initialization time in picoseconds	C_SIM_INIT_TIME_PS ⁽⁸⁾		1000000 0	integer

Notes:

1. Set this parameter to 0 if C_USE_POSEDGE_OUTREGS = 1.
2. Manual precharge timing numbers should be used for this parameter if the SDRAM data sheet has different timing numbers for manual and auto precharge.
3. This parameter is used to calculate the refresh command interval and therefore should be set to the number of rows in a refresh period, which is not always the same as the number of rows in the SDRAM device. Check the data sheet carefully for this parameter.
4. Data width of SDRAM devices must be ≥ 8 and:
 - a. = OPB data width OR
 - b. = OPB data width/2 OR
 - c. = OPB data width/4
5. $C_SDRAM_AWIDTH + C_SDRAM_COL_AWIDTH + C_SDRAM_BANK_AWIDTH + \log_2(C_SDRAM_DWIDTH/8)$ must be $< C_OPB_AWIDTH - 1$.
6. The range specified by C_BASEADDR and C_HIGHADDR must comprise a complete, contiguous power of two range such that $range = 2^n$, and the n least significant bits of C_BASEADDR must be zero. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR + 1.
7. These parameters are automatically calculated by the system generation tool and are not input by the user.
8. Simulation only parameter. This parameter is used to change the SDRAM time for simulation only. Note, the SDRAM requires ~300 nS after this initialization time to complete the initialization sequence. Also note that if this parameter is modified from the default of 100 uS, simulation results will vary from hardware implementation.

OPB SDRAM Controller I/O Signals

The pin diagram of the OPB SDRAM Controller is shown in **Figure 1**:

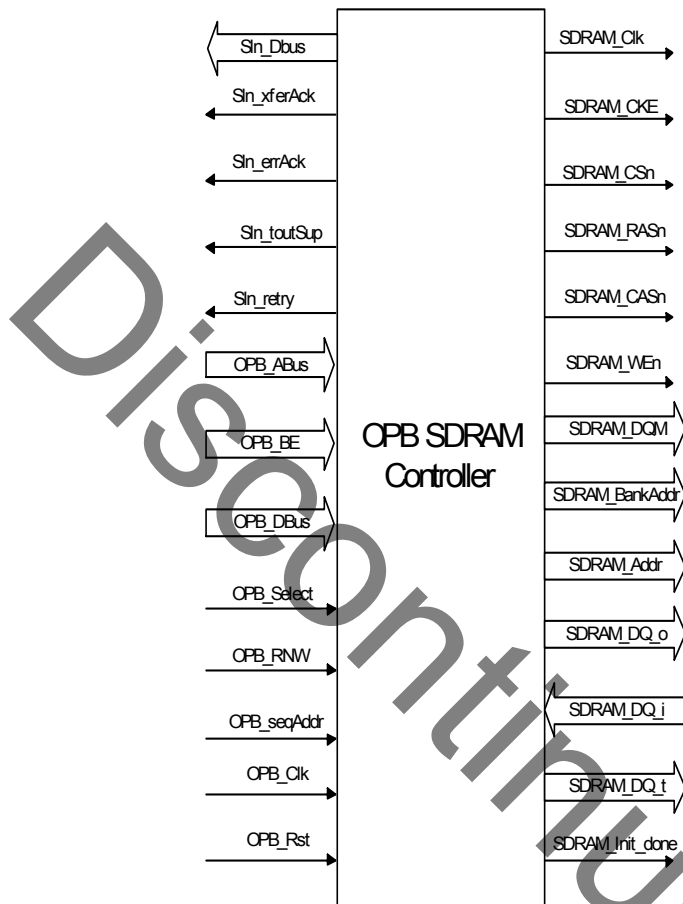


Figure 1: OPB SDRAM Controller Pin Diagram

Table 2 provides a summary of all OPB SDRAM Controller input/output (I/O) signals, the interfaces under which they are grouped, and a brief description of the signals.

Table 2: OPB SDRAM Controller Pin Descriptions

Grouping		Signal Name	Interface	I/O	Initial State	Description
SDRAM Signals	P1	SDRAM_Clk	SDRAM	O	0	SDRAM Clock
	P2	SDRAM_CKE	SDRAM	O	0	SDRAM Clock Enable
	P3	SDRAM_CSs	SDRAM	O	1	Active low SDRAM chip select
	P4	SDRAM_RASn	SDRAM	O	1	Active low SDRAM row address strobe
	P5	SDRAM_CASn	SDRAM	O	1	Active low SDRAM column address strobe

Table 2: OPB SDRAM Controller Pin Descriptions (Continued)

Grouping	Signal Name	Interface	I/O	Initial State	Description	
	P6	SDRAM_WEn	SDRAM	O	1	Active low SDRAM write enable
	P7	SDRAM_DQM [0:C_SDRAM_DWIDTH/8 - 1]	SDRAM	O	0	SDRAM data mask
	P8	SDRAM_BankAddr [0:C_SDRAM_BANK_AWIDTH-1]	SDRAM	O	0	SDRAM bank address
	P9	SDRAM_Addr [0:C_SDRAM_AWIDTH - 1]	SDRAM	O	0	SDRAM address
	P10	SDRAM_DQ_o [0:C_SDRAM_DWIDTH - 1]	SDRAM	O	0	Output data to SDRAM
	P11	SDRAM_DQ_i [0:C_SDRAM_DWIDTH - 1]	SDRAM	I		Input data from SDRAM
	P12	SDRAM_DQ_t [0:C_SDRAM_DWIDTH - 1]	SDRAM	O	0	3-state control for SDRAM data buffers
	P13	SDRAM_Clk_in	SDRAM	I		Connected to OPB_Clk.
	P14	SDRAM_Init_done	SDRAM	O	0	SDRAM power-up initialization done
OPB Slave Signals ⁽¹⁾	P15	OPB_Select	OPB	I		OPB select
	P16	OPB_RNW	OPB	I		OPB read, not write
	P17	OPB_ABus[0:C_OPB_AWIDTH-1]	OPB	I		OPB address bus
	P18	OPB_DBus[0:C_OPB_DWIDTH-1]	OPB	I		OPB data bus
	P19	OPB_BE[0:C_OPB_DWIDTH/8-1]	OPB	I		OPB byte enables
	P20	OPB_seqAddr	OPB	I		OPB sequential address
	P21	SIn_xferAck	OPB	O	0	SDRAM Controller transfer acknowledge
	P22	SIn_errAck	OPB	O	0	SDRAM Controller error acknowledge
	P23	SIn_toutSup	OPB	O	0	SDRAM Controller timeout suppress
	P24	SIn_retry	OPB	O	0	SDRAM Controller retry
	P25	SIn_DBus[0:C_OPB_DWIDTH-1]	OPB	O	0	SDRAM Controller OPB data bus
	P26	OPB_Clk	OPB	I		OPB clock
	P27	OPB_Rst	OPB	I		OPB reset

Notes:

1. Please refer to the IBM OPB Bus Architecture Specification for more detailed information on these signals.

Parameter- Port Dependencies

The dependencies between the OPB SDRAM Controller design parameters and I/O signals are shown in [Table 3](#). It gives information about how the ports and parameters get affected by changing certain parameters.

Table 3: Parameter-Port Dependencies

Grouping	Name	Affects	Depends	Description
Design Parameters	G24	C_OPB_AWIDTH	P16	Width of the OPB Address Bus vary based on the OPBaddress width
	G23	C_OPB_DWIDTH	P17,P18,P24	Width of the OPB Data Bus, byte enables and slave data busses vary based on the OPBdata width
		C_SDRAM_DWIDTH	P7,P10,P11,P12	Width of the memory data interface varies based on the data width of the SDRAM memory
		C_SDRAM_AWIDTH	P9	Width of the memory address interface varies based on the address width of the SDRAM memory
		C_SDRAM_BANK_ADDRESS_WIDTH	P8	Width of the memory bank address interface varies based on the bank address width of the SDRAM memory
I/O Signals	P16	OPB_ABus	C_OPB_AWIDTH	Width varies with the width of the OPB Address Bus
	P17	OPB_DBus	C_OPBDWIDTH	Width varies with the width of the OPB Data Bus
	P18	OPB_BE	C_OPBDWIDTH	Width varies with the width of the OPB Data Bus
	P24	SlIn_DBus	C_OPB_DWIDTH	Width varies with the width of the OPB Data Bus
	P11	SDRAM_DQ_i	G17	Width varies with the data width of the SDRAM memory
	P10	SDRAM_DQ_o	G17	Width varies with the data width of the SDRAM memory
	P12	SDRAM_DQ_t	G17	Width varies with the data width of the SDRAM memory
	P7	SDRAM_DQM	G17	Width varies with the data width of the SDRAM memory
	P8	SDRAM_BankAddr	G20	Width varies with the width of the SDRAM Bank Address Bus
	P9	SDRAM_Addr	G18	Width varies with the width of the SDRAM Address Bus

Connecting to Memory

Memory Data Types and Organization

SDRAM memory can be accessed as: byte (8 bits), halfword (2 bytes), or word (4 bytes), depending on the size of the bus to which the processor is attached. From the point of view of the OPB, data is organized as big-endian. The bit and byte labeling for the big-endian data types is shown below in [Figure 2](#).

Byte address	n	n + 1	n + 2	n + 3	Word	
Byte label	0	1	2	3		
Byte significance	MSByte			LSByte		
Bit label	0					31
Bit significance	MSBit					LSByte

Byte address	n	n + 1	Halfword	
Byte label	0	1		
Byte significance	MSByte	LSByte		
Bit label	0			15
Bit significance	MSBit	LSBit		

Byte address	n	Byte	
Byte label	0		
Byte significance	MSByte		
Bit label	0		7
Bit significance	MSBit		LSBit

Figure 2: Big-Endian Data Types

Memory to OPB SDRAM Controller Connections

The data and address signals at the memory controller are labeled with big-endian bit labeling (for example, D(0:31), D(0) is the MSB), whereas most memory devices are either endian agnostic (they can be connected either way) or little-endian D(31:0) with D(31) as the MSB.

Caution must be exercised with the connections to the external memory devices to avoid incorrect data and address connections. [Table 4](#) shows the correct mapping of memory controller pins to memory device pins.

Table 4: Example Signal to Device Pin Mapping (32M X 8)

SDRAM Signal (Big-Endian)	Memory Device Signal (Little-Endian)
SDRAM_Addr(0)	A12
SDRAM_Addr(1)	A11
SDRAM_Addr(2)	A10
SDRAM_Addr(3)	A9
SDRAM_Addr(4)	A8
SDRAM_Addr(5)	A7
SDRAM_Addr(6)	A6
SDRAM_Addr(7)	A5
SDRAM_Addr(8)	A4
SDRAM_Addr(9)	A3
SDRAM_Addr(10)	A2
SDRAM_Addr(11)	A1
SDRAM_Addr(12)	A0
SDRAM_BankAddr(0)	BA1
SDRAM_BankAddr(1)	BA0
SDRAM_DQ(0)	D7
SDRAM_DQ(1)	D6
SDRAM_DQ(2)	D5
SDRAM_DQ(3)	D4
SDRAM_DQ(4)	D3
SDRAM_DQ(5)	D2
SDRAM_DQ(6)	D1
SDRAM_DQ(7)	D0
SDRAM_DQM(0)	DQMU
SDRAM_DQM(1)	DQML

SDRAM Address Mapping

An address offset is calculated based on the width of the SDRAM data bus and the OPB data bus. The SDRAM column address is then mapped to the OPB address bus, followed by the row address and bank address.

Since the SDRAM will always be accessed to provide data the width of the OPB bus, the column address starting bit is based on the SDRAM data width offset and the column address ending bit is based on the OPB data width offset. The difference in these offsets are set to zero. This sends the proper column address to the SDRAM.

The OPB address bus bit locations for the SDRAM column, row, and bank addresses are calculated as shown in [Table 5](#) and [Table 6](#).

Table 5: SDRAM Address offset calculations

Variable	Equation
SDRAM_ADDR_OFFSET	$\log_2(C_SDRAM_DWIDTH/8)$
OPB_ADDR_OFFSET	$\log_2(C_OPB_DWIDTH/8)$
COLADDR_STARTBIT	$C_OPB_AWIDTH - (C_SDRAM_COL_AWIDTH + SDRAM_ADDR_OFFSET)$
COLADDR_ENDBIT	$C_OPB_AWIDTH - OPB_ADDR_OFFSET - 1$
NUM_ZEROADDR_BITS	$OPB_ADDR_OFFSET - SDRAM_ADDR_OFFSET$
ROWADDR_STARTBIT	$COLADDR_STARTBIT - C_SDRAM_AWIDTH$
ROWADDR_ENDBIT	$ROWADDR_STARTBIT + C_SDRAM_AWIDTH - 1$
BANKADDR_STARTBIT	$ROWADDR_STARTBIT - C_SDRAM_BANK_AWIDTH$
BANKADDR_ENDBIT	$BANKADDR_STARTBIT + C_SDRAM_BANK_AWIDTH - 1$

Table 6: SDRAM - OPB Address Bus Assignments

SDRAM Address	OPB Address Bus
Column Address	OPB_ABus(COLADDR_STARTBIT to COLADDR_ENDBIT) & NUM_ZEROADDR_BITS
Row Address	OPB_ABus(ROWADDR_STARTBIT to ROWADDR_ENDBIT)
Bank Address	OPB_ABus(BANKADDR_STARTBIT to BANKADDR_ENDBIT)

Table 7 and Table 8 show an example of the mapping between the OPB address and the SDRAM address when the data width of the SDRAM is 16 and the data width of the bus is 32, the column address width is 9, the row address width is 13, and the bank address width is 2. Note that since the OPB data width is 32, its address offset is 2 where the SDRAM address offset is 1. Therefore, the column address is OPB address bus bit 22 through bit 29 with a concatenated zero.

Table 7: OPB Example SDRAM Address offset calculations

Variable	Value
SDRAM_ADDR_OFFSET	$\log_2(16/8) = 1$
OPB_ADDR_OFFSET	$\log_2(32/8) = 2$
COLADDR_STARTBIT	$32 - (9+1) = 22$
COLADDR_ENDBIT	$32 - 2 - 1 = 29$
NUM_ZEROADDR_BITS	$2 - 1 = 1$
ROWADDR_STARTBIT	$22 - 13 = 9$
ROWADDR_ENDBIT	$9 + 13 - 1 = 21$
BANKADDR_STARTBIT	$9 - 2 = 7$
BANKADDR_ENDBIT	$7 + 2 - 1 = 8$

Table 8: SDRAM - OPB Address Bus Assignments

SDRAM Address	OPB Address Bus
Column Address	OPB_ABus(22: 29) & '0'
Row Address	OPB_ABus(9:21)
Bank Address	OPB_ABus(7:8)

SDRAM Controller Design

Block Diagram

The OPB SDRAM Controller consists of the OPB IPIF to provide the bus protocol, three state machines to control the SDRAM operation, an I/O module to instantiate the SDRAM I/O registers for the SDRAM data interface, and a clock generation module. The OPB SDRAM Controller block diagram is shown in Figure 3.

The separation of the Command State Machine and the Data State Machine allows for the application of commands to the SDRAM while data reception/transmission is in progress. Overlapping the SDRAM commands with the data transfer when accessing data in the same row of the same bank allows for more optimal SDRAM operation.

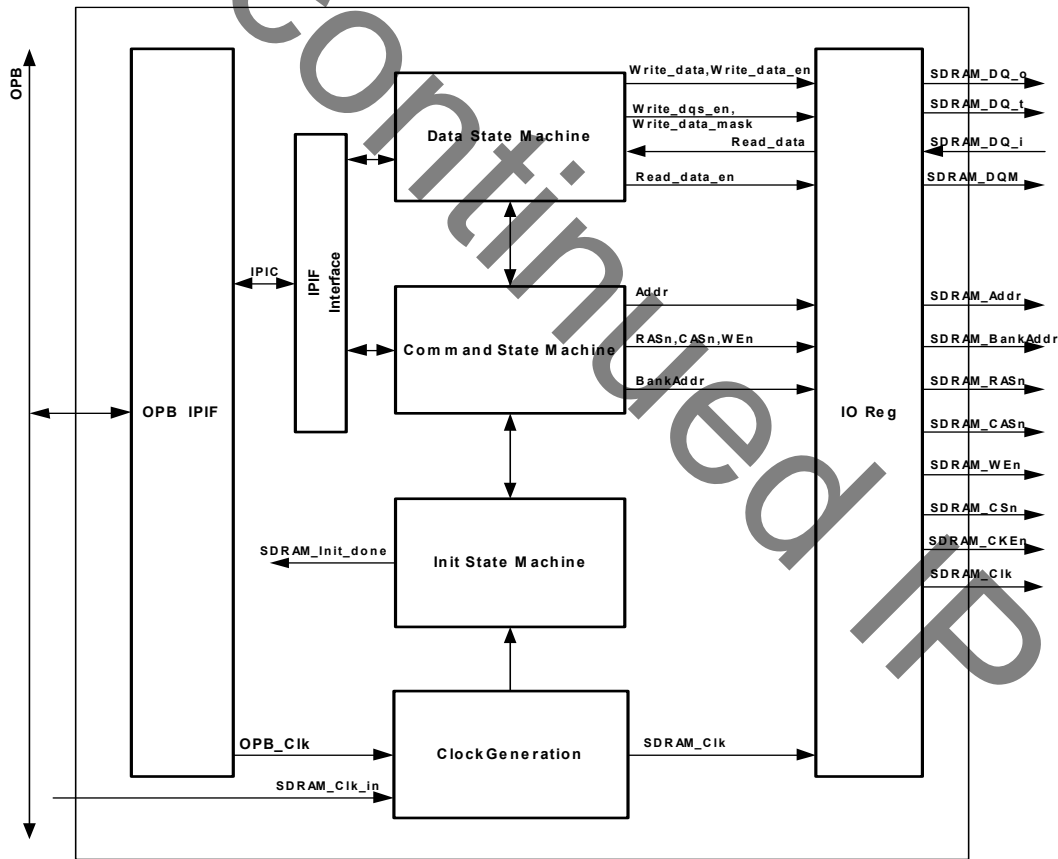


Figure 3: OPB SDRAM Controller Block Diagram

Init State Machine

SDRAMs must be powered up and initialized in a predefined manner specified in the SDRAM device data sheet. Once power has been applied and the clock is stable, the SDRAM requires a 100uS delay prior to issuing any command other than a COMMAND INHIBIT or a NOP. Figure 4 shows the state diagram of the Init State Machine.

The Init State Machine provides the 100uS delay and the sequencing of the required SDRAM start-up commands. It instructs the Command State Machine to send the proper commands in the proper sequence to the SDRAM. This state machine starts execution after Reset and returns to the IDLE state when Reset is applied.

For a typical SDRAM ~300 nS is required after the 100 uS reset / power-up time to complete the initialization sequence. During the initialization sequence, the OPB SDRAM Controller will respond to accesses by asserting OPB_Retry. When the initialization sequence has been completed, the INIT_DONE signal asserts. Note that after Reset has been applied, the 100 uS delay is again implemented before any commands are issued to the SDRAM. For simulation purposes, the 100 uS reset / power-up delay can be modified by the parameter C_SIM_INIT_TIME_PS. Approximately 300 nS after delay specified by C_SIM_INIT_TIME_PS, the initialization sequence is complete.

Note: If C_SIM_INIT_TIME_PS is modified from 100000000 (100 uS), the simulation behavior will vary from the hardware implementation results during initialization. The simulation will no longer be reflecting the hardware behavior during this time.

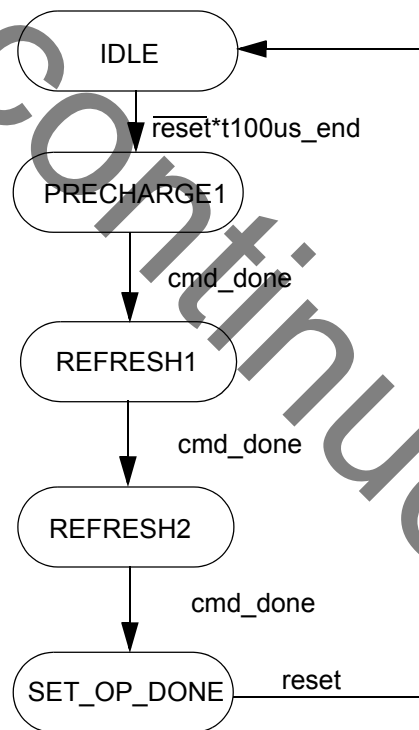


Figure 4: OPB SDRAM Init State Machine

Command State Machine

The Command State Machine provides the address bus and commands signals to the SDRAM. It sends the Pend_write and Pend_Read signals to the Data State Machine to start the reception/transmission of data.

If a burst transaction is in progress or a secondary transaction has been received, the Command State Machine will send the next command to the SDRAM while data reception/transmission is still in progress to optimize the SDRAM operation.

A simplified version of the Command State Machine is shown in Figure 5. For readability, only the major state transitions are shown

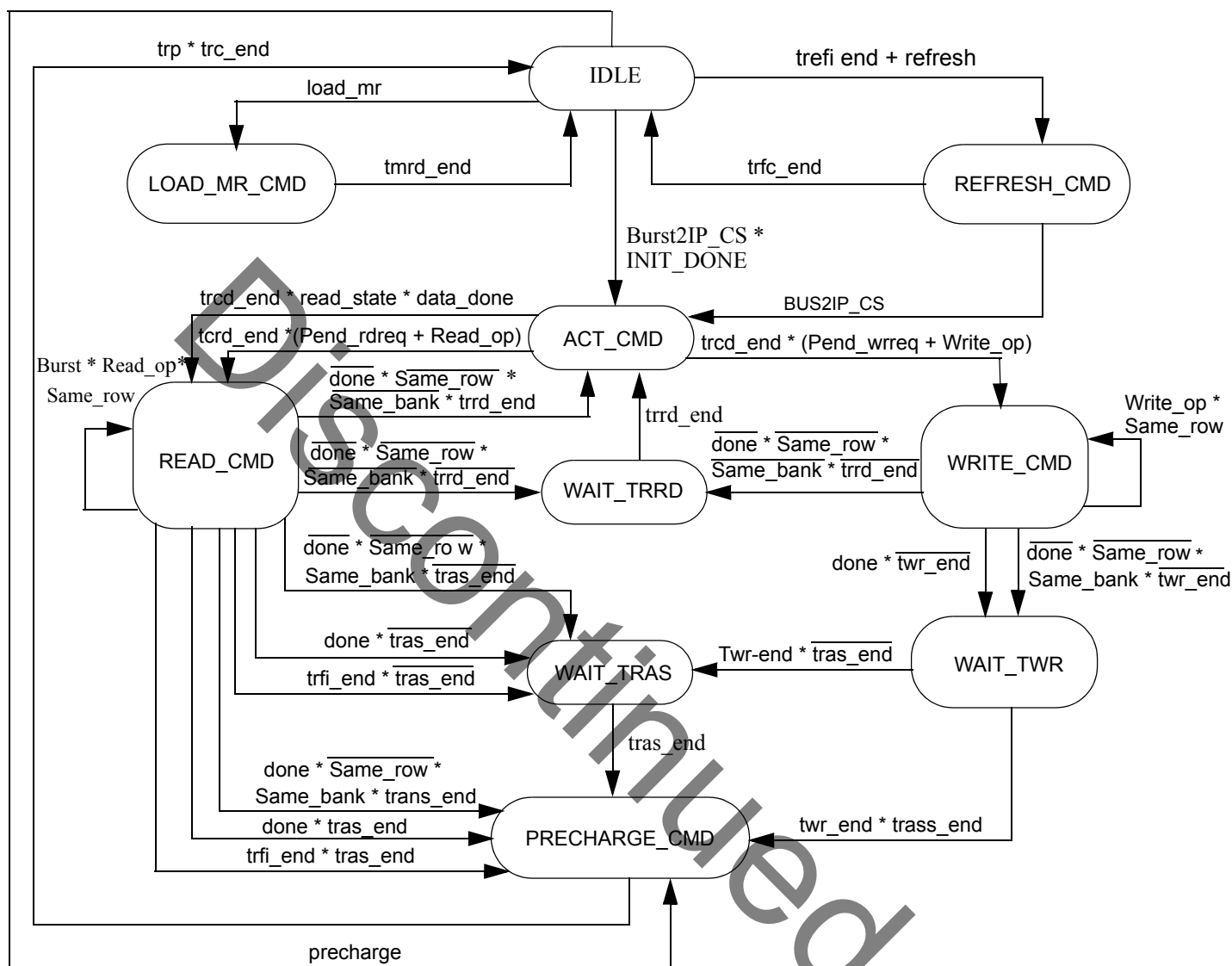


Figure 5: OPB SDRAM Command State Machine

Data State Machine

The Data State Machine transfers the data to/from the SDRAM and determines when the specified SDRAM burst is complete. It monitors the PENDING_READ and PENDING_WRITE signals from the Command State Machine and BUS2IP_Burst from the IPIF to know if more data transmissions are required. It waits for CAS_LATENCY during read operations and signals when the SDRAM has completed the data transfer for both read and write operations. The Data State Machine is shown in Figure 6.

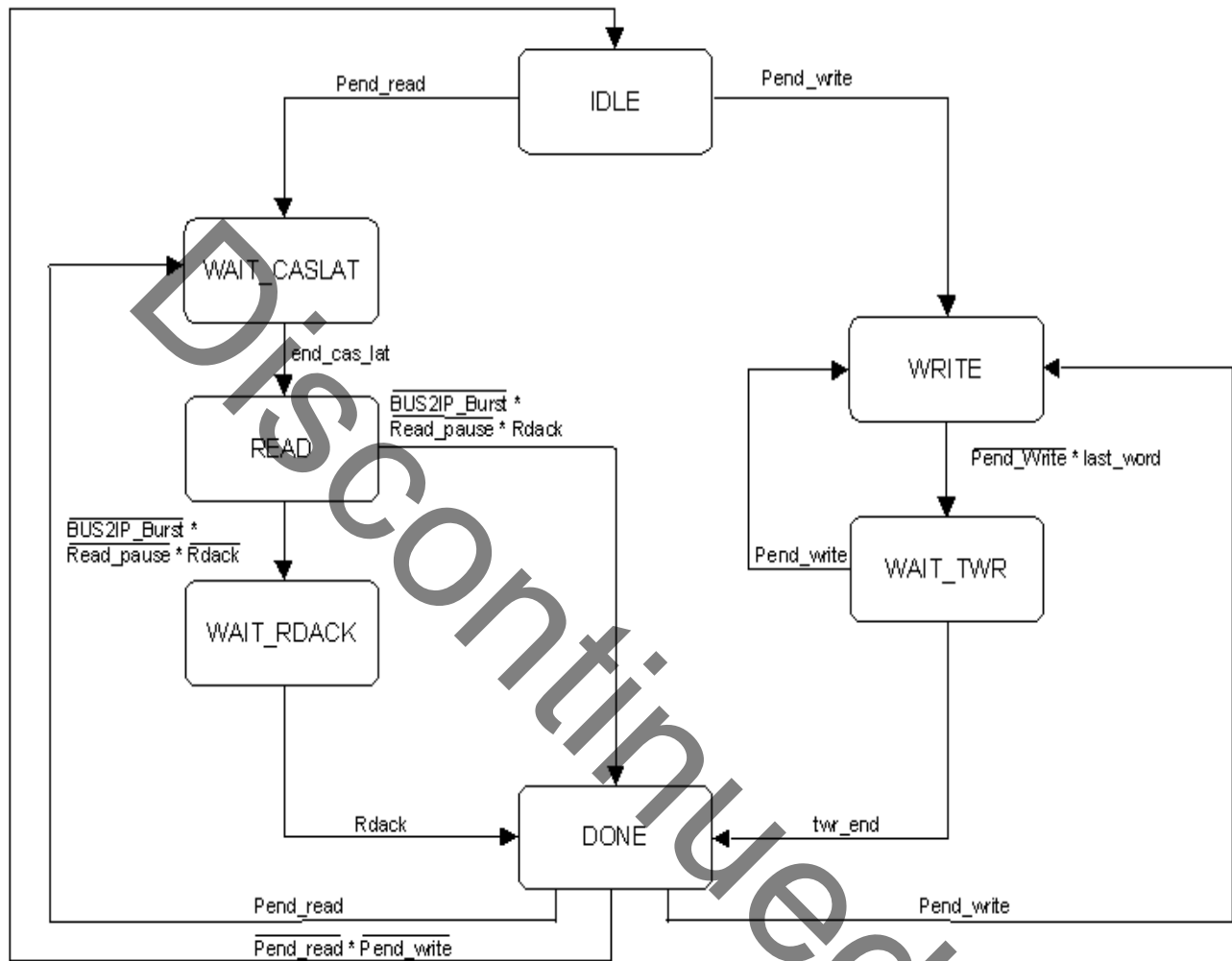


Figure 6: OPB SDRAM Data State Machine

Clock Generation

The Clock Generation module simply passes the SDRAM_Clk_in clock to the SDRAM_Clk output clock as shown in Figure 7. It also passes the OPB_Clk through to the Sys_Clk output to clock the rest of the SDRAM controller logic.

