

## Introduction

The LogiCORE™ IP UCF Generator for PCI/PCI-X automates the process of creating device and package-specific user constraints files (UCFs) for Initiator/Target cores for PCI targeted to Virtex®-5, Virtex-4, Spartan®-3A/3 AN/3A DSP, and Spartan-3E architectures, and PCI-X targeted to Virtex-5 and Virtex-4 architectures.

## Features

- Creates pinouts for any Initiator/Target v3 for PCI in various Virtex-4, Spartan-3A/3AN/3A DSP and Spartan-3E package/device combinations
- Creates pinouts for any Initiator/Target v4 for PCI in various Virtex-5 package/device combinations
- Creates pinouts for any Initiator/Target v5 for PCI-X in various Virtex-4 package/device combinations
- Creates pinouts for any Initiator/Target v6 for PCI-X in various Virtex-5 package/device combinations
- Available through the Xilinx CORE Generator™ software
- Intuitive GUI-based user interface

## Software Requirements

- Xilinx ISE® v11.1

## Support for Older Architectures

UCF files for Spartan-3 devices are generated with the PCI UCF generation tool that is accessible from:

[www.xilinx.com/cgi-bin/UCFgen/UCF4PCI.cgi](http://www.xilinx.com/cgi-bin/UCFgen/UCF4PCI.cgi)

## Overview

The UCF Generator tool provides a graphical user interface (GUI) for entering UCF parameters and generating user constraints files.

## To Access the UCF Tool

1. Install the latest IP update:  
[www.xilinx.com/ipcenter/coregen/updates.htm](http://www.xilinx.com/ipcenter/coregen/updates.htm)
2. Browse to an existing CORE Generator project, or create a new project, targeting an appropriate device.
3. Click the **View by Function** tab in the CORE Generator screen.
4. Choose **Standard Bus Interfaces > PCI** to display a list of PCI-related cores.
5. Double-click the **LogiCORE UCF Generator for PCI/PCI-X**.
6. Follow the series of on-screen prompts to create a UCF file.

### Important: Testing Requirements and Limitations

It is important to verify the UCF files generated by this tool to confirm that the timing requirements of your application are met. Xilinx cannot guarantee that every UCF file generated by the UCF Generator tool will work for every application.

The UCF files created using the UCF Generator tool are designed for PCI and PCI-X cores targeted to Virtex-5, Virtex-4, Spartan-3A/3AN/3A DSP and Spartan-3E architectures using ISE v11.1. As more characterization data is collected, the speed files for various devices may be changed to model device operation more closely. In this event, Xilinx reserves the right to limit the applicability of this tool to certain part and package combinations or to modify or limit the pin assignments that this tool may generate.

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## Revision History

Date	Version	Revision
1/15/07	1.1	Initial Xilinx release.
4/25/08	2.7	Added support for Virtex-5 FXT devices.
9/19/08	2.8	Updated for ISE v10.1 Service Pack 3.
4/24/09	2.85	Updated for ISE v11.1.