multiple packet operation.

- CSMA/CD compliant operation at 10 Mbps and 100 Mbps in half duplex mode
- Programmable PHY reset signal
- Internal loop-back capability
- Supports unicast, multicast, and broadcast transmit and receive modes as well as promiscuous address receive mode
- Supports a "Freeze" (graceful halt) mode based on input signal assertion to assist with emulator based software development
- Provides auto or manual source address field insertion or overwrite for transmission
- Provides auto or manual pad and Frame Check Sequence (FCS) field insertion
- Provides auto pad and FCS field stripping on receive
- Processes received pause packets
- Supports reception of longer VLAN type frames
- Supports MII management control writes and reads with MII PHYs
- Programmable interframe gap
- Provides counters and interrupts for many error conditions

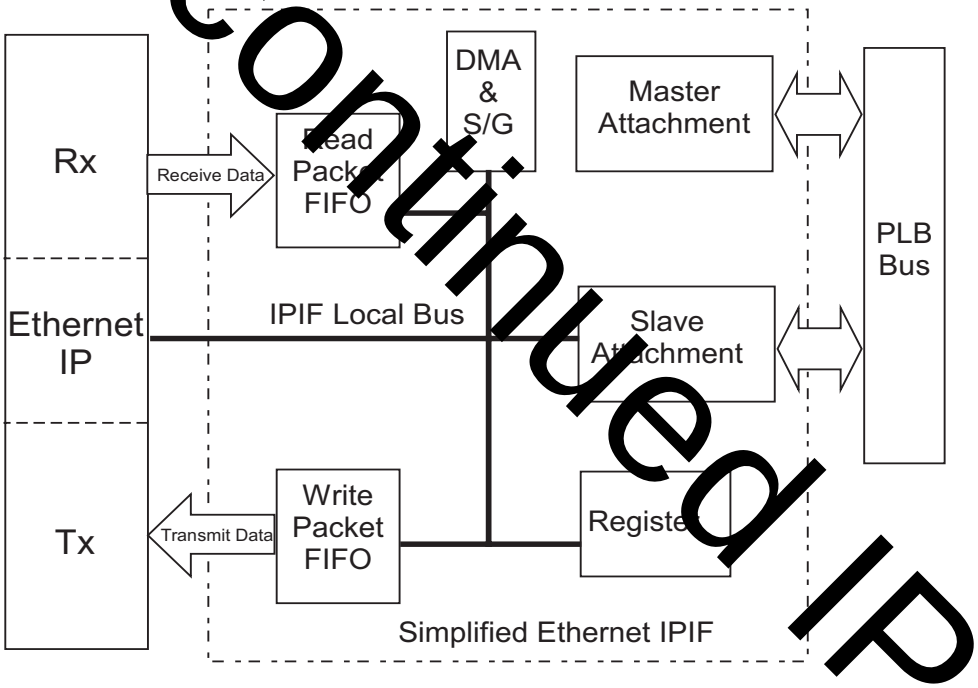

Figure 1: **IPIF and PLB EMAC Modules**

PLB Ethernet Protocol

PLB Ethernet data is encapsulated in frames as shown in Figure 2 for standard Ethernet and Figure 3 for VLANEthernet[1]. The fields in the frame are transmitted from left to right. The bits within the frame are transmitted from left to right (from least significant bit to most significant bit unless specified otherwise).

1. The PLB EMAC design does not support the Ethernet 8-byte preamble frame type