

## Introduction

The Turbo Convolution Code (TCC) decoder core is used in conjunction with a TCC encoder to provide an extremely effective way of transmitting data reliably over noisy data channels. The TCC decoder is designed to meet the *3GPP Mobile Communication System* specification [Ref 1].

## Features

- Drop-in module for Spartan<sup>™</sup>-3, Spartan-3A DSP, Virtex<sup>™</sup>-4, and Virtex-5 FPGAs
- Implements the 3GPP Long Term Evolution (LTE) specification [Ref 1]
- Core contains the full interleaver
- Full 3GPP LTE block size range supported, that is, 188 different block sizes in the range 40 - 6144
- Dynamically selectable number of Iterations 1-15
- Number representation is two's complement fractional numbers:
  - ◆ Data input: 5 integer bits and 3 fractional bits
  - ◆ Internal Calculations: 9 integer bits and 3 fractional bits
- Support for multiple processing (2, 4, 8) units to provide increased throughput
- Support for the MAX, MAX\_SCALE, and MAX\* algorithms.
- Configurable input memory depth
- Selection between DSP or fabric resources
- Support for rate 1/3 coded input
- C model available for fast simulation of BER performance
- Available through the Xilinx<sup>®</sup> CORE Generator<sup>™</sup> 10.1.1i and later software

## General Description

The TCC decoder is used in conjunction with a TCC encoder to provide an extremely effective way of transmitting data reliably over noisy data channels. The turbo decoder operates very well under low signal-to-noise conditions and provides a performance close to the theoretical optimal performance defined by the Shannon limit.

When a decoding operation is started, the core accepts the block size and the number of iterations from two input ports. A data load stage follows, in which the systematic and parity data is read into the core in parallel on a clock-by-clock basis and stored in internal block RAM. The core then starts the decoding process and implements the required number of iterations. Finally, the decoded bit sequence is output. All interleaving operations required in the 3GPP specification are handled automatically within the core.

The core expects two's complement fractional numbers as inputs and also uses this format for the internal calculations. Each fractional input number represents the Log Likelihood Ratio (LLR) divided by 2 for each input bit. This LLR value can be considered to be the confidence level that a particular bit is a one or zero.

## Performance

The performance of core varies with FPGA family and device, but has typical performances of:

- 200 Megabits per second (Mbps), 8 PU
- 100 Mbps, 4 PU
- 50 Mbps, 2 PU

## References

1. 3G TS.36.212 V1.0.0 (2007-03), *Multiplexing and Channel Coding (Release 8)*, Technical Specification Group Radio Access Network, 3rd Generation Partnership Project.

## Ordering Information

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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/25/08	1.0	Initial Xilinx release.

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