

## Introduction

The Utility Flip-Flop is a pipelining glue-logic core intended for use in a Xilinx Platform Studio (XPS) project.

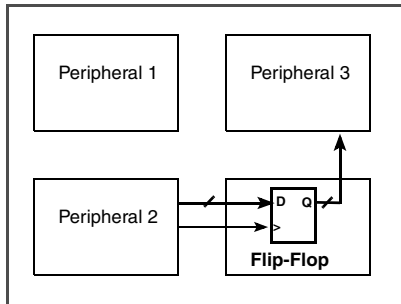


Figure 1: Utility Flip-Flop in a System

## Features

The flip-flop logic has the following features:

- Configurable size of the input and output bus
- Supports synchronous set and clear, or asynchronous reset and preset
- Supports optional clock enable
- Programmable init value of the register

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	See <a href="#">EDK Supported Device Families</a> .	
Version of Core	util_flipflop	v1.10a
Resources Used		
	Min	Max
LUTs	0	0
FFs	1	Variable <sup>(1)</sup>
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Design Tool Requirements		
Xilinx Implementation Tools	See <a href="#">Tools</a> for requirements.	
Simulation		
Synthesis		
Support		
Provided by <a href="#">Xilinx, Inc.</a>		

1. The number of flip-flops equals the parameter C\_SIZE.

## Utility Flip-Flop Parameters

Table 1: Utility Flip-Flop Parameters

Parameter	Description	Type
C_USE_RST	When C_USE_RST=1, the input signal "Rst" is connected as the "reset" or "clear" signal of the flip-flop depending on the value of C_USE_ASYNC. When C_USE_RST=0, the input signal "Rst" is not used.	Integer
C_SET_RST_HIGH	When C_SET_RST_HIGH = 1, the inputs Rst and Set is active high. When C_SET_RST_HIGH = 0, the inputs Rst and Set are active low.	Integer
C_USE_SET	When C_USE_SET=1, the input signal "Set" is connected as the "preset" or "set" signal of the flip-flop, depending on the value of C_USE_ASYNC. When C_USE_SET=0, the input signal "Set" is not used.	Integer
C_USE_CE	When C_USE_CE = 1, the input signal "CE" is connected as the "CE" (clock enable) of the flip-flop. When C_USE_CE = 0, the input signal CE is not used.	Integer
C_USE_ASYNC	When C_USE_ASYNC = 1, the FDCPE (D Flip-Flop with Clock Enable and Asynchronous Preset and Clear) is inferred. When C_USE_ASYNC = 0, the FDRSE (D Flip-Flop with Clock Enable and Synchronous Reset and Set) is inferred.	Integer
C_SIZE	The size of the vectors. Notice that the width of D and Q must be equal. The minimum value of this parameter is 1.	Integer
C_INIT	Initial startup value of flipflop, i.e. before set, reset or load operation	String

### Allowable Parameter Combinations

C\_INIT is a string of binary values defining the initial state of the utility flip-flop. The leftmost bit in the string is assigned to the flip-flop driving D[0], the following bit to the flip-flop driving D[1], and so on. When C\_INIT is set to the value "0" or "1", all flip-flops will have the initial value "0" or "1", respectively. Should the number of values in C\_INIT be greater than C\_SIZE, the rightmost bits in C\_INIT are ignored. C\_INIT greater than one but less than C\_SIZE is illegal and will give an error.

### Utility Flip-Flop I/O Signals

Table 2: Utility Flip-Flop I/O Signals

Signal	Interface	I/O	Description
Clk	None	I	Clock signal
Rst	None	I	When asynchronous style is selected (C_USE_ASYNC =1), this signal is connected as the "reset" signal. When synchronous style is selected (C_USE_ASYNC=0), this signal is connected as the "clear" signal. Rst is active high when active high reset is selected (C_SET_RST_HIGH=1), Rst is active low when active low reset is selected (C_SET_RST_HIGH=0) This signal has no effect when C_USE_RST = 0.

**Table 2: Utility Flip-Flop I/O Signals (Cont'd)**

Signal	Interface	I/O	Description
Set	None	I	When asynchronous style is selected (C_USE_ASYNCH=1), this signal is connected as the "preset" signal. When synchronous style is selected (C_USE_ASYNCH=0), this signal is connected as the "set" signal. Set is active high when active high set is selected (C_SET_RST_HIGH=1), Set is active low when active low set is selected (C_SET_RST_HIGH=0) This signal has no effect when C_USE_SET = 0.
CE	None	I	Clock enable. This signal has no effect when C_USE_CE = 0.
D	None	I	Input data bus to the flip-flop. Bus width is defined by the parameter C_SIZE.
Q	None	O	Output data bus from the flip-flop. Bus width is defined by the parameter C_SIZE.

## Parameter-Port Dependencies

**Table 3: Port and Parameter Dependencies**

Name	Affects	Depends	Relationship Description
<b>Design Parameters</b>			
C_SIZE	D	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Q	0 to C_SIZE-1	Scale width of output bus
<b>Port Signals</b>			
D		C_SIZE	Scale width of input bus
Q		C_SIZE	Scale width of output bus

## Utility Flip-Flop Register Descriptions

The core implements a pipeline register between the input bus 'D' and the output bus 'Q'.

## Utility Flip-Flop Interrupt Descriptions

There are no interrupts associated with this core.

## Utility Flip-Flop Block Diagram

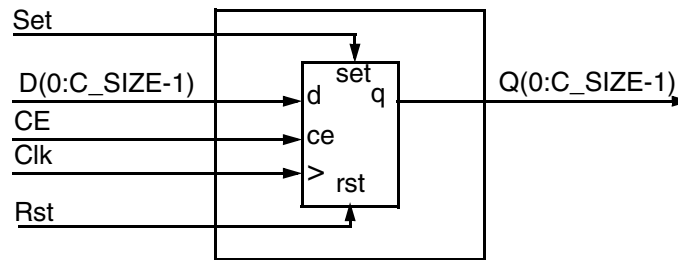


Figure 2: Utility Flip-Flop Diagram

## Design Implementation

### Design Tools

The Utility Flip-Flop design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Utility Flip-Flop.

### Target Technology

See [EDK Supported Device Families](#) for FPGA families.

## Device Utilization and Performance Benchmarks

This core instantiates C\_SIZE number of flop-flops.

There are no performance benchmarks available.

## Specification Exceptions

Not applicable.

## Reference Documents

None.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Revision History

The following table shows the revision history for this document.

<b>Date</b>	<b>Version</b>	<b>Revision</b>
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.
8/17/04	1.3	Updated for EDK 6.3. Updated trademarks and supported family device listing.
9/22/04	1.4	Updated according to new data sheet template
12/2/05	1.5	Added Spartan-3E to supported device families listing.
9/15/06	1.6	Parameter C_INIT added to define initial value of util flipflop Parameter C_SET_RST_HIGH to define active high or low set/reset signals
4/24/09	1.7	Removed support for Virtex, Virtex-II, Virtex-II Pro, Spartan-II and Spartan-II E devices. Replaced references to supported device families and tool names with hyperlink to PDF file.

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