

Introduction

The LogiCORE™ IP Virtex®-6 FPGA Embedded Tri-Mode Ethernet MAC Wrapper automates the generation of HDL wrapper files for the Embedded Tri-Mode Ethernet MAC (Ethernet MAC) in Virtex-6 LXT, SXT, HXT, and CXT FPGAs using the Xilinx® CORE Generator™ software.

VHDL and Verilog instantiation templates are available in the Libraries Guide for the Virtex-6 FPGA Ethernet MAC primitive; however, due to the complexity and large number of ports, the CORE Generator software simplifies integration of the Ethernet MAC by providing HDL examples based on user-selectable configurations.

Features

- Sets the Ethernet MAC attributes based on user options
- Provides user-configurable Ethernet MAC physical interfaces
 - Supports RGMII v1.3, RGMII v2.0, SGMII, and 1000BASE-X PCS/PMA interfaces, as well as GMII/MII at 2.5V only
 - Instantiates clock buffers, MMCMs, GTX serial transceivers, and logic as required for the selected physical interfaces
- Provides a simple FIFO-loopback example design, connected to the MAC client interface
- Provides a simple demonstration test bench based on the selected configuration
- Generates VHDL or Verilog
- Performance -- 10 Mb/s, 100 Mb/s, 1 Gb/s, and 2 or 2.5 Gb/s when overclocked. Performance is subject to device support; see [Performance, page 8](#).

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family ⁽¹⁾	Virtex-6 LXT, SXT, HXT, and CXT				
Supported User Interfaces	LocalLink (when using provided example FIFO), Client I/F				
Performance	10 Mb/s, 100 Mb/s, 1 Gb/s ⁽²⁾ , 2 Gb/s ⁽²⁾ , 2.5 Gb/s ⁽²⁾				
Resources ⁽³⁾					
Configuration	LUTs	FFs	RAMB36s	MMCMs	BUFGs
	280-430	400-620	2-2.5	0-1	1-4
Provided with Wrapper					
Documentation	Product Specification Getting Started Guide User Guide ⁽⁴⁾				
Design Files	Verilog or VHDL				
Example Design	Example FIFO connected to Client I/F				
Test Bench	Demonstration Test Bench, Scripts				
Constraints File	User Constraints File (.ucf)				
Simulation Model	Verilog SecureIP model ⁽⁵⁾				
Tested Design Tools					
Design Entry Tools	ISE 13.1 software				
Simulation	Mentor Graphics ModelSim 6.6d ⁽⁵⁾ Cadence Incisive Enterprise Simulator (IES) v10.2 ⁽⁵⁾ Synopsys VCS and VCS MX 2010.06 ^{(5),(6)}				
Synthesis Tools	XST 13.1				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the [release notes](#) for this core.
2. Performance is subject to device support; see [Performance, page 8](#).
3. The precise number depends on user configuration; see [Device Utilization, page 7](#).
4. Available from www.xilinx.com/support/documentation/user_guides/ug368.pdf
5. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.
6. Scripts are not provided for Synopsys VCS when VHDL is selected.

Ethernet Architecture Overview

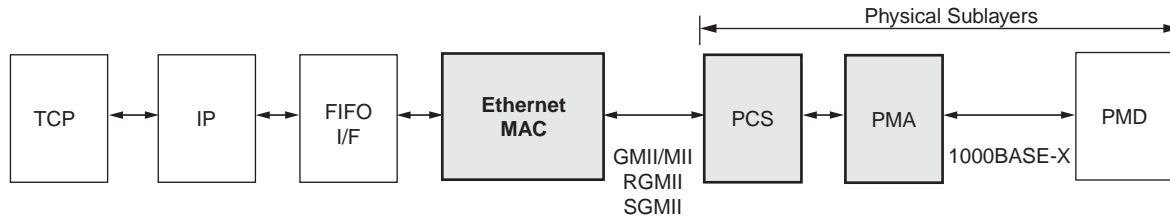


Figure 1: Typical Ethernet Architecture

Figure 1 displays the Ethernet MAC architecture from the MAC to the right, as defined in the *IEEE 802.3* specification, and also illustrates where the supported physical interfaces fit into the architecture.

MAC

The Ethernet MAC is defined in the *IEEE 802.3* specification clauses 2, 3, and 4. A MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can connect to, any type of physical sublayer.

GMII/MII

The Media Independent Interface (MII), defined in *IEEE 802.3* clause 22, is a parallel interface that connects a 10-Mb/s and/or 100-Mb/s capable MAC to the physical sublayers. The Gigabit Media Independent Interface (GMII), defined in *IEEE 802.3* clause 35, is an extension of the MII used to connect a 1-Gb/s capable MAC to the physical sublayers. MII can be considered a subset of GMII, and as a result, GMII/MII can carry Ethernet traffic at 10 Mb/s, 100 Mb/s, and 1 Gb/s. GMII/MII is supported at 2.5V only. See the *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide*.

RGMII

The Reduced-GMII (RGMII) is an alternative to GMII/MII. RGMII achieves a 50-percent reduction in the pin count, achieved by the use of double-data-rate (DDR) flip-flops. For this reason, RGMII is preferred over GMII by PCB designers. RGMII can carry Ethernet traffic at 10 Mb/s, 100 Mb/s, and 1 Gb/s.

SGMII

The Serial-GMII (SGMII) interface is an alternative to GMII/MII. SGMII converts the parallel interface of the GMII/MII into a serial format using a GTX serial transceiver, radically reducing the I/O count. For this reason, it is often the preferred interface of PCB designers. SGMII can carry Ethernet traffic at 10 Mb/s, 100 Mb/s, and 1 Gb/s.

PCS, PMA, PMD

The combination of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and the Physical Medium Dependent (PMD) sublayer comprise the physical layers of the Ethernet protocol.

Two main physical standards are specified for Ethernet:

- BASE-T, a copper standard using twisted pair cabling systems
- BASE-X, usually a fiber optical physical standard using short and long wavelength laser

BASE-T devices, supporting 10 Mb/s, 100 Mb/s, and 1 Gb/s Ethernet speeds, are readily available as off-the-shelf parts. As illustrated in [Figure 1](#) and [Figure 2](#), these can be connected using GMII/MII, RGMII, or SGMII to provide a tri-speed Ethernet port.

The Ethernet MAC has built-in 1000BASE-X PCS/PMA functionality and can be connected to a GTX serial transceiver to provide a 1 Gb/s fiber optic port, as illustrated in [Figure 3](#).

Applications

Typical applications for the Ethernet MAC core include

- [Ethernet Tri-speed BASE-T Port](#)
- [Ethernet 1000BASE-X Port](#)

Ethernet Tri-speed BASE-T Port

[Figure 2](#) illustrates a typical application for an Ethernet MAC. The PHY side of the core is implementing an external GMII/MII by connecting it to IOBs; the external GMII/MII is connected to an off-the-shelf Ethernet PHY device, which performs the BASE-T standard at 1 Gb/s, 100 Mb/s, and 10 Mb/s speeds. Alternatively, the external GMII/MII can be replaced with an RGMII (as shown) or as an SGMII (which requires the use of a GTX serial transceiver). GMII, RGMII, and SGMII functionality are demonstrated in the HDL examples provided with the example design.

The client side of the Ethernet MAC is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO (delivered with the example design) to complete a single Ethernet port. This port is displayed connected to a Switch or Routing matrix, which can contain several ports.

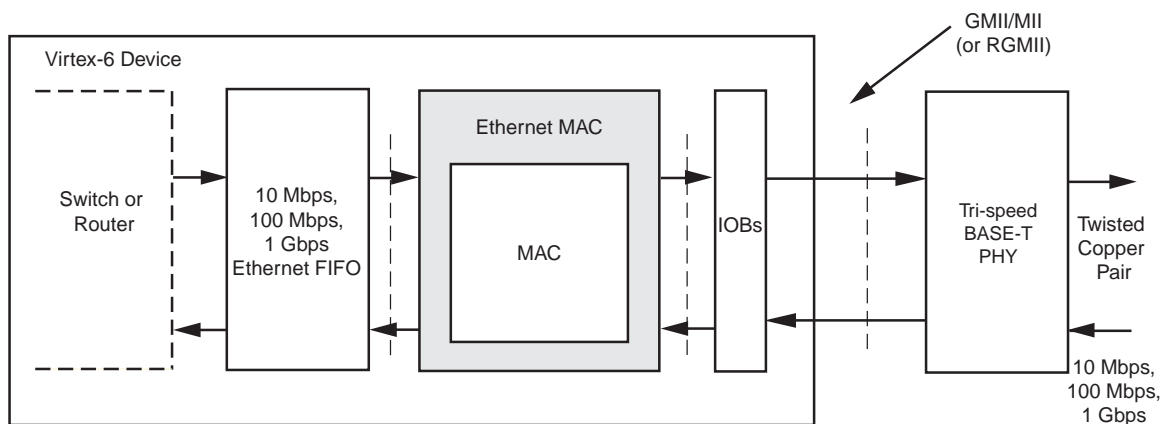


Figure 2: Typical 1000BASE-T Application

Ethernet 1000BASE-X Port

Figure 3 illustrates a typical application for an Ethernet MAC. The PHY side of the MAC is connected to a GTX serial transceiver, which in turn is connected to an external off-the-shelf GBIC or SFP optical transceiver. The 1000BASE-X PCS/PMA logic can be optionally provided by the Ethernet MAC, as displayed. 1000BASE-X functionality is demonstrated in the HDL examples provided with the example design.

The client side of the Ethernet MAC is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO (delivered with the example design) to complete a single Gigabit Ethernet port. This port is connected to a Switch or Routing matrix, which can contain several ports.

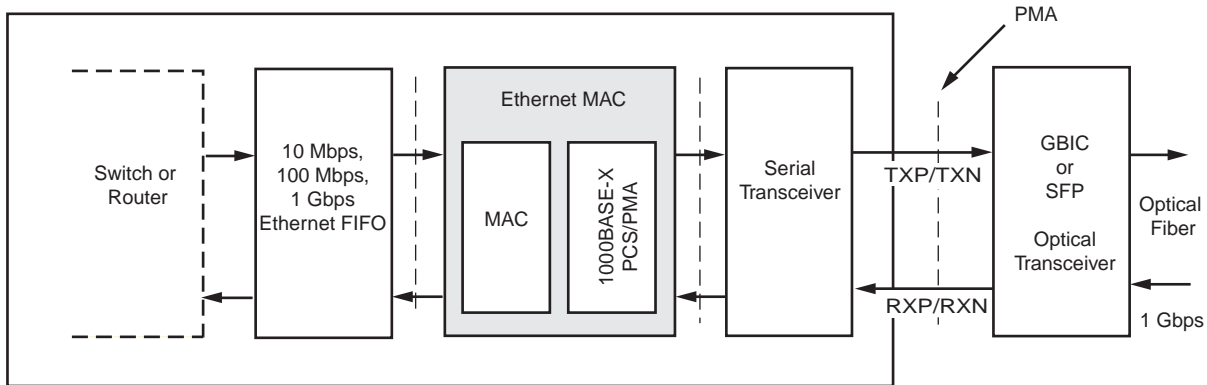


Figure 3: Typical 1000BASE-X Application

Example Design Overview

Figure 4 illustrates the major functional blocks of the Ethernet MAC example design. All illustrated components are provided in HDL, with the exception of the Ethernet MAC component.

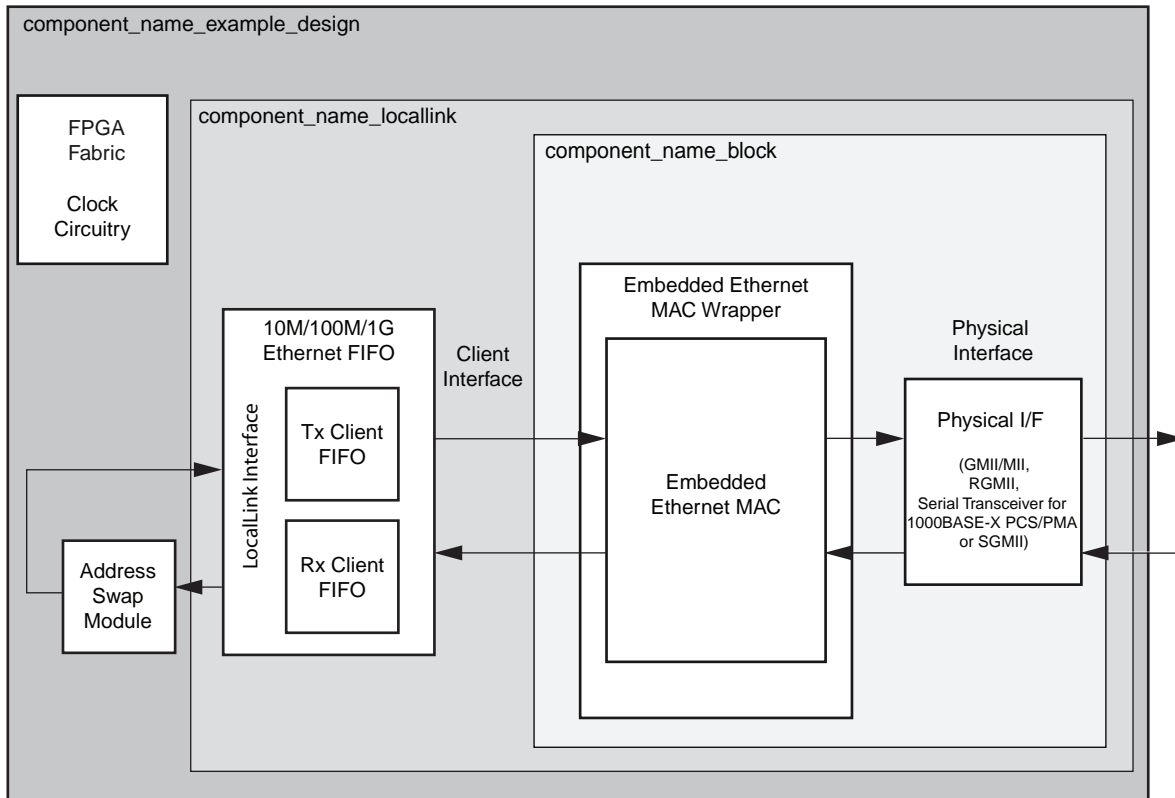


Figure 4: Example Design

Ethernet MAC Example Design

The example design is arranged for quick adaptation and can be downloaded onto an FPGA to provide a real hardware test environment. In addition, all the clock management logic required to operate the Ethernet MAC and its example design is provided. MMCMs, clock buffers, and so forth are instantiated as required.

The data is looped back at the client interface, enabling the Ethernet MAC to be quickly connected to a protocol tester—frames injected into the Ethernet MAC PHY Receive port are relayed back through the Ethernet MAC and out through the Ethernet MAC PHY Transmit port. Using this method, they are received back at the protocol tester.

The design includes an Address Swapping Module and a FIFO. Frames received by the Ethernet MAC are passed through the Receive side of the FIFO. Data from the Receive side of the FIFO is passed into the Address Swap Module and then on to the Transmit side of the FIFO using a LocalLink interface. The Transmit FIFO queues frames for transmission and connects directly to the client side Transmit interface of the Ethernet MAC.

Address Swap Module

The Address Swap Module switches the Destination Address and Source Address within the received MAC frame. Using this method, frames received from a link partner, for example a protocol tester, are relayed back to the correct Destination Address.

10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO

The 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO is a wrapper file around the Receive and Transmit FIFO components. These components can be used in more complex client applications, as illustrated in [Figure 2](#) and [Figure 3](#). To use the FIFOs, the `component_name_locallink` component can be instantiated in the user design.

Receive Client FIFO

The Receive (Rx) Client FIFO, a 4k-byte FIFO implemented in block RAM, can be used for more complex client applications and can be connected directly to the Rx Client Interface of the Ethernet MAC. The Rx Client provides a LocalLink connection for the user.

- The FIFO operates at all Ethernet speeds supported by the Ethernet MAC.
- The FIFO drops all frames marked as bad from the Ethernet MAC so that only error-free frames are passed to the Ethernet client.

Transmit Client FIFO

The Transmit (Tx) Client FIFO, a 4k-byte FIFO implemented in block RAM, can be used for more complex client applications and can be connected directly to the Tx Client Interface of the Ethernet MAC. The Tx Client FIFO provides a LocalLink connection for the user.

- The FIFO operates at all Ethernet speeds supported by the Ethernet MAC.
- The FIFO is capable of half-duplex re-transmission. For this reason, if a collision occurs on the medium, the Ethernet MAC indicates a collision on the Tx Client interface and the FIFO automatically re-queues the frame for re-transmission.

Ethernet MAC Wrapper

The Ethernet MAC wrapper file instantiates the full Ethernet MAC primitive.

- All unused input ports on the primitive are tied to the appropriate logic level; all unused output ports are left unconnected.
- The Ethernet MAC attributes are set based on options selected in the CORE Generator tool.
- Only used ports are connected to the ports of the wrapper file.

This simplified wrapper should be used as the instantiation template for the Ethernet MAC in customer designs.

Physical I/F

An appropriate Physical Interface is provided for the Ethernet MAC. This interface connects the physical interface of the Ethernet MAC block to the I/O of the FPGA. As required, these components are provided:

- For MII, this component contains Input/Output block (IOB) buffers and IOB flip-flops.
- For GMII, this component contains IOB buffers, IOB flip-flops, an IDELAYCTRL, and IODELAY elements to align the incoming data with the receiver clock.
- For RGMII, this component contains IOB buffers, IOB Double-Data Rate flip-flops, an IDELAYCTRL, and IODELAY elements to align the incoming data with the receiver clock. An IODELAY element is also used to delay the transmitted clock in RGMII v2.0.
- For 1000BASE-X PCS/PMA or SGMII, this component instantiates and connects a GTX serial transceiver.

Device Utilization

The following sections provide approximate device utilization figures for common configurations of the Ethernet MAC and its example design:

- [1 Gb/s Only Operation](#)
- [Tri-Speed Operation](#)
- [100 Mb/s or 10 Mb/s Operation](#)

Of interest is the utilization of clock resources, specifically the global clock usage (BUFGs), which can influence the selection of the interface type. These clock resource figures do not consider any clock that can be used for the host interface.

1 Gb/s Only Operation

[Table 1](#) defines approximate utilization figures for common configurations of the Ethernet MAC and its example design for 1 Gb/s operation. In supported devices, the 1000BASE-X (16-bit client) physical interface can also operate at 2 or 2.5 Gb/s.

Table 1: Device Utilization for 1 Gb/s Operation

Parameter Values	Device Resources					
Physical Interface	LUTs	Registers	RAMB36s	BUFGs	BUFRs	MMCMs
GMII	400	400	2	1 ⁽¹⁾	1	0
RGMII 1.3	390	410	2	1 ⁽¹⁾	1	0
RGMII 2.0	400	410	2	1 ⁽¹⁾	1	0
SGMII	410	420	2	1	1	0
1000BASE-X (8-bit client)	410	420	2	1	1	0
1000BASE-X (16-bit client)	280	470	2	4	1	1

1. These implementations use IODLEAY elements, which require a 200MHz reference clock for the associated IDELAYCTRL. The reference clock's BUFG is not accounted for.

Tri-Speed Operation

Table 2 defines approximate utilization figures for common configurations of the Ethernet MAC and its example design 10 Mb/s, 100 Mb/s, or 1 Gb/s operation.

Table 2: Device Utilization for Tri-Speed Operation

Parameter Values	Device Resources				
Physical Interface	LUTs	Registers	RAMB36s	BUFGs	BUFRs
GMII/MII (Standard Clocking)	360	430	2	4 ⁽¹⁾	1
GMII/MII (with Clock Enable)	380	440	2	1 ⁽¹⁾	1
RGMII 1.3 (Standard Clocking)	360	440	2	3 ⁽¹⁾	1
RGMII 1.3 (with Clock Enable)	380	450	2	1 ⁽¹⁾	1
RGMII 2.0 (Standard Clocking)	360	440	2	3 ⁽¹⁾	1
RGMII 2.0 (with Clock Enable)	380	450	2	1 ⁽¹⁾	1
SGMII	410	620	2.5 ⁽²⁾	2	2

1. These implementations use IODLEAY elements, which require a 200MHz reference clock for the associated IDELAYCTRL. The reference clock's BUFG is not accounted for.
2. Tri-speed SGMII configurations use 2 RAMB36 resources, plus an additional RAMB18 resource to implement the receive elastic buffer.

100 Mb/s or 10 Mb/s Operation

Table 3 provides approximate utilization figures for common configurations of the Ethernet MAC and its example design for 10 Mb/s or 100 Mb/s operation. For all other interfaces, see [Tri-Speed Operation, page 8](#).

Table 3: Device Utilization for 10 Mb/s, 100 Mb/s Operation

Parameter Values	Device Resources			
Physical Interface	LUTs	Registers	RAMB36s	BUFGs
MII (Standard Clocking)	410	410	2	4
MII (with Clock Enable)	430	420	2	2

Performance

Table 4 specifies the maximum supported performance of the Ethernet MAC in various Virtex-6 devices. For a matrix of supported configurations, see the *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide*.

Table 4: Performance Capabilities

Performance	Virtex-6 Devices			
	LXT	SXT	HXT	CXT
10 Mb/s / 100 Mb/s / 1 Gb/s	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes	Yes
1000BASE-X overclocking at 2 or 2.5 Gb/s	Yes ⁽¹⁾	Yes ⁽¹⁾	Yes	No

1. Varies for Virtex-6 Lower Power devices (-1L speed grades). See Performance in Virtex-6 Lower Power Devices in the next section.

Performance in Virtex-6 Lower Power Devices

Following are Ethernet MAC limitations for Virtex-6 Lower Power devices (-1L speed grades):

- 1000BASE-X overclocking at 2 or 2.5 Gb/s is not supported for these devices.
- Use of the GMII physical interface for 1 Gb/s operation will not meet the receiver setup and/or hold time requirements of the GMII specification by a total of at least 165 ps. Sufficient system margin and IODELAY tap settings are necessary for correct operation. See Xilinx [Answer Record 33195](#) for more details.
- Use of the RGMII physical interface for 1 Gb/s operation is marginal with respect to the receiver timing specification. Sufficient system margin and IODELAY tap settings are necessary for correct operation. See Xilinx [Answer Record 33195](#) for more details.

Hardware Verification

The core has been tested on the ML605 Virtex-6 LXT FPGA test board. The design comprises the Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC Wrapper, a ping loopback FIFO, and a test pattern generator all under embedded processor control. This design successfully passed IEEE 802.3 conformance testing at UNH IOL.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Ethernet MAC wrapper is provided under the [End User License Agreement](#) and can be generated using CORE Generator software v13.1 and higher. The CORE Generator software is shipped with Xilinx ISE® Design Suite Series Development software.

In ISE v11.4 and later, a license key is not required to access the IP. To access the wrapper in ISE v11.4 and older, a no cost full license must be obtained from Xilinx. See the product page www.xilinx.com/products/ipcenter/V6_Embedded_TEMAC_Wrapper.htm.

Contact your local Xilinx [sales representative](#) for pricing and availability about Xilinx LogiCORE IP modules and software or see the Xilinx [IP Center](#).

List of Acronyms

Table 5: List of Acronyms

Acronym	Spelled Out
DDR	Double Data Rate
FF	Flip-Flop
FIFO	First In First Out
FPGA	Field Programmable Gate Array
Gb/s	Gigabits per second
GBIC	Gigabit Interface Converter
GMII	Gigabit Media Independent Interface
HDL	Hardware Description Language
I/F	Interface
I/O	Input/Output
IES	Incisive Enterprise Simulator
IOB	Input Output Block
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
Mb/s	Megabits per second
MII	Media Independent Interface
MMCM	Mixed-Mode Clock Manager
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
ps	picoseconds
RAM	Random Access Memory
RGMII	Reduced Gigabit Media Independent Interface
Rx	Receive
SFP	Start of Frame Delimiter
SGMII	Serial Gigabit Media Independent Interface
Tx	Transmit
UCF	User Constraints File
VCS	Verilog Compiled Simulator (Synopsys)
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
XST	Xilinx Synthesis Technology

Revision History

This table shows the revision history for this document:

Date	Version	Description of Revisions
6/24/09	1.5	Initial Xilinx release. Updated to core v1.2 and ISE v11.2. Added Virtex-6 CXT support.
9/16/09	2.0	Updated to core v1.3 and ISE v11.3. Added Virtex-6 HXT and Virtex-6 -1L support.
10/15/09	2.0.1	Updated Ordering Information.
4/19/10	3.0	Updated to core v1.4 and ISE v12.1.
3/01/11	4.0	Updated to core v1.5 and ISE v13.1.

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