

Introduction

The Xilinx[®] Platform Studio (XPS) System Monitor (SYSMON) Analog-to-Digital Converter (ADC) Intellectual Property (IP) core is a 32-bit slave peripheral that connects to the PLB (Processor Local Bus) and provides the controller interface for the SYSMON hard macro on the Virtex[®]-5 and Virtex-6 family of Field Programmable Gate Arrays (FPGAs). This document describes the specifications for the XPS SYSMON ADC IP core. It is assumed that the user is familiar with the SYSMON hard macro. For information on the SYSMON hard macro, see the System Monitor user guide mentioned in [Reference Documents](#) section.

Features

- Connects as a 32-bit slave on PLB V4.6 buses of 32, 64, or 128 bits
- Uses the dedicated System Monitor (SYSMON) hard macro on Virtex-5 and Virtex-6 devices
- Supports the 10-bit, 200-KSPS (Kilo-Samples Per Second) Analog-to-Digital Converter (ADC)
- Supports on-chip monitoring of supply voltages and temperature
- Supports 1 dedicated high bandwidth differential analog-input pair and 16 auxiliary low bandwidth differential analog-input pairs
- Supports automatic alarms based on user defined limits
- Supports optional interrupt request generation
- Supports configurable cycle time for read and write operations

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	Virtex-6 ⁽²⁾ , Virtex-5
Supported User Interfaces	PLB Interface
Resources	
See Table 13 and Table 14 .	
Provided with Core	
Documentation	Product Specification
Design Files	VHSIC Hardware Description Language (VHDL)
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	N/A
Tested Design Tools ⁽³⁾	
Design Entry Tools	XPS
Simulation	ModelSim
Synthesis Tools	Xilinx Synthesis Technology (XST)
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For a complete list of supported derivative devices, see the [IDS Embedded Edition Derivative Device Support](#).
2. For more information on the Virtex-6 devices, see the [DS150 Virtex-6 Family Overview](#)
3. For the supported versions of the tools, see the [ISE Design Suite 13: Release Notes Guide](#).

Functional Description

The top-level block diagram for the XPS SYSMON ADC IP core is shown in Figure 1.

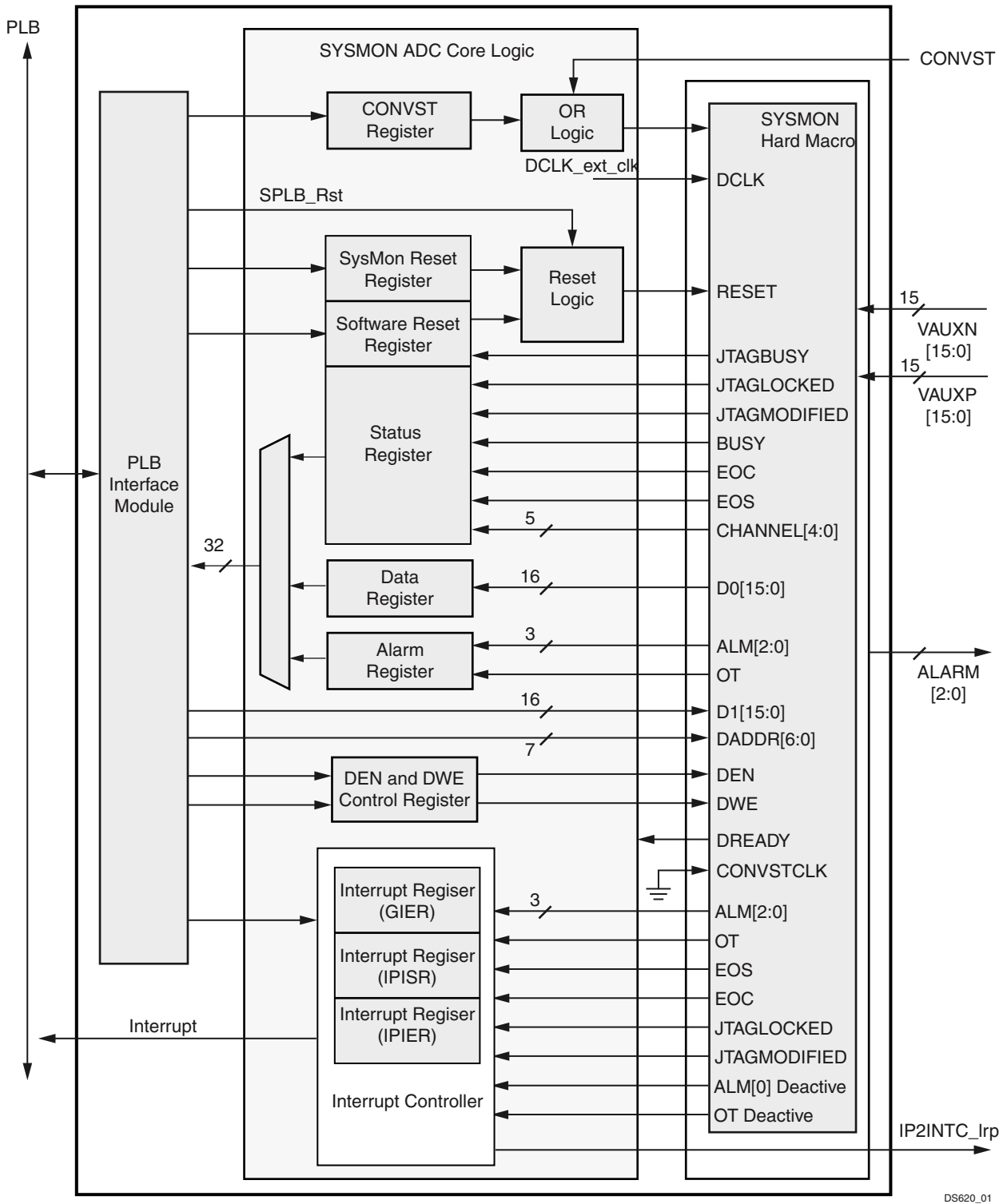


Figure 1: Block Diagram of the XPS SYSMON ADC Core

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The XPS SYSMON ADC IP core consists of following major blocks.

- PLB Interface Module
- SYSMON ADC Core Logic
- SYSMON Hard Macro

PLB Interface Module

The PLB Interface Module provides the interface to the PLB. Read and write transactions at the PLB are translated into equivalent SYSMON ADC core logic and SYSMON hard macro transactions. The register interfaces of the SYSMON ADC core Logic Module connect to the PLB Interface Module. The PLB Interface Module also provides an address decoding service.

SYSMON ADC Core Logic

The SYSMON ADC core Logic Module provides necessary address decoding logic, control signal generation and interface between the PLB and the SYSMON hard macro. The read/write requests along with the address and data (in case of write) from the PLB Interface Module are transferred to either the Dynamic Reconfiguration Port (DRP) registers of the SYSMON hard macro or local registers in the IP along with the necessary control signals, such as DEN and DWE.

If the SYSMON ADC Core Logic Module supports including/excluding the Interrupt Controller based on generic `C_INCLUDE_INTR`. If `C_INCLUDE_INTR = 1`, then the Interrupt Controller is included in the design.

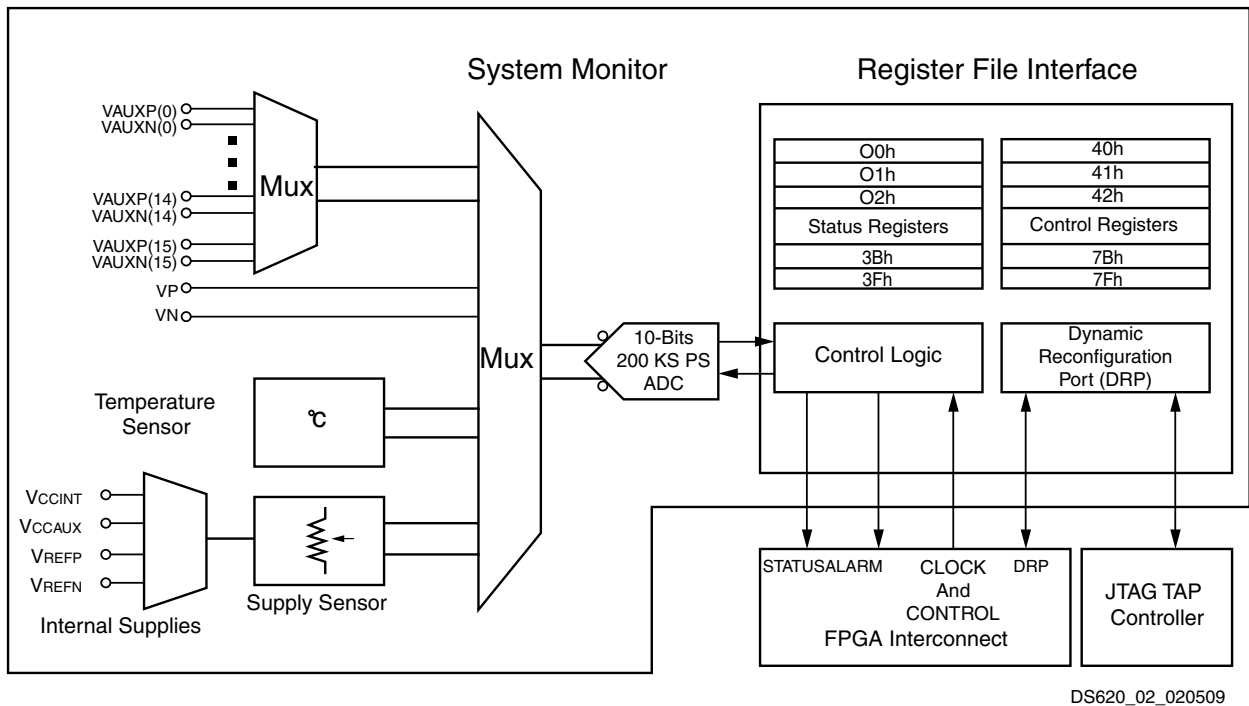
There is a new Design Rule Checker (DRC) limitation which has been imposed on the DCLK input clock of SYSMON hard macro on Virtex-6 devices. The DCLK for the hard macro must not exceed 80 Mega Hertz (MHz) value. To take care of this limitation a new parameter '`C_DCLK_RATIO`' is added in the design. Based upon the core frequency (when used in the system), this parameter needs to be set in such a way as to make the DCLK less than or equal to 80 MHz. These constraints are applicable only for the Virtex-6 device. Users must make sure that the maximum clock at this port is 80 MHz. If this clock increases beyond 80 MHz, then a DRC violation related to the SYSMON hard macro will be raised and the hard macro may not work properly. For all Virtex-5 devices, this parameter should be assigned to '1'. In short, the SYSMON hard macro on Virtex-5 devices can operate at the core frequency which can be beyond 80 MHz.

The `C_DCLK_RATIO` supports a range of values between 1 to 8. Internally, this value is used to divide the clock. It is strongly recommended that the value of `C_DCLK_RATIO` should be set in such a way that, the DCLK input frequency is always equal to 80 MHz or close to 80 MHz. Read [Precautions to be taken while Assigning the C_DCLK_RATIO Parameter](#).

The SYSMON hard macro can be accessed via both Joint Test Action Group (JTAG) TAP (Test Access Port) and the XPS SYSMON ADC IP core. When simultaneous access of the SYSMON hard macro occurs, the JTAGLOCKED port can be asserted High by JTAG TAP. In this scenario, the XPS SYSMON ADC IP Core is not allowed to do any read/write access from/to DRP. When the JTAGLOCKED port is again deasserted through JTAG TAP, the XPS SYSMON ADC IP core can perform a read/write operation from/to DRP.

This functionality is especially useful in applications where the user is configuring DRP through JTAG TAP and does not want the FPGA logic (XPS SYSMON ADC IP core) to alter the configuration. The user can make `JTAGLOCKED = '1'` through JTAG TAP, which blocks any read and write transactions from or to DRP through the FPGA logic and thus ensures a non-destructive access through the JTAG TAP.SYSMON Hard Macro

The SYSMON hard macro is present in every Virtex-5 and Virtex-6 FPGA. The block diagram for the System Monitor ADC hard macro on a Virtex-5 FPGA is shown in [Figure 2](#).



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Figure 2: Block Diagram of the XPS SYSMON ADC Core

The XPS SYSMON ADC IP core is built around the dedicated System Monitor hard macro on the Virtex-5 and Virtex-6 device family. The hard macro uses a 10-bit, 200-KSPS ADC internally for conversion of various analog data. The XPS SYSMON ADC IP core is used to measure die temperature and voltage. Additionally, the XPS SYSMON ADC IP core provides analog-to-digital conversion of up to 17 external channels. From a user point of view, the core is defined as an XPS SYSMON ADC which can operate to monitor on-chip voltage and temperature and external analog voltages, or both.

The SYSMON hard macro consists of a Register File Interface (RFI) which in turn consists of Status and Control registers. Status registers are read-only and contain the results of analog-to-digital conversion of the on-chip sensors and external channels. The status registers also store the maximum and minimum temperature and VCCAUX/VCCINT voltages. The control registers are used to configure the SYSMON hard macro operation. The SYSMON hard macro functionality (ADC operating modes, Channel Sequencer, and Alarm limits) is controlled through these registers. The first three registers in the control register block are also called Configuration Registers, which are used to configure the SYSMON hard macro operating modes. In addition to RFI of the hard macro, the XPS SYSMON ADC IP core consists of a set of local register and optional interrupt registers.

The SYSMON hard macro provides channel sequencing, averaging and filtering functions. Many of the 16-bit registers are not defined in SYSMON hard macro RFI. Accessing a location which is undefined returns an undefined value.

In the SYSMON hard macro, a channel sequencer allows the user to specify the channels monitored but the sequence order is fixed. Users can specify an averaging filter to reduce noise. There are programmable alarm thresholds for the on-chip sensors, and if an on-chip temperature or voltage is enabled and outside the specified limit, an alarm is activated.

Structurally, the XPS SYSMON ADC IP Core consists of the SYSMON hard macro, the PLB Interface Module, Optional Interrupt Source Controller Module, Soft Reset Module, SYSMON Reset Register, and additional logic to interface to the core. The Soft Reset Module provides a way for resetting the entire IP without disturbing the entire system. The SYSMON Reset Register is provided to reset the SYSMON hard macro only.

All read and write operations to the configuration and limit registers are synchronized to DCLK (the DCLK input of SYSMON hard macro is connected to `SPLB_Clk`). The SYSMON hard macro has an internal clock divider which divides DCLK by any integer ranging from 2 to 255 to generate ADCCLK, which is an internal clock used by the ADC. Because an internal clock divider is provided, the DCLK frequency can be in the range of 2 MHz to 200 MHz in the case of Virtex-5 devices and 2 MHz to 80 MHz in the case of Virtex-6 devices. See the Virtex-5 and Virtex-6 FPGA data sheets for the maximum operating frequency of the XPS SYSMON ADC core.

The SYSMON hard macro operates either in event-driven or continuous-sampling mode. In event-driven sampling mode, the conversion process is initiated on the rising edge of CONVST. The XPS SYSMON ADC core supports this operation by providing a rising-edge signal on the external CONVST port or by writing into the CONVST Register. In continuous sampling mode, the ADC continues to carry out a conversion on the selected analog inputs as long as the ADCCLK (DCLK) is present. For more information on the SYSMON hard macro, see the System Monitor user guide mentioned in [Reference Documents](#) section.

Design Parameters

To allow the user to obtain an XPS SYSMON ADC IP core that is uniquely tailored for the system, certain features can be parameterized in the XPS SYSMON ADC design. This allows the user to configure a design that utilizes the resources required by the system only and that operates with the best possible performance. The features that can be parameterized are shown in [Table 1](#).

Table 1: XPS SYSMON ADC Design Parameters

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters					
G1	Target FPGA family	C_FAMILY	virtex5, virtex6	virtex5	string
PLB Parameters					
G2	PLB base address	C_BASEADDR	Valid Address ⁽¹⁾	None ⁽²⁾	std_logic_vector
G3	PLB high address	C_HIGHADDR	Valid Address ⁽¹⁾	None ⁽²⁾	std_logic_vector
G4	PLB least significant address bus width	C_SPLB_AWIDTH	32	32	integer
G5	PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
G6	Shared bus topology	C_SPLB_P2P	0 = Shared bus topology ⁽³⁾	0	integer
G7	PLB master ID bus Width	C_SPLB_MID_WIDTH	$\log_2(\text{C_SPLB_NUM_MASTERS})$ with a minimum value of 1	1	integer
G8	Number of PLB masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
G9	Width of the slave data bus	C_SPLB_NATIVE_DWIDTH	32	32	integer
G10	Burst support	C_SPLB_SUPPORT_BURSTS	0 = No burst support ⁽⁴⁾	0	integer
XPS SYSMON ADC Parameters					

Table 1: XPS SYSMON ADC Design Parameters (Cont'd)

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G11	Include/Exclude interrupt support	C_INCLUDE_INTR	0 = Exclude interrupt support 1 = Include interrupt support	1	integer
G12	File name for Analog input stimuli	C_SIM_MONITOR_FILE	string	Design.txt	string
G13	DCLK clock division ratio	C_DCLK_RATIO	1,2,3,4,5,6,7,8 ⁽⁵⁾	1 ⁽⁶⁾	string

Notes:

1. The range C_BASEADDR to C_HIGHADDR is the address range for the XPS SYSMON ADC core. This range is subject to restrictions to accommodate the simple address decoding scheme that is employed: The size, C_HIGHADDR - C_BASEADDR + 1, must be a power of two and must be at least 0x400 to accommodate all XPS SYSMON ADC core registers. However, a larger power of two can be chosen to reduce decoding logic. C_BASEADDR must be aligned to a multiple of the range size.
2. No default value is specified to ensure that an actual value appropriate to the system is set.
3. Point-to-point bus topology is not supported.
4. Burst is not supported.
5. Based upon the core frequency, this parameter should be set to generate the DCLK frequency less than or equal to 80 MHz. The C_DCLK_RATIO supports a range of values between 1 to 8. Internally, this value is used to divide the clock. It is strongly recommended that, the value of C_DCLK_RATIO should be set in such a way that, the DCLK input frequency to the SYSMON macro is always equal to 80 MHz or close to 80 MHz. If the value chosen for C_DCLK_RATIO causes the DCLK to operate at very low value, then the SYSMON macro takes a longer time to generate the DRDY signal and can hamper the core functionality and efficiency while working with the interconnect. See [Precautions to be taken while Assigning the C_DCLK_RATIO Parameter, page 24](#) before using this parameter.
6. This parameter is set to 1 as default for all Virtex-5 devices. For all Virtex-6 devices this parameter needs to be assigned some value. For Virtex-6 devices, the value of 1 is allowed when the core frequency is not exceeding the 80 MHz limit.

I/O Signals

The XPS SYSMON ADC Input/Output (I/O) signals are listed and described in [Table 2](#).

Table 2: I/O Signal Descriptions

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	SPLB_Clk	System	I	-	PLB clock
P2	SPLB_Rst	System	I	-	PLB reset, active high
P3	IP2INTC_Irpt	System	O	0	Interrupt control signal from XPS SYSMON ADC
PLB Interface Signals					
P4	PLB_ABus[0 : 31]	PLB	I	-	PLB address bus
P5	PLB_PAVValid	PLB	I	-	PLB primary address valid
P6	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P7	PLB_RNW	PLB	I	-	PLB read not write
P8	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	PLB	I	-	PLB byte enables
P9	PLB_size[0 : 3]	PLB	I	-	PLB size of requested transfer
P10	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P11	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus

Table 2: I/O Signal Descriptions (Cont'd)

Port	Signal Name	Interface	I/O	Initial State	Description
Unused PLB Interface Signals					
P12	PLB_UABus[0 : 31]	PLB	I	-	PLB upper address bits
P13	PLB_SAVValid	PLB	I	-	PLB secondary address valid
P14	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P15	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P16	PLB_abort	PLB	I	-	PLB abort bus request
P17	PLB_busLock	PLB	I	-	PLB bus lock
P18	PLB_MSize[0 : 1]	PLB	I	-	PLB data bus width indicator
P19	PLB_lockErr	PLB	I	-	PLB lock error
P20	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P21	PLB_rdBurst	PLB	I	-	PLB burst read transfer
P22	PLB_wrPendReq	PLB	I	-	PLB pending bus write request
P23	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P24	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P25	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending read request priority
P26	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
P27	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute
PLB Slave Interface Signals					
P28	SI_addrAck	PLB	O	0	Slave address acknowledge
P29	SI_SSize[0 : 1]	PLB	O	0	Slave data bus size
P30	SI_wait	PLB	O	0	Slave wait
P31	SI_rearbitrate	PLB	O	0	Slave bus re-arbitrate
P32	SI_wrDAck	PLB	O	0	Slave write data acknowledge
P33	SI_wrComp	PLB	O	0	Slave write transfer complete
P34	SI_rdDBus[0 : C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P35	SI_rdDAck	PLB	O	0	Slave read data acknowledge
P36	SI_rdComp	PLB	O	0	Slave read transfer complete
P37	SI_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P38	SI_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P39	SI_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					
P40	SI_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P41	SI_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P42	SI_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P43	SI_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request

Table 2: I/O Signal Descriptions (Cont'd)

Port	Signal Name	Interface	I/O	Initial State	Description
XPS SYSMON ADC IP Core Interface Signals					
P44	VAUXP[15 : 0]	SYSMON	I	-	Positive auxiliary differential analog inputs
P45	VAUXN[15 : 0]	SYSMON	I	-	Negative auxiliary differential analog inputs
P46	CONVST	SYSMON	I	-	Convert Start input port is used to control the sampling instant on the ADC input and is used only in event-driven sampling mode. This port is auto connected to ground internally, if not in use.
P47	ALARM[2:0]	SYSMON	O	0	SYSMON hard macro Alarm output signals

Parameter - Port Dependencies

The dependencies between the XPS SYSMON ADC IP core design parameters and I/O signals are described in Table 3.

Table 3: Parameter-Port Dependencies

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G5	C_SPLB_DWIDTH	P8, P11, P34	-	Affects the number of bits in data bus
G7	C_SPLB_MID_WIDTH	P6	G8	This value is calculated as: $\log_2(\text{C_SPLB_NUM_MASTERS})$ with a minimum value of 1
G8	C_SPLB_NUM_MASTERS	P37, P38, P39, P43	-	Affects the number of PLB masters
I/O Signals				
P6	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	-	G7	Width of the PLB_mastedID varies according to C_SPLB_MID_WIDTH
P8	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	-	G5	Width of the PLB_BE varies according to C_SPLB_DWIDTH
P11	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	-	G5	Width of the PLB_wrDBus varies according to C_SPLB_DWIDTH
P34	SI_rdDBus[0 : C_SPLB_DWIDTH - 1]	-	G5	Width of the SI_rdDBus varies according to C_SPLB_DWIDTH
P37	SI_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MBusy varies according to C_SPLB_NUM_MASTERS
P38	SI_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MWrErr varies according to C_SPLB_NUM_MASTERS

Table 3: Parameter-Port Dependencies (Cont'd)

Generic or Port	Name	Affects	Depends	Relationship Description
P39	SI_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MRdErr varies according to C_SPLB_NUM_MASTERS
P43	SI_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MIRQ varies according to C_SPLB_NUM_MASTERS

Register Descriptions

Table 4 shows the XPS SYSMON ADC IP core registers and their corresponding addresses.

Table 4: Core Registers

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
XPS SYSMON ADC Local Register Grouping				
C_BASEADDR + 0x00	Software Reset Register (SRR)	Write ⁽¹⁾	N/A	Software reset register
C_BASEADDR + 0x04	Status Register (SR)	Read ⁽²⁾	N/A	Status register
C_BASEADDR + 0x08	Alarm Output Status Register (AOSR)	Read ⁽²⁾	0x0	Alarm output status register
C_BASEADDR + 0x0C	CONVST Register (CONVSTR)	Write ⁽¹⁾	N/A	ADC convert start register ⁽³⁾
C_BASEADDR + 0x10	SYSMON Reset Register (SYSMONRR)	Write ⁽¹⁾	N/A	SYSMON hard macro reset register
XPS SYSMON ADC Interrupt Controller Register Grouping				
C_BASEADDR + 0x5C	Global Interrupt Enable Register (GIER)	R/W	0x0	Global interrupt enable register
C_BASEADDR + 0x60	IP Interrupt Status Register (IPISR)	R/TOW ⁽⁴⁾	N/A	IP interrupt status register
C_BASEADDR + 0x68	IP Interrupt Enable Register (IPIER)	R/W	0x0	IP interrupt enable register
SYSMON Hard Macro Register Grouping ⁽⁵⁾				
C_BASEADDR + 0x200	Temperature	Read ⁽⁶⁾	N/A	The 10-bit Most Significant Bit (MSB) justified result of on-chip temperature measurement is stored in this register
C_BASEADDR + 0x204	V _{CCINT}	Read ⁽⁶⁾	N/a	The 10-bit MSB justified result of on-chip V _{CCINT} supply monitor measurement is stored in this register
C_BASEADDR + 0x208	V _{CCAUX}	Read ⁽⁶⁾	N/A	The 10-bit MSB justified result of on-chip V _{CCAUX} Data supply monitor measurement is stored in this register

Table 4: Core Registers (Cont'd)

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x20C	V _P /V _N	R/W ⁽⁷⁾	0x0	When read: The 10-bit MSB justified result of Analog-to-Digital (A/D) conversion on the dedicated analog input channel (V _p /V _n) is stored in this register When written: Write to this register resets the SYSMON hard macro. No specific data is required. Applicable only when the Virtex-6 device is targeted.
C_BASEADDR + 0x210	V _{REFP}	Read	0x0	The 10-bit MSB justified result of A/D conversion on the reference input V _{REFP} is stored in this register.
C_BASEADDR + 0x214	V _{REFN}	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the reference input V _{REFN} is stored in this register.
C_BASEADDR + 0x218 to C_BASEADDR + 0x21C	Undefined	N/A	Undefined	These locations are unused and contain invalid data.
C_BASEADDR + 0x220	Supply Offset	Read ⁽⁶⁾	N/A	The calibration coefficient for the supply sensor offset is stored in this register.
C_BASEADDR + 0x224	ADC Offset	Read ⁽⁶⁾	N/A	The calibration coefficient for the ADC offset calibration is stored in this register.
C_BASEADDR + 0x228	Gain Error	Read ⁽⁶⁾	N/A	The calibration coefficient for the gain error is stored in this register.
C_BASEADDR + 0x22C to C_BASEADDR + 0x23C	Undefined	N/A	Undefined	These locations are unused and contain invalid data
C_BASEADDR + 0x240	V _{AUXP} [0]/ V _{AUXN} [0]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 0 is stored in this register.
C_BASEADDR + 0x244	V _{AUXP} [1]/ V _{AUXN} [1]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 1 is stored in this register.
C_BASEADDR + 0x248	V _{AUXP} [2]/ V _{AUXN} [2]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 2 is stored in this register.
C_BASEADDR + 0x24C	V _{AUXP} [3]/ V _{AUXN} [3]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 3 is stored in this register.
C_BASEADDR + 0x250	V _{AUXP} [4]/ V _{AUXN} [4]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 4 is stored in this register.
C_BASEADDR + 0x254	V _{AUXP} [5]/ V _{AUXN} [5]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 5 is stored in this register
C_BASEADDR + 0x258	V _{AUXP} [6]/ V _{AUXN} [6]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 6 is stored in this register.
C_BASEADDR + 0x25C	V _{AUXP} [7]/ V _{AUXN} [7]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 7 is stored in this register.

Table 4: Core Registers (Cont'd)

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x260	V _{AUXP} [8]/ V _{AUXN} [8]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 8 is stored in this register.
C_BASEADDR + 0x264	V _{AUXP} [9]/ V _{AUXN} [9]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 9 is stored in this register.
C_BASEADDR + 0x268	V _{AUXP} [10]/ V _{AUXN} [10]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 10 is stored in this register.
C_BASEADDR + 0x26C	V _{AUXP} [11]/ V _{AUXN} [11]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 11 is stored in this register.
C_BASEADDR + 0x270	V _{AUXP} [12]/ V _{AUXN} [12]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 12 is stored in this register.
C_BASEADDR + 0x274	V _{AUXP} [13]/ V _{AUXN} [13]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 13 is stored in this register.
C_BASEADDR + 0x278	V _{AUXP} [14]/ V _{AUXN} [14]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 14 is stored in this register.
C_BASEADDR + 0x27C	V _{AUXP} [15]/ V _{AUXN} [15]	Read ⁽⁶⁾	0x0	The 10-bit MSB justified result of A/D conversion on the auxiliary analog input 15 is stored in this register.
C_BASEADDR + 0x280	Max Temp	Read ⁽⁶⁾	N/A	The 10-bit MSB justified maximum temperature measurement.
C_BASEADDR + 0x284	Max V _{CCINT}	Read ⁽⁶⁾	N/A	The 10-bit MSB justified maximum V _{CCINT} measurement.
C_BASEADDR + 0x288	Max V _{CCAUX}	Read ⁽⁶⁾	N/A	The 10-bit MSB justified maximum V _{CCAUX} measurement.
C_BASEADDR + 0x28C	Undefined	N/A	Undefined	This location is unused and contains invalid data.
C_BASEADDR + 0x290	Min Temp	Read ⁽⁶⁾	N/A	The 10-bit MSB justified minimum temperature measurement.
C_BASEADDR + 0x294	Min V _{CCINT}	Read ⁽⁶⁾	N/A	The 10-bit MSB justified minimum V _{CCINT} measurement.
C_BASEADDR + 0x298	Min V _{CCAUX}	Read ⁽⁶⁾	N/A	The 10-bit MSB justified minimum V _{CCAUX} measurement.
C_BASEADDR + 0x29C to C_BASEADDR + 0x2F8	Undefined	N/A	Undefined	These locations are unused and contain invalid data.
C_BASEADDR + 0x2FC	Flag Register	Read ⁽⁶⁾	N/A	The 16-bit register gives general status information of ALARM, Over Temperature (OT), Disable information of SYSMON and information whether the SYSMON is using internal reference voltage or external reference voltage.
C_BASEADDR + 0x300	Configuration Register 0	R/W ⁽⁹⁾	0x0	SYSMON Configuration register 0

Table 4: Core Registers (Cont'd)

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x304	Configuration Register 1	R/W ⁽⁹⁾	0x0	SYSMON Configuration register 1
C_BASEADDR + 0x308	Configuration Register 2	R/W ⁽⁹⁾	0x1E00	SYSMON Configuration register 2
C_BASEADDR + 0x30C to C_BASEADDR + 0x31C	Test register 0 to 4	N/A	N/A	SYSMON Test register 0 to 4 (for factory test only)
C_BASEADDR + 0x320	Sequence Register 0	R/W	0x0	SYSMON Sequence register 0 (ADC channel selection)
C_BASEADDR + 0x324	Sequence Register 1	R/W	0x0	SYSMON Sequence register 1 (ADC channel selection)
C_BASEADDR + 0x328	Sequence Register 2	R/W	0x0	SYSMON Sequence register 2 (ADC channel averaging enable)
C_BASEADDR + 0x32C	Sequence Register 3	R/W	0x0	SYSMON Sequence register 3 (ADC channel averaging enable)
C_BASEADDR + 0x330	Sequence Register 4	R/W	0x0	SYSMON Sequence register 4 (ADC channel analog-input mode)
C_BASEADDR + 0x334	Sequence Register 5	R/W	0x0	SYSMON Sequence register 5 (ADC channel analog-input mode)
C_BASEADDR + 0x338	Sequence Register 6	R/W	0x0	SYSMON Sequence register 6 (ADC channel acquisition time)
C_BASEADDR + 0x33C	Sequence Register 7	R/W	0x0	SYSMON Sequence register 7 (ADC channel acquisition time)
C_BASEADDR + 0x340	Alarm Threshold Register 0	R/W	0x0	The 10-bit MSB justified alarm threshold register 0 (Temperature Upper)
C_BASEADDR + 0x344	Alarm Threshold Register 1	R/W	0x0	The 10-bit MSB justified alarm threshold register 1 (V _{CCINT} Upper)
C_BASEADDR + 0x348	Alarm Threshold Register 2	R/W	0x0	The 10-bit MSB justified alarm threshold register 2 (V _{CCAUX} Upper)
C_BASEADDR + 0x34C	Alarm Threshold Register 3	R/W ⁽⁹⁾⁽¹⁰⁾	0x0	The 12-bit MSB justified alarm threshold register 3 (OT Upper)
C_BASEADDR + 0x350	Alarm Threshold Register 4	R/W	0x0	The 10-bit MSB justified alarm threshold register 4 (Temperature Lower)
C_BASEADDR + 0x354	Alarm Threshold Register 5	R/W	0x0	The 10-bit MSB justified alarm threshold register 5 (V _{CCINT} Lower)
C_BASEADDR + 0x358	Alarm Threshold Register 6	R/W	0x0	The 10-bit MSB justified alarm threshold register 6 (V _{CCAUX} Lower)
C_BASEADDR + 0x35C	Alarm Threshold Register 7	R/W	0x0	The 10-bit MSB justified alarm threshold register 7 (OT Lower)

Table 4: Core Registers (Cont'd)

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x360 to C_BASEADDR + 0x3FC	Undefined	N/A	Undefined	Do not Read/Write these register

Notes:

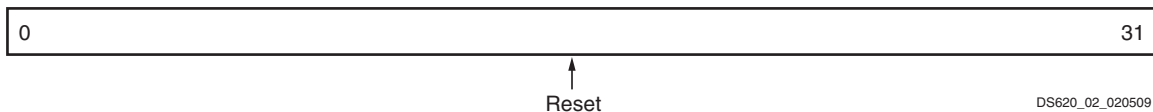
1. Reading of this register returns an undefined value.
2. Writing into this register has no effect.
3. Used in event-driven sampling mode only.
4. TOW = Toggle On Write. Writing a '1' to a bit position within the register causes the corresponding bit position in the register to toggle.
5. These are 16-bit registers internal to the SYMON hard macro. These are mapped to the lower half word boundary on the 32-bit XPS SYMON ADC IP core registers. For more detail See the System Monitor Register File Interface section in the Virtex-5 and Virtex-6 System Monitor User Guide,UG192 (latest version).
6. Writing to this SYSMON hard macro register is not allowed. The SYSMON ADC hard macro data registers are 16-bits in width. The SYSMON hard macro specification guarantees the first 10-MSB bits accuracy, so only these bits are used for reference.
7. Writing to this register resets the SYSMON hard macro. No specific data pattern is required to reset the SYSMON hard macro. Reading of this register gives the details of Vp/Vn port.
8. See the System Monitor User Guide, UG192 (latest version) for setting the different bits available in configuration registers for Virtex-5 and Virtex-6 devices.
9. The OT upper register is available only in Virtex-6 FPGAs. This register location is N/A when Virtex-5 devices are targeted.
10. The OT upper register is a user-configurable register for the upper threshold level of temperature. If this register is left unconfigured, then the SYSMON considers 125⁰C as the upper threshold value for OT. Note that, while configuring this register, the last 4-bits must be set to 0011 Alarm Threshold Register 3[3:0] = 0011. The upper 12 bits of this register are user configurable.

Local Register Grouping

It is expected that the XPS SYSMON ADC IP core registers are going to be accessed in their preferred-access mode only. If the write attempt is made to read-only registers, there is not any effect on register contents. If the write-only registers are read, then it results in undefined data. All the internal registers of the core must be accessed in 32-bit format. If any other kind of access, such as half word or byte access, is done for the XPS SYSMON ADC IP core's internal 32 bit registers, the transaction is completed with an error generation for the corresponding transaction.

Software Reset Register (SRR)

The Software Reset Register permits the programmer to reset the XPS SYSMON ADC IP core, including the SYSMON hard macro output ports (except JTAG related outputs), independently of other IP cores in the systems. To activate the software reset, the value 0x0000_000A must be written to the register. Any other access, read or write, has undefined results. The bit assignment in the software reset register is shown in Figure 3 and described in Table 5.



DS620_02_020509

Figure 3: Software Reset Register

Table 5: Software Reset Register Description (C_BASEADDR + 0x00)

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	Reset	Write only	N/A	The only allowed operation on this register is a write of 0x0000_000A, which resets the XPS SYSMON ADC IP Core. The reset is active only for two clock cycles.

Status Register (SR)

The Status Register contains the XPS SYSMON ADC IP core channel status and the End of Conversion (EOC), End of Sequence (EOS), and JTAG access signals. This register is read only. Any attempt to write the bits of the register does not change the bits. The Status Register bit definitions are shown in Figure 4 and explained in Table 6.

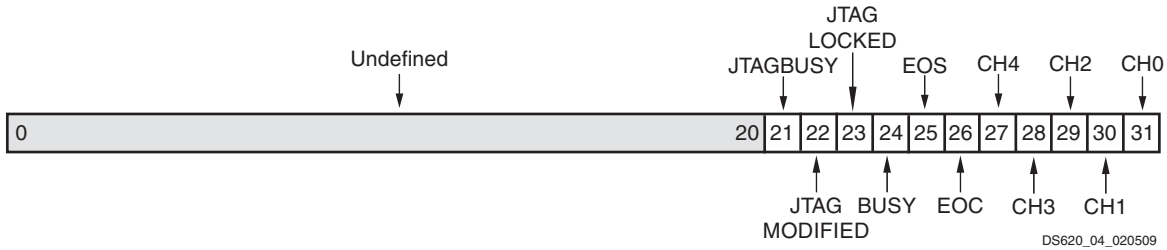


Figure 4: Status Register

Table 6: Status Register (C_BASEADDR + 0x04)

Bit(s)	Name	Core Access	Reset Value	Description
0 - 20	Undefined	N/A	N/A	Undefined
21	JTAGBUSY	Read	'0'	Used to indicate that a JTAG DRP transaction is in progress.
22	JTAG MODIFIED	Read	'0'	Used to indicate that a write to DRP through the JTAG interface has occurred. This bit is cleared when a successful DRP read/write operation through the FPGA logic is performed. The DRP read/write through FPGA logic fails, if JTAGLOCKED = '1'
23	JTAG LOCKED	Read	'0'	Used to indicate that a DRP port lock request has been made by the Joint Test Action Group (JTAG) interface.
24	BUSY	Read	N/A	ADC busy signal. This signal transitions high during an ADC conversion.
25	EOS	Read	N/A	End of Sequence. This signal transitions to an active High when the measurement data from the last channel in the auto sequence is written to the status registers. This bit is cleared when a read operation is performed on status register.
26	EOC	Read	N/A	End of Conversion signal. This signal transitions to an active High at the end of an ADC conversion when the measurement is written to the SYSMON hard macro's status register. This bit is cleared when a read operation is performed on status register.
27 - 31	CHANNEL [4 : 0]	Read	N/A	Channel selection outputs. The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.

Alarm Output Status Register (AOSR)

The Alarm Output Status Register contains all the alarm outputs for the XPS SYSMON ADC IP core. This register is read only. Any attempt to write the bits of the register does not change the bits. The Alarm Output Status Register bit definitions are shown in Figure 5 and explained in Table 7.

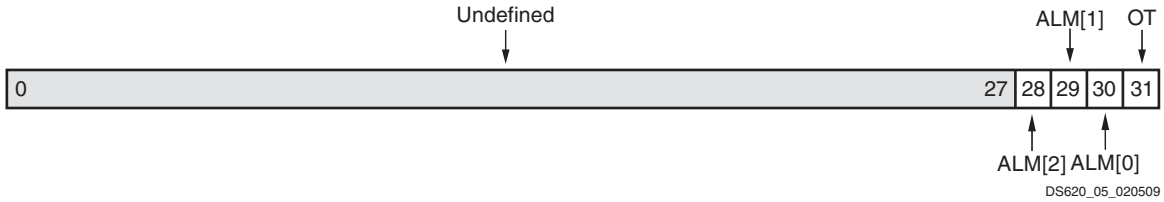


Figure 5: Alarm Output Status Register

Table 7: Alarm Output Status Register (C_BASEADDR + 0x08)

Bit(s)	Name	Core Access	Reset Value	Description
0 - 27	Undefined	N/A	N/A	Undefined
28	ALM[2]	Read	'0'	System Monitor VCCAUX-sensor Interrupt. System Monitor VCCAUX-sensor alarm output interrupt occurs when VCCAUX exceeds user-defined threshold.
29	ALM[1]	Read	'0'	System Monitor VCCINT-sensor Interrupt. System Monitor VCCINT-sensor alarm output interrupt occurs when VCCINT exceeds user-defined threshold.
30	ALM[0]	Read	'0'	System Monitor temperature-sensor Interrupt. System Monitor temperature-sensor alarm output interrupt occurs when device temperature exceeds user-defined threshold.
31	OT	Read	'0'	Over-Temperature alarm Interrupt. Over-Temperature alarm output interrupt occurs when the die temperature exceeds a factory set limit of 125 degree celsius.

CONVST Register (CONVSTR)

The CONVST Register is used for initiating a new conversion in the event-driven sampling mode. The output of this register is logically ORed with an external CONVST input signal. The attempt to read this register results in undefined data. The CONVST Register bit definitions are shown in Figure 6 and explained in Table 8.

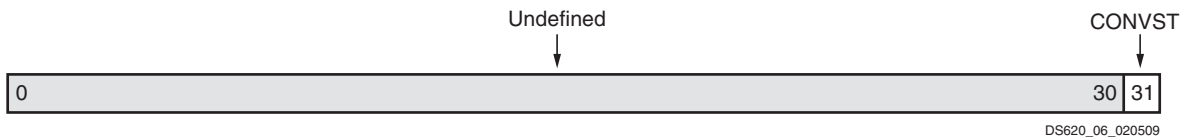


Figure 6: CONVST Register

Table 8: CONVST Register (C_BASEADDR + 0x0C)

Bit(s)	Name	Core Access	Reset Value	Description
0 - 30	Undefined	N/A	N/A	Undefined
31	CONVST	Write	'0'	A rising edge on the CONVST input initiates start of ADC conversion in event-driven sampling mode. For selected channel the CONVST bit in the register needs to be set to '1' and again reset to '0' to start a new conversion cycle. The conversion cycle ends with EOC bit going high.

SYSMON Reset Register (SYSMONRR)

The SYSMON Reset Register is used to reset only the SYSMON hard macro. As soon as the reset is released, the ADC begins with a new conversion. If sequencing is enabled, this conversion is the first in the sequence. This register resets the OT and ALM[n] output from the SYSMON hard macro. This register does not reset the interrupt registers if they are included in the design. Also any reset from the FPGA logic does not affect the RFI (Register File Interface) contents of the SYSMON hard macro. The attempt to read this register results in undefined data. The SYSMON Reset Register bit definitions are shown in Figure 7 and explained in Table 9.

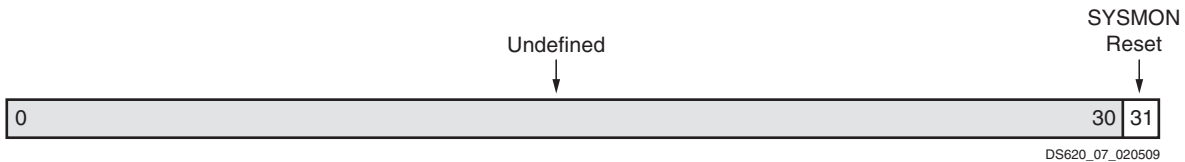


Figure 7: SYSMON Reset Register

Table 9: SYSMON Reset Register (C_BASEADDR + 0x10)

Bit(s)	Name	Core Access	Reset Value	Description
0 - 30	Undefined	N/A	N/A	Undefined.
31	SYSMON Reset	Write	'0'	Writing '1' to this bit position resets the SYSMON hard macro. The reset is released only after '0' is written to this register.

XPS SYSMON ADC Interrupt Controller Register Grouping

The Interrupt Controller Module is included in XPS SYSMON ADC IP core design when C_INCLUDE_INTR = '1'. The XPS SYSMON ADC has a number of distinct interrupts that are sent to the Interrupt Controller Module which is one of the submodules of the XPS SYSMON ADC IP core. The Interrupt Controller Module allows each interrupt to be enabled independently (via the IP interrupt enable register (IPIER)). All the interrupt signals are rising edge sensitive.

The interrupt registers are in the Interrupt Controller Module. The XPS SYSMON ADC IP core permits multiple conditions for an interrupt, or an interrupt strobe which occurs only after the completion of a transfer.

Global Interrupt Enable Register (GIER)

The Global Interrupt Enable Register (GIER) is used to globally enable the final interrupt output from the Interrupt Controller as shown in Figure 8 and described in Table 10. This bit is a read/write bit and is cleared upon reset.

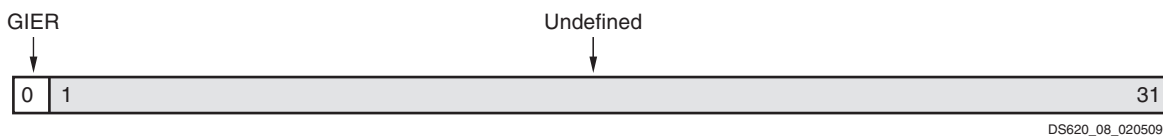


Figure 8: Global Interrupt Enable Register (GIER)

Table 10: Global Interrupt Enable Register (GIER) Description (C_BASEADDR + 0x5C)

Bit(s)	Name	Access	Reset Value	Description
0	GIER	R/W	'0'	Global Interrupt Enable Register. It enables all individually enabled interrupts to be passed to the interrupt controller. '0' = Disabled '1' = Enabled
1 - 31	Undefined	N/A	N/A	Undefined.

IP Interrupt Status Register (IPISR)

Six unique interrupt conditions are possible in the XPS SYSMON ADC IP core.

The Interrupt Controller has a register that can enable each interrupt independently. Bit assignment in the Interrupt register for a 32-bit data bus is shown in Figure 9 and described in Table 11. The interrupt register is a read/toggle on write register and by writing a '1' to a bit position within the register causes the corresponding bit position in the register to 'toggle'. All register bits are cleared upon reset.

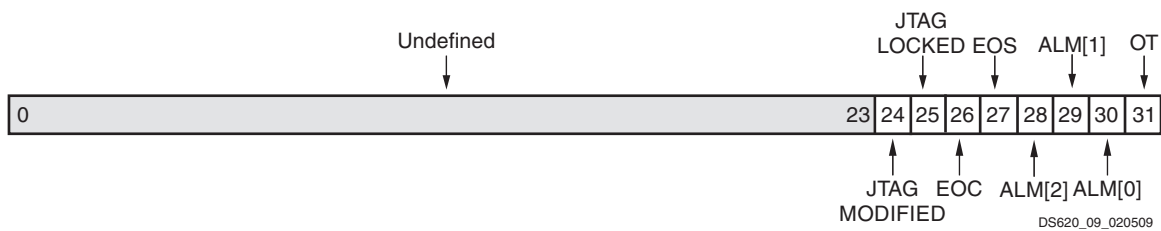


Figure 9: IP Interrupt Status Register (IPISR)

Table 11: IP Interrupt Status Register (IPISR) Description (C_BASEADDR + 0x60)

Bit(s)	Name	Access	Reset Value	Description
0 - 21	Undefined	N/A	N/A	Undefined.
22	ALM[0] Deactive	R/TOW ⁽¹⁾	'0'	ALM[0] Deactive Interrupt. This signal indicates that the falling edge of the ALM[0] (ALM[0] indicates the user temperature range violation) signal is detected. It is cleared by writing '1' to this bit position. Note that the "ALM[0] Deactive" signal is generated locally from the core. This signal indicates that the SYSMON macro has deactivated the user temperature violation signal output.
23	OT Deactive	R/TOW ⁽¹⁾	'0'	OT Deactive Interrupt. This signal indicates that the falling edge of the Over Temperature signal is detected. It is cleared by writing '1' to this bit position. Note that the "OT Deactive" signal is generated locally from the core. This signal indicates that the SYSMON macro has deactivated the Over Temperature signal output.
24	JTAG MODIFIED	R/TOW ⁽¹⁾⁽²⁾	'0'	JTAGMODIFIED Interrupt. This signal indicates that a write to DRP through JTAG interface has occurred. It is cleared by writing '1' to this bit position.
25	JTAG LOCKED	R/TOW ⁽¹⁾⁽²⁾	'0'	JTAGLOCKED Interrupt. This signal is used to indicate that a DRP port lock request has been made by the Joint Test Action Group (JTAG) interface.
26	EOC	R/TOW ⁽¹⁾⁽²⁾	N/A	End of Conversion signal Interrupt. This signal transitions to an active High at the end of an ADC conversion when the measurement is written to the SYSMON hard macro's status register.
27	EOS	R/TOW ⁽¹⁾⁽²⁾	N/A	End of Sequence Interrupt. This signal transitions to an active High when the measurement data from the last channel in the auto sequence is written to the status registers.
28	ALM[2]	R/TOW ⁽¹⁾⁽²⁾	'0'	System Monitor VCCAUX-sensor Interrupt. System Monitor VCCAUX-sensor alarm output interrupt occurs when VCCAUX exceeds user defined threshold.
29	ALM[1]	R/TOW ⁽¹⁾⁽²⁾	'0'	System Monitor VCCINT-sensor Interrupt. System Monitor VCCINT-sensor alarm output interrupt occurs when VCCINT exceeds user defined threshold.
30	ALM[0]	R/TOW ⁽¹⁾⁽²⁾	'0'	System Monitor temperature-sensor Interrupt. System Monitor temperature-sensor alarm output interrupt occurs when device temperature exceeds user defined threshold.
31	OT	R/TOW ⁽¹⁾⁽²⁾	'0'	Over-Temperature alarm Interrupt. Over-Temperature alarm output interrupt occurs when the die temperature exceeds a factory set limit of 125 degree celsius.

Notes:

1. TOW = Toggle On Write. Writing a '1' to a bit position within the register causes the corresponding bit position in the register to toggle.
2. This interrupt signal is directly generated from the SYSMON hard macro.

IP Interrupt Enable Register (IPIER)

The IPIER register has an enable bit for each defined bit of the IPISR register as shown in Figure 10 and described in Table 12. All bits are cleared upon reset.

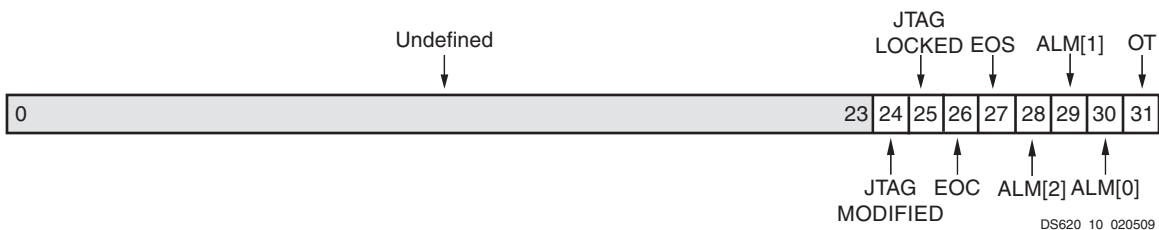


Figure 10: IP Interrupt Enable Register (IPIER)

Table 12: IP Interrupt Enable Register (IPIER) Description (C_BASEADDR + 0x68)

Bit(s)	Name	Access	Reset Value	Description
0 - 21	Undefined	N/A	N/A	Undefined.
22	ALM[0] Deactive	R/W	'0'	ALM[0] Deactive Interrupt '0' = Disabled '1' = Enabled
23	OT Deactive	R/W	'0'	OT Deactive Interrupt '0' = Disabled '1' = Enabled
24	JTAG MODIFIED	R/W	'0'	JTAGMODIFIED Interrupt '0' = Disabled '1' = Enabled
25	JTAG LOCKED	R/W	'0'	JTAGLOCKED Interrupt '0' = Disabled '1' = Enabled
26	EOC	R/W	'0'	End of Conversion signal Interrupt '0' = Disabled '1' = Enabled
27	EOS	R/W	'0'	End of Sequence Interrupt '0' = Disabled '1' = Enabled
28	ALM[2]	R/W	'0'	System Monitor V _{CCAUX} -sensor Interrupt '0' = Disabled '1' = Enabled
29	ALM[1]	R/W	'0'	System Monitor V _{CCINT} -sensor Interrupt '0' = Disabled '1' = Enabled
30	ALM[0]	R/W	'0'	System Monitor temperature-sensor Interrupt '0' = Disabled '1' = Enabled
31	OT	R/W	'0'	Over-Temperature alarm Interrupt '0' = Disabled '1' = Enabled

More about Locally Generated Interrupt Bits in IPIER and IPISR

The interrupt bits ranging from the bit-24 to bit-31 in the IPISR and IPIER registers are direct output signals of the SYSMON hard macro. Signals such as OT Deactive (bit-23) and ALM[0] Deactive (bit-22) are locally generated in the core. These two interrupts are generated on the falling edge of the Over Temperature and AML[0] signals. The falling edge of these two signals can be used to control external functions, such as controlling the fan or air-conditioning of the system. See the Virtex-5 FPGA System Monitor user guide (UG192) for detailed reference about the significance of these interrupts.

SYSMON Hard Macro Register Grouping

The SYSMON hard macro register set consists of all the registers present in the SYSMON hard macro on Virtex-5 and Virtex-6 FPGAs. The addresses of these registers are mentioned in Table 4. Because these registers are 16-bit wide, but the processor data bus is 32-bit wide, the hard macro register data resides on the lower 16 bits of the 32-bit data bus as shown in Figure 11. The 10-bit MSB aligned A/D converted value of different channels from the SYSMON hard macro is left shifted and resides from bit position 16 to 25 of the processor data bus. The remaining bit positions from 26 to 31 should be ignored while considering the ADC data for different channels. Along with 16-bit data, the JTAGMODIFIED and JTAGLOCKED bits are passed, which can be used by the software driver application for determining the validity of the DRP read data. The JTAGMODIFIED bit is cleared when a DRP read/write operation through the FPGA logic is successful. A DRP read/write through the FPGA logic fails, if JTAGLOCKED = '1'. The JTAGLOCKED signal is independently controlled through JTAG TAP. It is expected that these SYSMON hard macro registers should be accessed in their preferred access-mode only. The XPS SYSMON ADC IP core will not be able to differentiate any non-preferred access to the SYSMON hard macro registers. For more information on these registers, see the Reference Documents section.



Figure 11: SYSMON Hard Macro Register

XPS SYSMON ADC Timing Diagrams

Figure 12 shows the write operation and Figure 13 shows the read operation waveform for the XPS SYSMON ADC IP core local registers. Figure 14 shows the write operation and Figure 15 shows the read operation waveform for SYSMON hard macro registers through the XPS SYSMON ADC IP core.

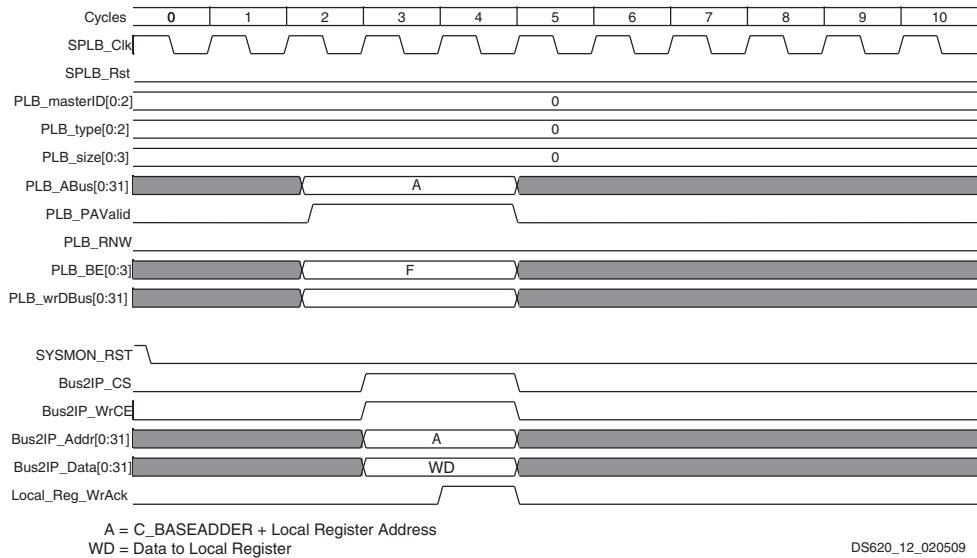


Figure 12: XPS SYSMON ADC IP Core Local Register Write Operation

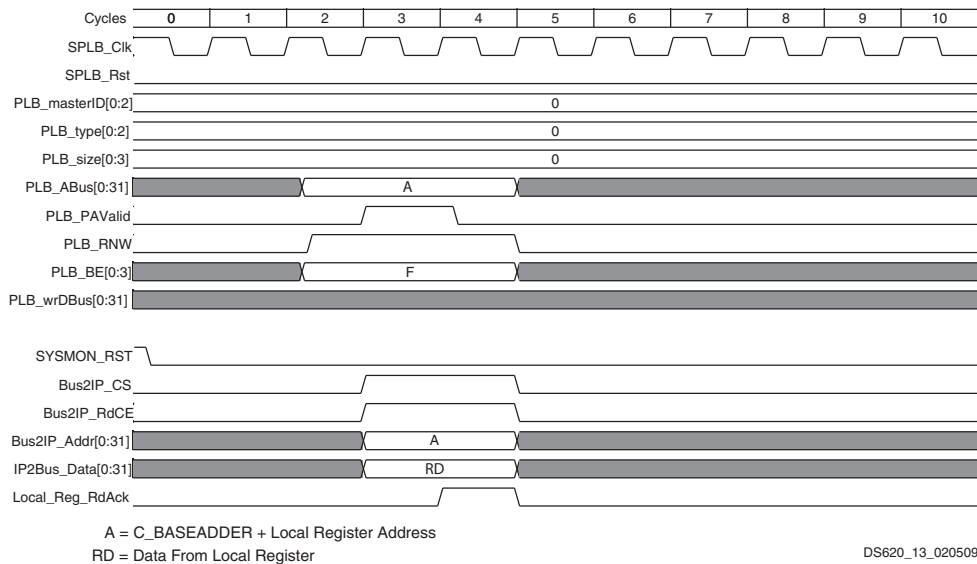


Figure 13: XPS SYSMON ADC IP Core Local Register Read Operation

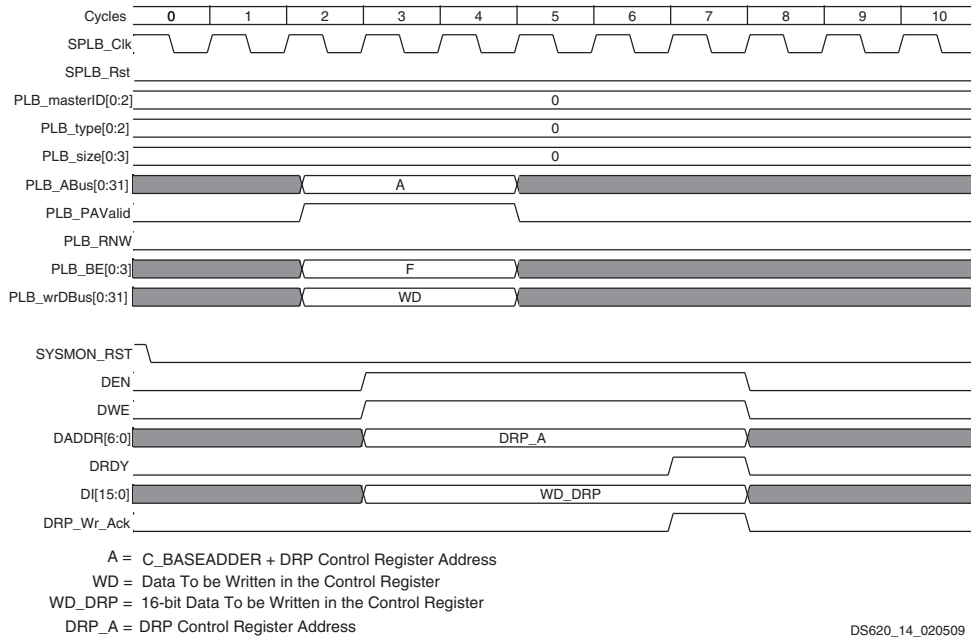


Figure 14: SYSMON Hard Macro Register Write Operation (For Virtex5 Device, C_DCLK_RATIO = 1)

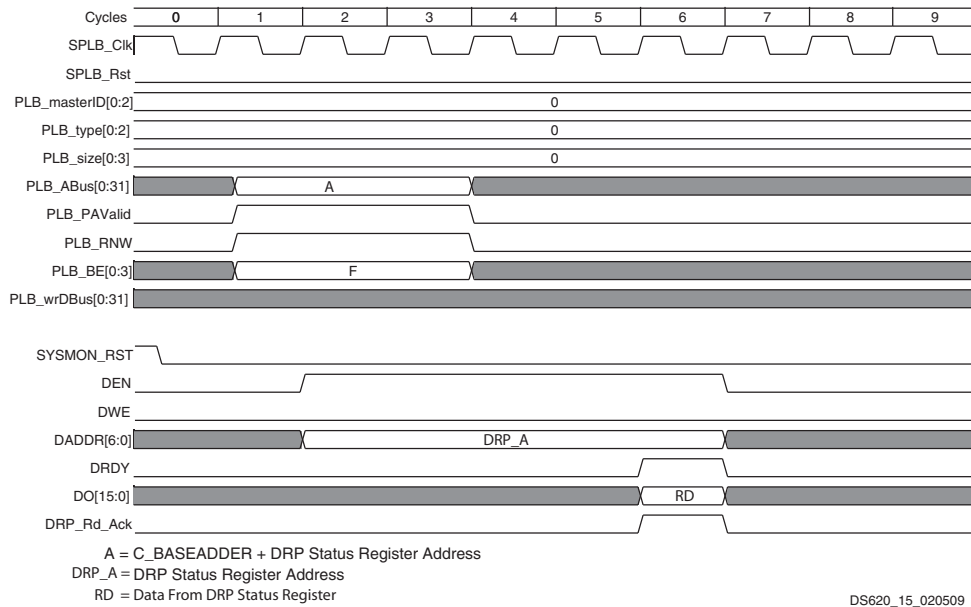


Figure 15: SYSMON Hard Macro Register Read Operation (For Virtex5 Device, C_DCLK_RATIO = 1)

Design Implementation

Target Technology

The intended target technology is Virtex-5 and Virtex-6 FPGAs.

Device Utilization and Performance Benchmarks

Core Performance

Because the XPS SYSMON ADC IP core can be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the XPS SYSMON ADC IP core is combined with other designs in the system, the utilization of FPGA resources and timing of the XPS SYSMON ADC IP core design varies from the results reported here.

The XPS SYSMON ADC IP core resource utilization for various parameter combinations measured with the Virtex-5 FPGA as the target device are detailed in [Table 13](#).

Table 13: Performance and Resource Utilization Benchmarks on the Virtex-5 FPGA (xc5vlx50-ff676-1)

Parameter Values (Other parameters at default values)	Device Resources		Performance
	Slice Flip-Flops	LUTs	F _{Max} (MHz)
C_INCLUDE_INTR			
0	189	114	150
1	251	139	150

Note:

- For utilization calculation, the C_DCLK_RATIO = 1 is used, while the clock was targeted at 150 MHz.

The XPS SYSMON ADC IP core resource utilization for various parameter combinations measured with the Virtex-6 FPGA as the target device are detailed in [Table 14](#).

Table 14: Performance and Resource Utilization Benchmarks on the Virtex-6 FPGA (xc6vlx130t-ff1156-1)

Parameter Values (Other parameters at default values)	Device Resources		Performance
	Slice Flip-Flops	LUTs	F _{Max} (MHz)
C_INCLUDE_INTR			
0	190	149	200
1	252	236	200

Note:

- For utilization calculation, the C_DCLK_RATIO = 3 is used, while the clock was targeted at 200 MHz.

System Performance

To measure the system performance (F_{MAX}) of the XPS SYSMON ADC core, it was added to a Virtex-5 and Virtex-6 FPGA system as the Device Under Test (DUT) as shown in [Figure 16](#).

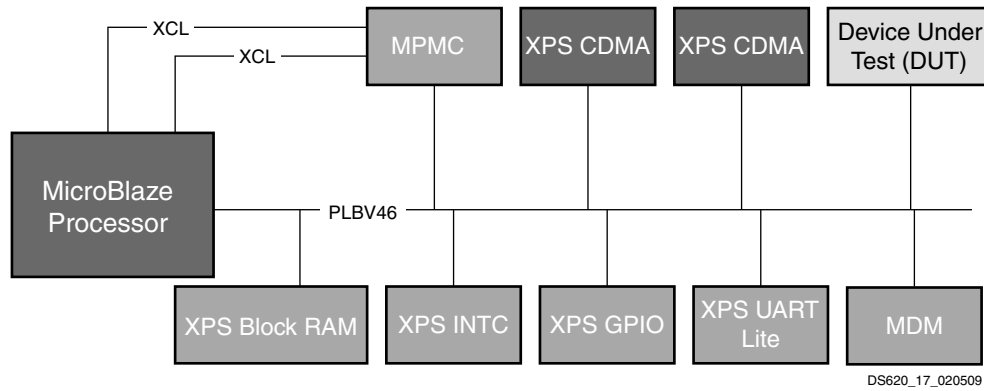


Figure 16: Virtex-5 and Virtex-6 FPGA System with the XPS SYSMON ADC Core as the DUT

The target FPGA was then filled with logic to drive the Lookup Table (LUT) and block Random Access Memory (RAM) utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 15.

Table 15: XPS SYSMON ADC Core System Performance

Target FPGA	Target F_{MAX} (MHz)
V5LXT50 -1	120
V6LXT130-1	150

The target F_{MAX} is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Precautions to be taken while Assigning the C_DCLK_RATIO Parameter

The C_DCLK_RATIO parameter has a range from 1 to 8. It is the user’s responsibility to set a particular value for this parameter. The value set for this parameter divides the clock and the output of this division is provided to the DCLK input of the SYSMON hard macro. This clock is provided through regional clocking nets. It is recommended that the DCLK clock should be always set to 80 MHz with respect to the clock input to the core as well as the proper C_DCLK_RATIO parameter. The user can set a different value for C_DCLK_RATIO, based upon the requirements. If the DCLK clock is very slow, then the SYSMON can take a longer time for conversion of any input including the on-chip parameter and Over Temperature (OT). In such cases, the alarm interrupt for on-chip parameters or Over Temperature (OT) can come early than the actual EOC signal. User should take this into account while writing the application. Also there is no timeout counter involved in the core. So if the DCLK is operating at a very slow speed, then the transactions from the interface may be in wait mode, until the core generates an acknowledge signal for the current transaction. This can affect the overall system performance.

User Application Examples

This section provides examples on configuring XPS SYSMON ADC IP core in either continuous cycling of sequence or single channel (continuous or event driven) mode. It is assumed that the user is aware with the XPS SYSMON ADC IP core register description given in Table 4, page 9.

Continuous Cycling Of Sequence Mode Example

To configure the XPS SYSMON ADC IP core in the Continuous Cycling of Sequence Mode, the SEQ1 and SEQ0 bits in the Configuration Register 1 should be set to '1' and '0', respectively. The specific value written to registers can vary depending upon the need of the application. Following is the configuration example for monitoring the On-Chip Temperature channels, V_{CCINT} and V_{CCAUX} , in a continuous cycling of sequence mode with the clock ratio set to 32.

1. Issue a software reset by writing the data word 0x0000_000A to the SRR. This asserts the reset of the XPS SYSMON ADC IP core for 16 clock cycles.
2. Write 0x0000_0000 to Configuration register 0. This configures the SYSMON hard macro in continuous sampling mode.
3. Write 0x0000_2000 to Configuration register 1. This configures the SYSMON hard macro in continuous cycling of sequence mode, all calibration disabled and all alarm outputs enabled.
4. Write 0x0000_2000 to Configuration Register 2. This configures the SYSMON hard macro to have $ADCCLK = DCLK/32$.
5. Read Status Register (SR) to reset EOC/EOS signal set by any previous conversions.
6. If an interrupt controller is present, then read IPISR to know the value set by any previous conversions. Assume for this application the value read is 0x0000_003E.
7. Write 0x0000_003E to IPISR to toggle the bits which are '1' so that the new value of IPISR becomes 0x0000_0000.
8. If interrupt controller is present, that is, $C_INCLUDE_INTR = 1$, do global enabling of interrupts by writing 0x8000_0000 to GIER.
9. Enable the operational interrupts by writing 0x0000_00FF to the IPIER.
10. Write 0x0000_0700 to Sequence Register 0 and 0x0000_0000 to Sequence Register 1. This configures SYSMON hard macro for monitoring On-Chip Temperature, V_{CCINT} and V_{CCAUX} channel.
11. Write 0x0000_0000 to Sequence Register 2 and 3. This disables ADC channel averaging.
12. Write 0x0000_0000 to Sequence Register 4 and 5. This configures ADC channel in unipolar input mode.
13. Write 0x0000_0000 to Sequence Register 6 and 7. This configures ADC channel acquisition time to four $ADCCLK$ cycles.
14. Write 0x0000_A900 to Alarm Register 0. This configures the upper limit for temperature alarm, which for this application is set to 60° C.
15. Write 0x0000_9980 to Alarm Register 1. This configures the upper limit for V_{CCINT} alarm, which for this application is set to 1.8 V.
16. Write 0x0000_EE80 to Alarm Register 2. This configures the upper limit for V_{CCAUX} alarm, which for this application is set to 2.8 V.
17. Write 0x0000_A000 to Alarm Register 4. This configures the lower limit for temperature alarm, which for this application is set to 42° C.
18. Write 0x0000_4400 to Alarm Register 5. This configures the lower limit for V_{CCINT} alarm, which for this application is set to 0.8 V.
19. Write 0x0000_9980 to Alarm Register 6. This configures the lower limit for V_{CCAUX} alarm, which for this application is set to 1.8 V.
20. Write 0x0000_A180 to Alarm Register 7. This configures the lower limit for OT alarm, which for this application is set to 45° C.
21. The Alarm Register 3 is active only in case of Virtex-6 device. When the Virtex-6 FPGA is targeted then this register is used to set the upper limit of OT. The OT upper is 12 bit register, with lower 4 bits needs to be set to "0011". If this register is left un-initialized, then 125° C is considered as the default upper temperature for OT.

22. Write 0x0000_2000 to Configuration Register 1. This configures the SYSMON hard macro in continuous cycling of sequence mode, all calibration disabled and all alarm outputs enabled. We need to perform a write operation on this register to enable the sequence written to sequence registers. [See the System Monitor User Guide for bits of Configuration Register 0, when targeted for Virtex-5 and Virtex-6 devices]
23. Read SR, if the present conversion cycle is completed then EOS bit in SR is set to '1'. If the interrupt controller is present then the EOS bit in IPISR is also set to '1'.
24. Read converted value of On-Chip Temperature, V_{CCINT} and V_{CCAUX} channel from address C_BASEADDR + 0x200, C_BASEADDR + 0x204 and C_BASEADDR + 0x208 respectively.

Single Channel Mode Examples

To configure the XPS SYSMON ADC IP core in Single Channel Mode, both the SEQ1 and SEQ0 bits in the Configuration register 1 should be set to '1'. The Single Channel Operation can be programmed to operate either in Event-Driven Sampling Mode or Continuous Sampling Mode by setting the $\overline{E\bar{C}}$ bit in Configuration Register 0 to '1' or '0'.

Single Channel Event-Driven Sampling Mode Example

To configure the XPS SYSMON ADC IP core in Single Channel Event-Driven Sampling Mode, $\overline{E\bar{C}}$ bit in Configuration Register 0 should be set to '1'. The specific value written to registers can vary depending upon the need of the application. Also if On-Chip temperature or voltages are monitored, then the Alarm registers should be configured with the appropriate values before writing to the Configuration Registers. Following is the configuration example for monitoring the V_P/V_N channel with the clock ratio set to 32.

1. Issue a software reset by writing the data word 0x0000_000A to the SRR. This asserts the reset of the XPS SYSMON ADC IP core for 16 clock cycles.
2. If interrupt controller is present, for example, C_INCLUDE_INTR = 1, perform the global enabling of interrupts by writing 0x8000_0000 to the GIER register.
3. Enable the operational interrupts by writing 0x0000_00FF to the IPIER register.
4. Write 0x0000_0203 to Configuration register 0. This configures the SYSMON hard macro with no averaging, unipolar mode, event-driven sampling, and selects channel 3 (V_P/V_N) for conversion.
5. Write 0x0000_3000 to Configuration register 1. This configures the SYSMON hard macro in single channel mode, all calibration disabled and all alarm outputs enabled.
6. Write 0x0000_2000 to Configuration register 2. This configures the SYSMON hard macro to have ADCCLK = DCLK/32.
7. Read the Status Register (SR) to reset the EOC/EOS signal which has been set by any previous conversions.
8. If interrupt controller is present, read the IPISR register to know the value set by any previous conversions. Assume for this application the value read is 0x0000_003E.
9. Write 0x0000_003E to IPISR to toggle the bits which are '1' so that the new value of IPISR becomes 0x0000_0000.
10. Conversion Start can be signalled by writing 0x0000_0001 to CONVSTR or by making external CONVST port = '1'.
11. Reset the CONVSTR by writing 0x0000_0000 to it or by making CONVST port = '0' depending upon which kind of trigger (either CONVSTR register or CONVST port) is used for the conversion start.
12. Read SR, if conversion is completed then the EOC bit in SR is set to '1'. If the interrupt controller is present then EOC bit in the IPISR is also set to '1'.
13. Read converted value of channel 3 (V_P/V_N) from address C_BASEADDR + 0x20C.

Single Channel Continuous Sampling Mode Example

To configure the XPS SYSMON ADC IP core in the Single Channel Continuous Sampling Mode, the \overline{EC} bit in Configuration Register 0 should be set to '0'. The specific value written to registers can vary depending upon the need of the application. Also, if On-Chip temperature or voltages are monitored, then the Alarm registers should be configured with appropriate values before writing to Configuration Registers. Following is the configuration example for monitoring V_P/V_N channel with clock ratio set to 32.

1. Issue a software reset by writing the data word 0x0000_000A to the SRR. This asserts the reset of the XPS SYSMON ADC IP core for 16 clock cycles.
2. If interrupt controller is present, that is, $C_INCLUDE_INTR = 1$, do global enabling of interrupts by writing 0x8000_0000 to GIER.
3. Enable the operational interrupts by writing 0x0000_00FF to the IPIER.
4. Write 0x0000_0003 to Configuration Register 0. This configures the SYSMON hard macro with no averaging, unipolar mode, event-driven sampling, and selects channel 3 (V_P/V_N) for conversion.
5. Write 0x0000_3000 to Configuration Register 1. This configures the SYSMON hard macro in single channel mode, all calibration disabled and all alarm outputs enabled.
6. Write 0x0000_2000 to Configuration Register 2. This configures the SYSMON hard macro to have $ADCCLK = DCLK/32$.
7. Write 0x0000_0001 to the SYSMON Reset Register to reset the SYSMON hard macro. This step is required to put the SYSMON hard macro in the reset state.
8. Read Status Register (SR) to reset EOC/EOS signal set by any previous conversions. After reading the Status Register the EOC, EOS from IP core is in reset state.
9. If Interrupt Controller is present, read IPISR to know the value set by any previous conversions. Assume for this application the value read is 0x0000_003E.
10. Write 0x0000_003E to IPISR to toggle the bits which are '1' so that the new value of IPISR becomes 0x0000_0000.
11. Write 0x0000_0000 to the SYSMON Reset Register to bring the SYSMON hard macro out of reset. After the SYSMON hard macro comes out of reset, it starts its normal operation of data acquisition of the configured channels.
12. Read SR, if conversion is completed then the EOC bit in SR is set to '1'. If the interrupt controller is present, the EOC bit in IPISR is also set to '1'.
13. Read converted value of channel 3 (V_P/V_N) from address $C_BASEADDR + 0x20C$.

Reference Documents

To search for Xilinx documentation, go to <http://www.xilinx.com/support>.

1. UG192 Virtex-5 FPGA System Monitor User Guide
2. UG370 Virtex-6 FPGA System Monitor User Guide
3. DS561 PLBV46 Slave Single Product Specification
4. IBM CoreConnect™ 128-Bit Processor Local Bus, Architectural Specification (v4.6)

Support

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List of Acronyms

Table 16: List of Acronyms

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
CDMA	Code-Division Multiple Access
CONVSTR	CONVST Register
DRC	Design Rule Checker
DRP	Dynamic Reconfiguration Port
DUT	Device Under Test
EDK	Embedded Development Kit
EOC	End of Conversion
EOS	End of Sequence
FPGA	Field Programmable Gate Array
GIER	Global Interrupt Enable Register
GPIO	General Purpose Input/Output
I/O	Input/Output
IP	Intellectual Property
IPIER	IP interrupt enable register
IPISR	IP Interrupt Status Register
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
KSPS	Kilo-Samples Per Second
LUT	Lookup Table
MHz	Mega Hertz
MSB	Most Significant Bit
OT	Over Temperature
PLB	Processor Local Bus
RAM	Random Access Memory
RFI	Register File Interface
SR	Status Register
SRR	Software Reset Register

Table 16: List of Acronyms (Cont'd)

Acronym	Description
SYSMON	System Monitor
SYSMONRR	SYSMON Reset Register
TAP	Test Access Port
TOW	Toggle On Write
UART	Universal Asynchronous Receiver Transmitter
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
XPS	Xilinx Platform Studio
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
08/06/07	1.0	Initial Xilinx release
10/1/07	1.2	Added FMax Margin System Performance section.
6/27/08	1.3	Updated the version. Added locally generated interrupt bits information.
6/24/09	1.4	Updated for EDK_L 11.2; created v2.00a; added Virtex-6 support; updated the SYSMON register data base to support newly added registers; updated the utilization table for Virtex-5 and added utilization table for Virtex-6 devices.
12/14/10	1.5	Incorporated CR573247; converted to current data sheet template.
10/19/11	1.6	Summary of core changes <ul style="list-style-type: none"> • Updated for support of 13.3 tools • Updated to core version v3.00.b Summary of documentation changes <ul style="list-style-type: none"> • Updated IP Facts table with new format and information • Updated Notice of Disclaimer and copyright notice • Added List of Acronyms • Removed AXI references • Update Figures 1, 2, and 16

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