

Platform Specification Format Reference Manual

*Embedded Development Kit
EDK*

EDK 10.1, Service Pack 3





© Copyright 2002 – 2008 Xilinx, Inc. All Rights Reserved.

XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

The PowerPC name and logo are registered trademarks of IBM Corp., and used under license. All other trademarks are the property of their respective owners.

Xilinx is disclosing this user guide, manual, release note, and/or specification (the "Documentation") to you solely for use in the development of designs to operate with Xilinx hardware devices. You may not reproduce, distribute, republish, download, display, post, or transmit the Documentation in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Xilinx expressly disclaims any liability arising out of your use of the Documentation. Xilinx reserves the right, at its sole discretion, to change the Documentation without notice at any time. Xilinx assumes no obligation to correct any errors contained in the Documentation, or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. THE DOCUMENTATION IS DISCLOSED TO YOU "**AS-IS**" WITH NO WARRANTY OF ANY KIND. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS. IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION.

Platform Specification Format Reference Manual EDK 10.1, Service Pack 3

The following table shows the revision history for this document.

Date	Revision
08/20/04	Initial release for EDK 6.3i.
02/15/05	EDK 7.1i release.
04/28/05	EDK 7.1i Service Pack 1 release.
07/05/05	EDK 7.1i Service Pack 2 release.
10/24/05	EDK 8.1i release.
01/16/06	EDK 8.1 Service Pack 1 release. Updated to note obsolete cores.
06/23/06	EDK 8.2i release.
01/08/07	EDK 9.1i release.
09/05/07	EDK 9.2i release.
01/14/07	EDK 10.1 release.
09/19/08	EDK 10.1 Service Pack 3 release.

About This Guide

Guide Contents

This manual contains the following chapters:

- Chapter 1, “Introduction”
- Chapter 2, “Microprocessor Hardware Specification (MHS)”
- Chapter 3, “Microprocessor Peripheral Definition (MPD)”
- Chapter 4, “Peripheral Analyze Order (PAO)”
- Chapter 5, “Black-Box Definition (BBD)”
- Chapter 6, “Microprocessor Software Specification (MSS)”
- Chapter 7, “Microprocessor Library Definition (MLD)”
- Chapter 8, “Microprocessor Driver Definition (MDD)”
- Chapter 9, “Xilinx Board Description (XBD) Format”
- Appendix A, “Glossary”

Additional Resources

To find additional documentation, see the Xilinx website:

<http://www.xilinx.com/support/documentation/index.htm>.

The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
EDK Home	Embedded Development Kit home page, FAQ, and tips. http://www.xilinx.com/ise/embedded_design_prod/platform_studio.htm
EDK Examples	A set of complete EDK examples. http://www.xilinx.com/ise/embedded/edk_examples.htm
Tutorials	Tutorials covering Xilinx design flows from design entry to verification and debugging http://www.xilinx.com/support/techsup/tutorials/index.htm

Resource	Description/URL
Answer Browser	To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at: http://www.xilinx.com/support/mysupport.htm
Application Notes	For descriptions of device-specific design techniques and approaches, click the Doc Type tab on the following web page: http://www.xilinx.com/support/documentation/index.htm
Data Sheets	For device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging, click the Doc Type tab on the following web page: http://www.xilinx.com/support/documentation/index.htm
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues: http://www.xilinx.com/support/troubleshoot/psolvers.htm
GNU Manuals	The entire set of GNU manuals may be found at: http://www.gnu.org/manual

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	<code>speed grade: - 100</code>
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu	File → Open
	Keyboard shortcuts	Ctrl+C

Convention	Meaning or Use	Example
<i>Italic font</i>	Variables in a syntax statement for which you must supply values	ngdbuild <i>design_name</i>
	References to other manuals	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more	lowpwr = { on off }
Vertical bar	Separates items in a list of choices	lowpwr = { on off }
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name</i> <i>loc1 loc2 ... locn;</i>

Online Documents

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section " Additional Resources " for details. Refer to " Title Formats " in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Table of Contents

Preface: About This Guide

Guide Contents	5
Additional Resources	5
Conventions	6
Typographical	6
Online Documents	7

Chapter 1: Introduction

Files	15
BBD - Black Box Definition	15
MDD - Microprocessor Driver Definition	15
MHS - Microprocessor Hardware Specification	15
MPD - Microprocessor Peripheral Definition	16
MSS - Microprocessor Software Specification	16
MLD - Microprocessor Library Definition	16
PAO - Peripheral Analyze Order	16
XBD - Xilinx Board Definition	16
File and IP Naming Rules	17
Version Scheme	17
Version Setting for MHS and MSS	17
Version Setting for BBD, MPD, and PAO	17
Load Path	18
Peripheral and pcore Directory Structures	18
Using Versions	19
Creating Your IP	19
Is Your IP Pure HDL?	19
Is Your IP Only a Black-Box Netlist?	19
Is Your IP a Mixture of Black-Box Netlists and VHDL or Verilog?	19
Creating HDL Libraries for Your IP	19
Primary Library	19
Resource Library	20
Resource Libraries and PAO Files	20
Library File Locations	20
Verilog Include Directories	21
Format	21
Restrictions	21

Chapter 2: Microprocessor Hardware Specification (MHS)

MHS Syntax	23
About the Syntax	23
Comments	24
Format	24
MHS Example	25
Bus Interface	27

Definition	27
Example	28
Local Bus Interface	28
Local Bus Interface Keyword(s)	28
Global Parameter	28
Definition	28
Global Parameter Keyword(s)	28
Local Parameter	29
Definition	29
Local Parameter Keyword(s)	29
Global Port	29
Global Port Keyword Summary	29
Global Port Keyword Definitions	29
Local Port	31
Design Considerations	31
Defining Memory Size	31
Power Signals (net_gnd/net_vcc)	32
Unconnected Ports	32
Constant Assignments	32
Concatenation	32
Internal vs. External Signals	33
External Interrupt Signals	33

Chapter 3: Microprocessor Peripheral Definition (MPD)

MPD Syntax	35
Definition	35
Comments	36
Format	36
Assignment Commands	36
Signal Direction	36
MPD Example	37
Bus Interface	39
Definition	39
Bus Interface Keyword Summary	40
Bus Interface Keyword Definitions	40
Bus Interface Naming Conventions	42
IO Interface	42
Definition	42
IO Interface Keywords	43
Option	43
Definition	43
Option Keyword Summary	43
Option Keyword Definitions	44
Parameter	51
Definition	51
Parameter Keyword Summary	51
Parameter Keyword Definitions	51
Parameter Naming Conventions	56
Port	57
Definition	57

Port Keyword Summary	57
Port Keyword Definitions	58
Port Naming Conventions	63
Global Ports	63
Slave DCR Ports	63
Slave LMB Ports	64
Master PLB Ports	64
Slave PLB Ports	65
Reserved Parameters	67
Reserved Parameter Names Summary	67
Reserved Parameter Descriptions	67
Reserved Port Connections	69
Clock and Reset Ports	69
Slave LMB Ports	70
Master PLB Ports	70
Slave PLB Ports	71
Design Considerations	71
Unconnected Ports	71
Scalable Data Path	72
MPD Example	72
Interrupt Signals	72
Tri-state (InOut and Output) Signals	72
Tri-state (InOut) With Single-Bit Enable	74
Tri-state (InOut) With Multi-Bit Enable	74
Tri-state (In/Out) With Single-Bit Enable With Freely Named Ports	75
Tri-state (InOut) With Multi-Bit Enable With Freely Named Ports	75
Tri-state (Output) With Single-Bit Enable	76
Tri-state (Output) With Multi-Bit Enable	76
Tri-state (Output) With Single-Bit Enable With Freely Named Ports	76
Tri-state (Output) With Multi-Bit Enable With Freely Named Ports	77

Chapter 4: Peripheral Analyze Order (PAO)

PAO Format	79
Format	79
Comments	80
Verilog Include Directories	80
Format	80
Restrictions	80
PAO Example	81

Chapter 5: Black-Box Definition (BBD)

BBD Format	83
Comments	83
Lists	83
Common Repository Library	84
BBD Examples	84
File Selection Without Options	84
Multiple File Selections Without Options	84
File Selection With Options	84
File Selection With Common Repository Library	84

Chapter 6: Microprocessor Software Specification (MSS)

Overview	85
Additional Resources	85
TMSS Format	85
MSS Keywords	86
Requirements	86
MSS Example	86
Global Parameters	88
PSF Version	88
Parameter INT_HANDLER	88
Instance-Specific Parameters	88
OS, Driver, Library, and Processor Block Parameters Summary	88
OS, Driver, Library, and Processor Block Parameters Definitions	88
MDD/MLD Specific Parameters	91
OS-Specific Parameters Summary	91
Processor-Specific Parameter Summary	91
Processor-Specific Parameter Definitions	92

Chapter 7: Microprocessor Library Definition (MLD)

Overview	95
Requirements	95
Additional Resources	96
Library Definition Files	96
MLD Format Specification	96
MLD File Format Specification	96
Parameter Description Section	96
Tcl File Format Specification	96
DRC Section	97
Generation Section	97
Examples	97
Example: MLD File for a Library	97
Example: Tcl File of a Library	98
Example: MLD File for an OS	99
Example: Tcl File of an OS	99
MLD Parameter Description Section	100
Conventions	100
Comments	100
OS or Library Definition	100
MLD or MDD Keyword Summary	101
MLD or MDD Keyword Definitions	101
Design Rule Check (DRC) Section	106
Library Generation (Generate) Section	106

Chapter 8: Microprocessor Driver Definition (MDD)

Overview	107
Requirements	107
Additional Resources	108
Driver Definition Files	108

MDD Format Specification	108
MDD File Format Specification	108
Tcl File Format Specification	109
DRC Section	109
Generation Section	109
Example	109
MDD: File Example	109
Example: Tcl File	111
MDD Parameter Description	111
Conventions	111
Comments	111
Driver Definition	112
MDD Keyword Summary	112
MDD Keyword Definitions	112
Design Rule Check (DRC) Section	117
Driver Generation (Generate) Section	117

Chapter 9: Xilinx Board Description (XBD) Format

Overview	119
XBD Syntax	120
Comments in XBD	120
Format	120
Module Definitions	120
Assignment Commands	121
XBD Example	121
Global Attribute Commands	122
Global Attribute Command Summary	122
Global Attribute Command Definitions	122
Local Attribute Commands	123
Local Attribute Command Summary	123
Local Attribute Command Definitions	123
Local Parameter Commands	124
Local Parameter Subproperties	124
Local Port Commands	125
Local Port Subproperties	125
Local Port Subproperty Summary	125
Local Port Subproperty Definitions	126
Associating IPs with IO_INTERFACE in XBD	127
Bridging IP with IO_INTERFACE	129
XBD Load Path	129
BSB Restrictions	130
Existing Xilinx IO Types	131

Appendix A: Glossary

133

Introduction

EDK tools are designed to operate in a data-driven manner. There are various meta-data files that capture information, for example, about various IPs, drivers, and software libraries being used in the EDK tools. Files are also used to capture both hardware and software aspects of your design information. These are ASCII files. The set of all these meta-data formats is referred to as the Platform Specification Format or PSF.

This chapter contains the following sections:

- “Files”
- “File and IP Naming Rules”
- “Load Path”
- “Creating Your IP”
- “Creating HDL Libraries for Your IP”
- “Verilog Include Directories”

Files

BBD - Black Box Definition

The Black Box Definition (BBD) file manages the file locations of optimized hardware netlists for the black-box sections of your peripheral design.

Refer to [Chapter 5, “Black-Box Definition \(BBD\),”](#) for more information.

MDD - Microprocessor Driver Definition

An MDD file contains directives for customizing software drivers.

Refer to [Chapter 8, “Microprocessor Driver Definition \(MDD\),”](#) for more information.

MHS - Microprocessor Hardware Specification

The Microprocessor Hardware Specification (MHS) file defines the hardware component. You supply an MHS file as an input to the Platform Generator (Platgen) tool.

Refer to [Chapter 2, “Microprocessor Hardware Specification \(MHS\),”](#) for more information.

MPD - Microprocessor Peripheral Definition

The Microprocessor Peripheral Definition (MPD) file defines the interface of the peripheral.

Refer to [Chapter 3, “Microprocessor Peripheral Definition \(MPD\),”](#) for more information.

MSS - Microprocessor Software Specification

You supply an MSS file as an input to the Library Generator (Libgen). The MSS file contains directives for customizing libraries, drivers, and file systems.

Refer to [Chapter 6, “Microprocessor Software Specification \(MSS\),”](#) for more information.

MLD - Microprocessor Library Definition

An MLD file contains directives for customizing software libraries and operating systems.

Refer to [Chapter 7, “Microprocessor Library Definition \(MLD\)”](#) for more information.

PAO - Peripheral Analyze Order

A PAO (Peripheral Analyze Order) file contains a list of HDL files that are needed for synthesis and defines the analyze order for compilation.

Refer to [Chapter 4, “Peripheral Analyze Order \(PAO\),”](#) for more information.

XBD - Xilinx Board Definition

An XBD file contains a definition of logical interfaces present on a board and how they are connected to the FPGA. Refer to [Chapter 9, “Xilinx Board Description \(XBD\) Format,”](#) for more information.

File and IP Naming Rules

File and IP names must be all lower-case to ensure consistency across the following:

- OS: UNIX (case-sensitive) vs. Win (case-insensitive)
- HDL: Verilog (case-sensitive) vs. VHDL (case-insensitive)

A lower-case naming convention is used to deal with the above combinations. For example: MYCORE_v2_1_0 and mycore_v2_1_0 would mean two different files in UNIX, whereas in Windows, they would be the same.

Assembly of lower-level cores into the top-level are merged by name reference. Therefore, it is important that names match.

Version Scheme

Form of the version level is X.Y.Z

- X - major revision
- Y - minor revision
- Z - patch level

Version Setting for MHS and MSS

In the body of the MHS and MSS file, add the following statement:

```
PARAMETER VERSION = 2.1.0
```

The version is specified as a literal of the form 2.1.0.

Version Setting for BBD, MPD, and PAO

The version level is concatenated to the base name of the data files. The literal form of the version level is vX_Y_Z.

- *<ipname>*_vX_Y_Z.mpd
- *<ipname>*_vX_Y_Z.bbd
- *<ipname>*_vX_Y_Z.pao
- *<ipname>*_vX_Y_Z.mdd

