

PlanAhead Software Tutorial

I/O Pin Planning

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PlanAhead Software Tutorial

I/O Pin Planning

Introduction

This tutorial introduces the Xilinx® PlanAhead™ software capabilities and benefits when performing I/O pin assignment for FPGA devices. It describes the procedure for creating and assigning I/O ports to physical package pins. The I/O Planner environment provides allows you to create, import, and configure the initial list of I/O ports. You can group the related ports into *Interfaces* and then assign them to package pins.

The capabilities include fully automatic pin placement or semi-automated interactive modes to allow controlled I/O port assignment. The I/O Planner environment shows the relationship of the physical package pins and banks with their corresponding I/O die pads. Intelligent decisions can be made to optimize the connectivity between the PCB and the FGPA device.

I/O Pin Assignment can be performed at various stages of the design cycle. Early package I/O exploration and assignment can be performed with a pin planning project even before the design source files are available. A CSV format file can be imported for I/O planning, or exported for use in PCB schematic symbol or HDL header generation.

PlanAhead also enables I/O pin planning in the elaborated RTL design or in the synthesized Netlist design. PlanAhead is able to perform more comprehensive I/O and clocking DRCs when using the Netlist Design. This tutorial covers both.

Not all commands or command options are covered in this tutorial. This tutorial uses the features contained in PlanAhead, which is bundled as a part of ISE® Design Suite version 12.

Sample Design Data

This tutorial uses the sample design data included with PlanAhead in the following directory:

```
<ISE_install_Dir>/PlanAhead/testcases/PlanAhead_Tutorial.zip
```

Extract the zip file into any write-accessible location. The location of the unzipped PlanAhead_Tutorial data is referred to as the *<Install_Dir>* throughout this document.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original PlanAhead_Tutorial data is required each time you run the tutorial. Refer to the *Tutorial Description* section for more information about the example design.

Xilinx ISE Design Suite and PlanAhead Software

The PlanAhead software is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead software is operational, and that the sample design data is installed. For installation instructions and information, see the *ISE Design Suite 12: Installation, Licensing, and Release Notes* on the Xilinx website:

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_2/irn.pdf

Required Hardware

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead software on larger devices. For this tutorial, a smaller xc6vlx75t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it might impact performance.

PlanAhead Software Documentation and Information

For information about the PlanAhead software, please see the following documents, which are available with your software:

- *PlanAhead User Guide* (UG632) - Provides detailed information about the PlanAhead software. http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_2/PlanAhead_UserGuide.pdf
- *Floorplanning Methodology Guide* (UG633) - Provides floorplanning hints. http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_2/Floorplanning_Methodology_Guide.pdf
- *Hierarchical Design Methodology Guide* (UG748) - Provides an overview of the PlanAhead hierarchical design capabilities. http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_2/Hierarchical_Design_Methodology_Guide.pdf
- For additional information about PlanAhead, including video demonstrations, go to <http://www.xilinx.com/planahead>.

Tutorial Description

The small sample design used in this tutorial includes:

- A RISC processor CPU core
- A pseudo FFT
- Four gigabit transceivers (GTs)
- Two USB interfaces

The design targets an xc6vlx75t device. A small design is used to:

- Allow the tutorial to be run with minimal hardware requirements
- Enable timely completion of the tutorials
- Minimize data size

If you have any questions or comments about the tutorial, contact Xilinx Technical Support.

Tutorial Objectives

The objective of this tutorial is to familiarize you with the I/O pin planning process using the I/O Planner functionality in the PlanAhead software.

Tutorial Procedures

This tutorial is separated into steps, followed by general instructions and supplementary detailed steps allowing you to make choices based on your skill level as you progress through the lab.

If you need help completing a general instruction, go to the detailed steps below it, or if you are ready, simply skip the step-by-step directions and move on to the next general instruction.

This tutorial consists of the following I/O pin planning tasks:

Step 1: Create an empty I/O pin planning project.

Step 2: Examine device I/O resources and the I/O bank die to package relationships

Step 3: Define alternate compatible devices for pin assignment consistency

Step 4: Create and configure I/O ports

Step 5: Import I/O ports

Step 6: Group I/O Ports into interfaces

Step 7: Export the package and I/O pin configuration data

Step 8: Open a Netlist Design and analyze I/O Port placement

Step 9: Clear I/O placement and clock logic constraints

Step 10: Place I/O Ports on physical pins using the various placement modes

Step 11: Place gigabit transceivers (GTs) and clock logic

Step 12: Examine multi-function pins and set device configuration modes

Step 13: Run DRC and SSN analysis to check for legal placement

Step 1: Creating an I/O Pin Planning Project

Step 1

The PlanAhead software provides an I/O pin planning environment called the I/O Planner. Opening the I/O Planner environment loads a PlanAhead software view layout with views more applicable to placing I/O Ports. I/O Planner can be invoked without a design for device resource analysis purposes. It is also available for any open RTL or Netlist Design.

1-1. Create a new project, open the I/O Planner environment, and explore the views.

- 1-1-1. Open the PlanAhead software and create the project_pinout I/O Pin Planning project.
 - On Windows, double-click the Xilinx PlanAhead 12.1 Desktop icon, or select **Start > Programs > Xilinx ISE Design Suite 12.2 > PlanAhead > PlanAhead**.
 - On Linux, go to `<Install_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data` directory and type **PlanAhead**.
- 1-1-2. In the Getting Started page, select **Create a New Project**.
- 1-1-3. Click **Next** to confirm the project creation and to display the Project Name page.
- 1-1-4. Type the Project name, `project_pinout`.
- 1-1-5. Enter the Project location:
`<Install_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data`.

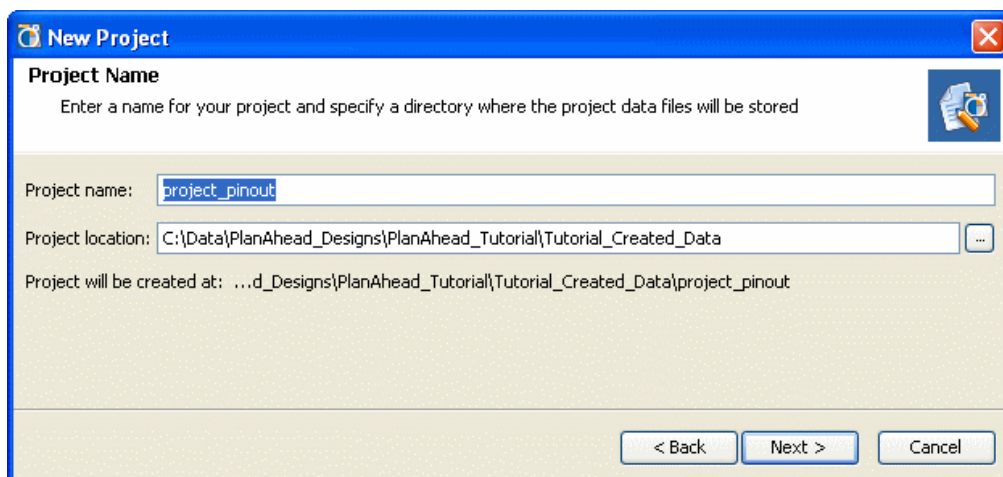


Figure 1: New Project Wizard

- 1-1-6. Click **Next** to open the Design Source page.
- 1-1-7. Select **Create an I/O Planning Project**.

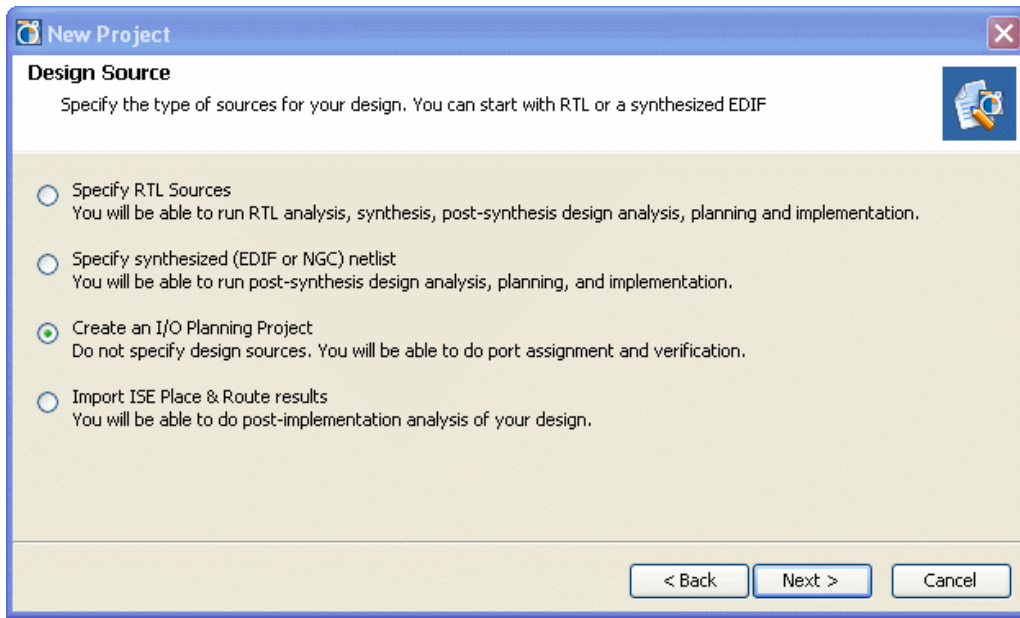


Figure 2: Design Source Page

- 1-1-8. Click **Next** to open the Import Ports page.
- 1-1-9. Select **Do not import I/O ports at this time**.

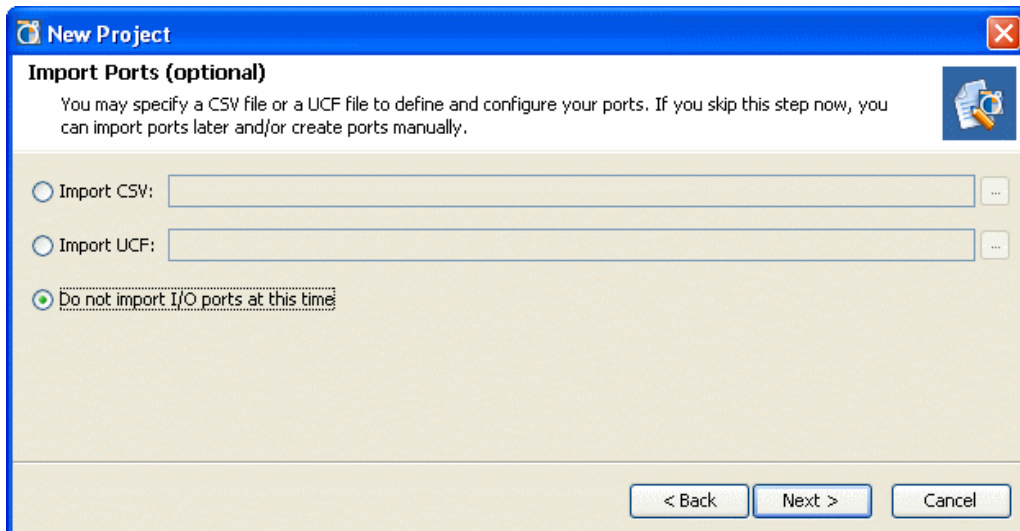


Figure 3: Import Ports Page

- 1-1-10. Click **Next** to open the Default Part Selector page.

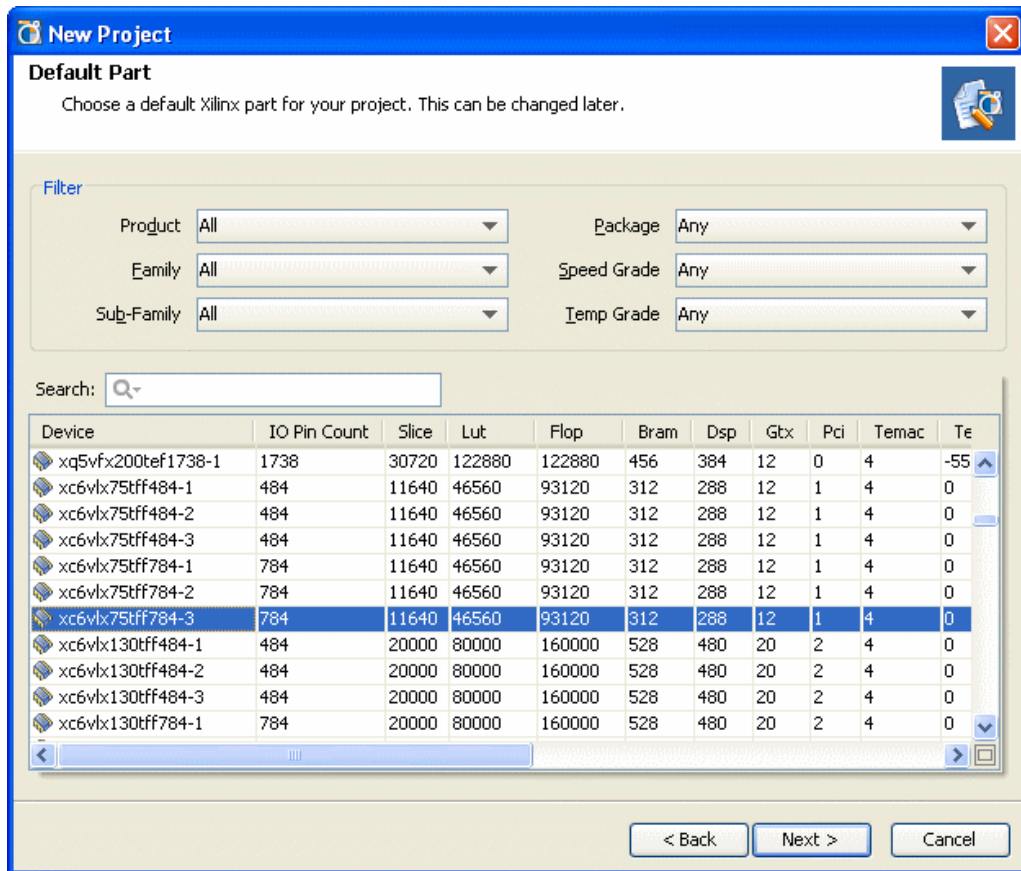


Figure 4: Default Part Selector Page

- 1-1-11. Explore the Device filtering options.
- 1-1-12. Use the Default Part browser to select **xc6vlx75tff784-3**.
- 1-1-13. Click **Next** to open the New Project Summary page.
- 1-1-14. Click **Finish** to create the project as shown in Figure 5.

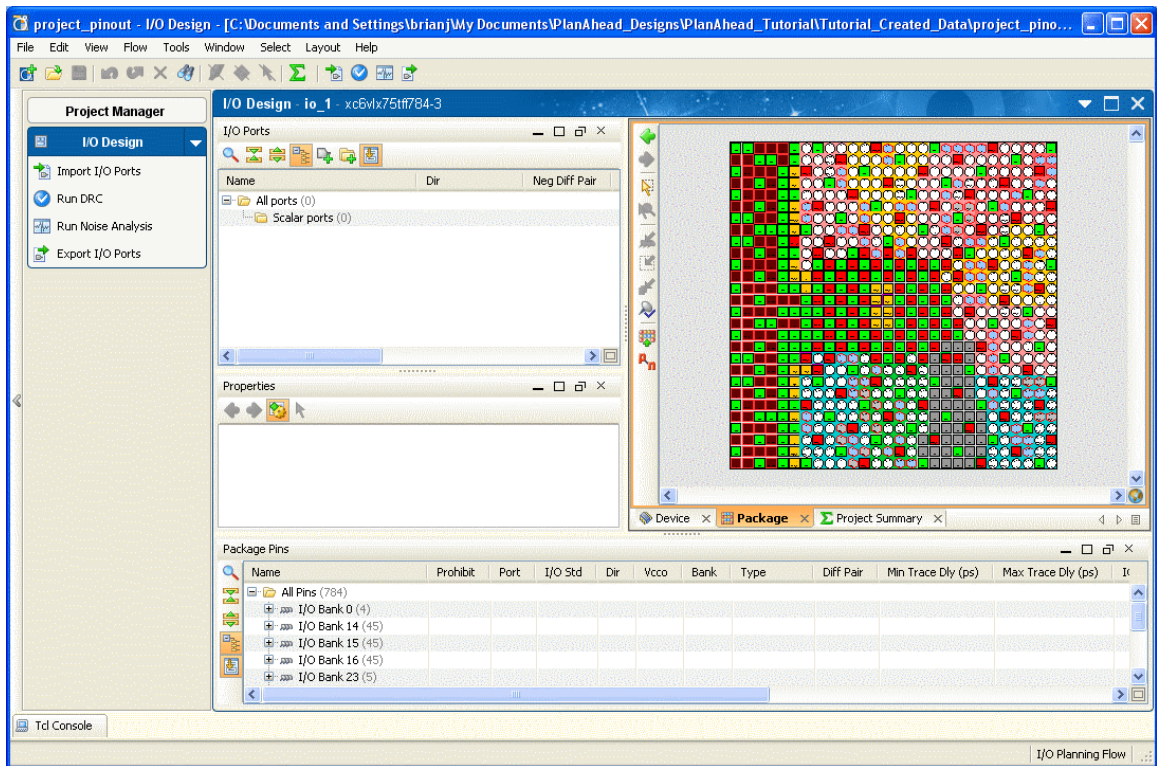


Figure 5: I/O Planner Environment

- 1-1-15.** Explore the various views in the I/O Planner. Many are empty as no I/O Ports have been defined yet.
- 1-1-16.** To maximize the viewing area for the I/O Design, click the **Maximize design view** button.



Figure 6: Maximizing the I/O Design Viewing Area

- 1-1-17.** Click the Restore Design View button to restore the Flow Navigator and Messaging viewing areas. Use Maximize and Restore at your discretion throughout the tutorial.

Step 2: Examining Device I/O Resources

Step 2

The PlanAhead software I/O pin planning environment lets you explore various device resources.

The PlanAhead software views graphically display and cross-select the location of various I/O, clock, and logic objects to help you determine I/O and device-related design decisions. The Package Pins or I/O Bank Properties view provides some I/O related information typically found in the device data sheets.

Next, you will learn how to select several I/O banks to show the package-to-die relationship, how to view I/O bank properties, and how to select and expand the I/O Bank 14 to view package pin specifications.

2-1. Examine I/O Bank properties.

2-1-1. In the Package Pins view, select I/O Bank 14.

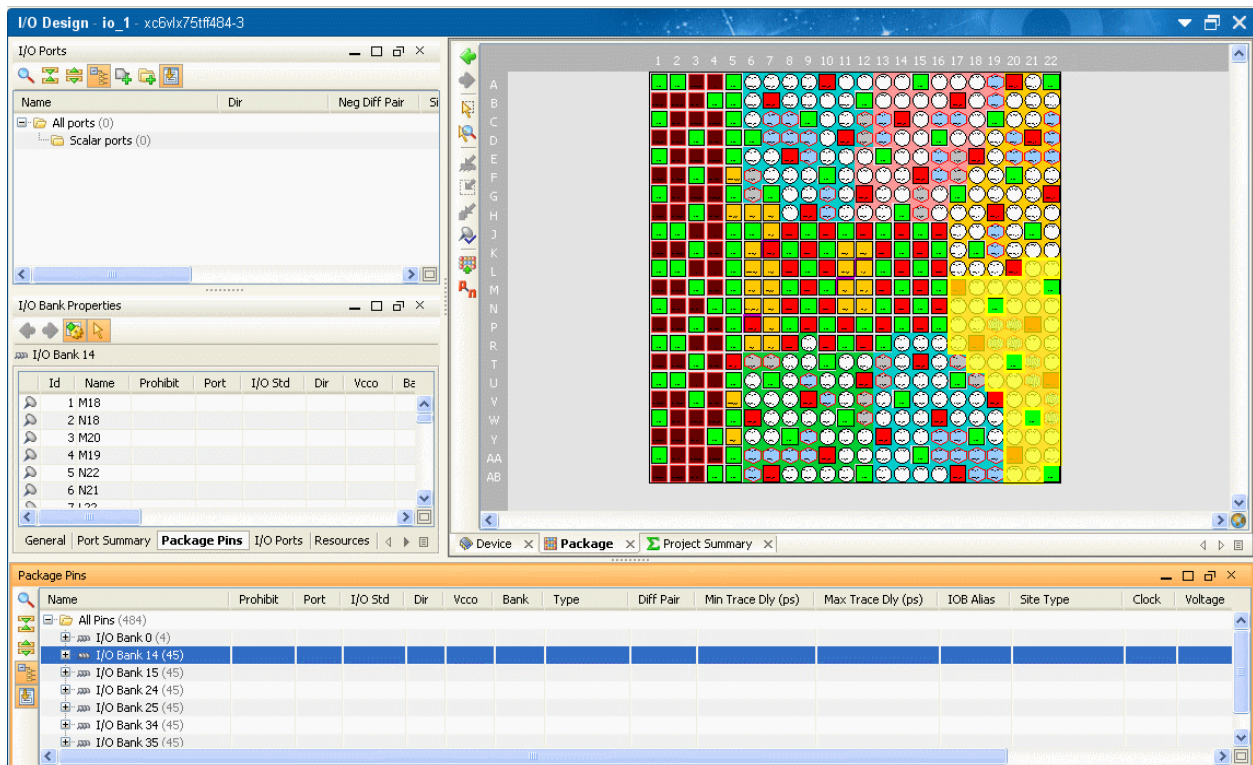


Figure 7: Cross Highlighting I/Os and I/O Banks

The I/O bank location is highlighted in the Package view.

2-1-2. Click the Device view tab in the Workspace to view the I/O bank location on the die.

Being able to visualize the I/O bank locations both internally and externally helps you plan for an optimal I/O port assignment.

2-1-3. Expand I/O Bank 14 in the Package Pins view to view the package pin information for each pin in the I/O Bank. The internal package trace min and max delays are also shown.

- 2-1-4.** Scroll down the list of I/O Banks in the Package Pins view to expand and explore the listed I/O Banks.

The Package Pin view displays the Global Clocks (GC) and regional Clock Capable (CC) pins. As you assign I/O ports more information is provided in this table, such as assigned pin and bank numbers, voltages, and I/O standards.

- 2-1-5.** Select any one of the I/O Banks.
- 2-1-6.** In the I/O Bank Properties view, scroll to view the information displayed for each of the pins in the I/O Bank.
- 2-1-7.** Select the General tab in the I/O Bank Properties view.
- 2-1-8.** Review the I/O count and voltages. This information is populated as I/O Ports are assigned to the I/O bank. This allows you to search for compatible I/O banks to place the remaining I/O Ports.

2-2. Examine the Package Pins View.

You can prohibit I/O package pins from having I/O Ports assigned to them. In the following sequence, you will sort the Package Pins view by Voltage to select all VREF I/O pins, then use the Set Prohibits pop-up command to prohibit placement on those pins.

- 2-2-1.** Select the Package Pins tab and click Maximize. 

The Package Pins view is maximized.

- 2-2-2.** Unselect the Group by I/O Bank button in the Package Pins view to expand and flatten the list.



- 2-2-3.** To reverse sort the list, click the Voltage column header twice and scroll to the top of the list to locate the VREF values.

- 2-2-4.** Select all VREF Voltage pins.

- 2-2-5.** Right-click and select **Set Prohibit**.

- 2-2-6.** In the Package Pins view header, click Restore. 

The Package Pins view is restored. The Package view now displays prohibited pins.

- 2-2-7.** Click Unselect All. 

- 2-2-8.** Zoom in to an area of the Package view to view the Prohibited pins marked with red Xs as shown in the figure below.

To zoom, draw a rectangle in the Package view starting at the upper left of the zoom area and drag to the lower right zoom area.

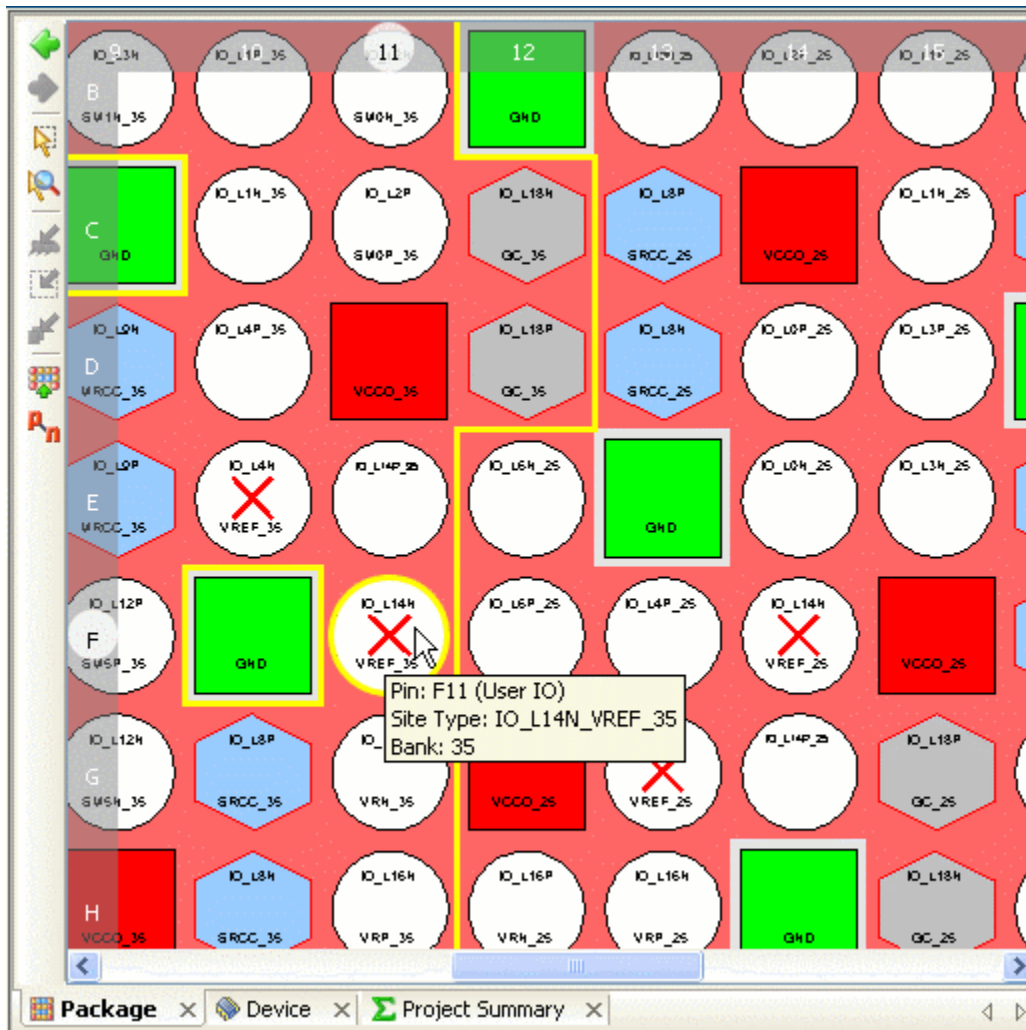


Figure 8: Examine Prohibited VREF Package Pins

2-2-9. Zoom Fit the Package view. Drag from the lower right to the upper left in a diagonal motion.

2-2-10. In the Package Pins view, click Group by I/O Bank .

2-2-11. Click Collapse All  to return the tree table display to the default display structure.

The PlanAhead software has several tree table style views. There are power search and filtering capabilities available in these views. See *Using Tree Table Style Views* in the *Using the Viewing Environment* chapter of the *PlanAhead User Guide* (UG632).

Step 3: Defining Alternate Compatible Devices

Step 3

During the FPGA design process, you might want to change the target device when a design decision dictates a larger or different type. The PlanAhead software lets you define alternate compatible devices up-front so I/O assignments can work across the selected set of devices.

This capability is limited to Virtex[®]-5, Virtex-6 and Spartan[®]-6 devices that use a common package.

3-1. Define alternate devices and place Prohibits on package pins in the selected device.

This step ensures that the I/O pinouts work across the selected set of devices.

- 3-1-1. With the cursor in either the Device or Package view, right-click and select Set Part Compatibility. The Set Part Compatibility opens.

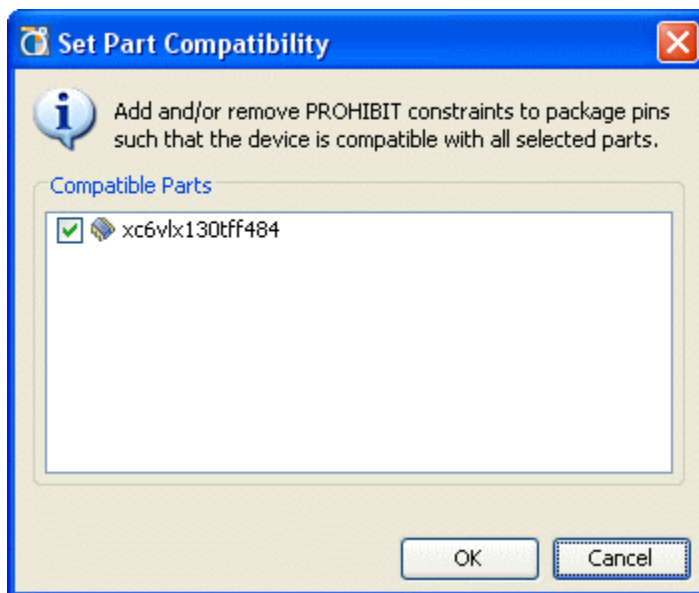


Figure 9: Defining Compatible Parts

- 3-1-2. Select the **xc6vlx130tff784** device.

- 3-1-3. Click **OK**.

The Prohibits are assigned based on the most restrictive parts. Since in this example, you are targeting the smallest device, no prohibits are placed.

- 3-1-4. In the confirmation dialog box, click **OK** to indicate that no Prohibits were placed.

Step 4: Creating and Configuring I/O Ports**Step 4**

I/O Ports can be created and/or configured interactively.

4-1. Create and configure a new I/O bus port called mybus.**4-1-1.** In the I/O Ports view, right-click and select **Create I/O Ports**.

The Create I/O Ports dialog box opens.

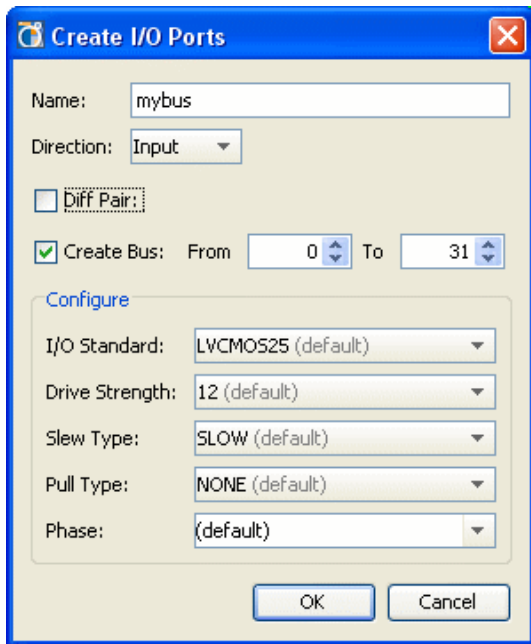


Figure 10: Creating I/O Ports

The Configure I/O Ports right-click menu opens a similar dialog box that enables configuration of existing I/O Ports.

4-1-2. Type `mybus` in the Name field.**4-1-3.** Select **Create Bus**.**4-1-4.** Accept the default dialog box options.**4-1-5.** Click **OK**.

The new I/O Ports display in the I/O Ports view.

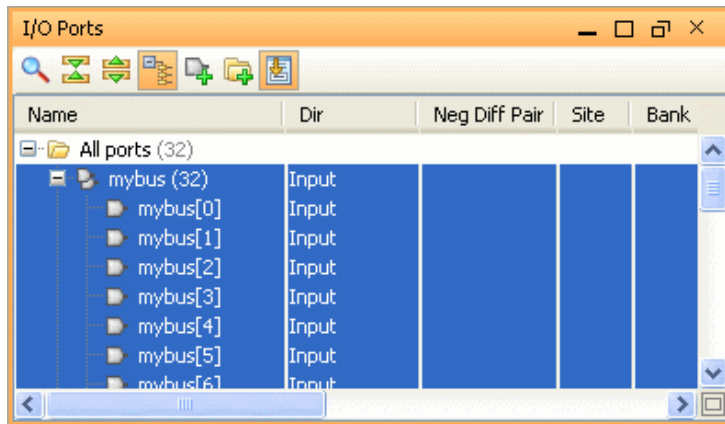


Figure 11: Display Newly Added I/O Ports

4-1-6. Select **Edit > Undo** to remove the recently added `mybus` I/O ports.

Step 5: Importing an I/O Port List

Step 5

The PlanAhead software can import a variety of file formats to begin the I/O pin planning process. Before you have a synthesized netlist, you can import CSV, UCF, or RTL format files to do I/O pin exploration and assignment. You can also create I/O Ports interactively, which is covered in an upcoming step.

Use care with early input methods for I/O pin planning. Without a synthesized netlist, the I/O Ports placement and DRC routines do not take clocks, clock relationships or GT logic into the calculation. When possible, perform I/O pin assignment after importing a synthesized netlist.

5-1. Import and examine the CSV format I/O port list.

5-1-1. In Windows Explorer, open the following I/O Ports list spreadsheet file:

```
<Install_Dir>/PlanAhead_Tutorial/Sources/IO_Ports_import.csv
```

5-1-2. Examine the I/O ports spreadsheet format and content, then exit *without* saving.

5-1-3. In the Flow Navigator on the left side of the PlanAhead software environment, select **I/O Design > Import I/O Ports**.

5-1-4. Select the CSV File browser, and then browse to select:

```
<Install_Dir>/PlanAhead_Tutorial/ Sources/IO_Ports_import.csv
```

The Device and Package views display the assigned Ports and the I/O Ports view is now populated with the imported I/O Ports.

Name	Dir	Neg Diff Pair	Site	Bank	I/O Std
All ports (144)					
DataIn_pad_0_j (8)	Input				LVC MOS25
DataIn_pad_1_j (8)	Input			15	LVC MOS25
DataOut_pad_0_o (8)	Output				LVC MOS25
DataOut_pad_1_o (8)	Output			15	LVC MOS25
LineState_pad_0_j (2)	Input			14	LVC MOS25
LineState_pad_1_j (2)	Input			15	LVC MOS25
OpMode_pad_0_o (2)	Output				LVC MOS25
OpMode_pad_1_o (2)	Output				LVC MOS25

Figure 12: I/O Bus Ports are Grouped by Bus

The buses are grouped together and are expandable.

Most of the remaining steps for I/O pin assignment involve interaction with the I/O Ports view. Unless otherwise specified, all commands in this tutorial should be run with the cursor in the I/O Ports view.

Step 6: Exporting the Device and I/O Pin Assignments

Step 6

The I/O Port assignments can be exported in UCF, CSV, VHDL or Verilog format. This is useful in HDL header and PCB schematic symbol generation.

The CSV format output file also contains package information for all pins and can be used as a seed to begin I/O Port assignment via the spreadsheet.

6-1. Export the I/O Ports list using the Export I/O Ports command.

6-1-1. In the Flow Navigator, select **Export I/O Ports**.

6-1-2. Select **CSV** and **UCF** in the Specify Types to Generate.

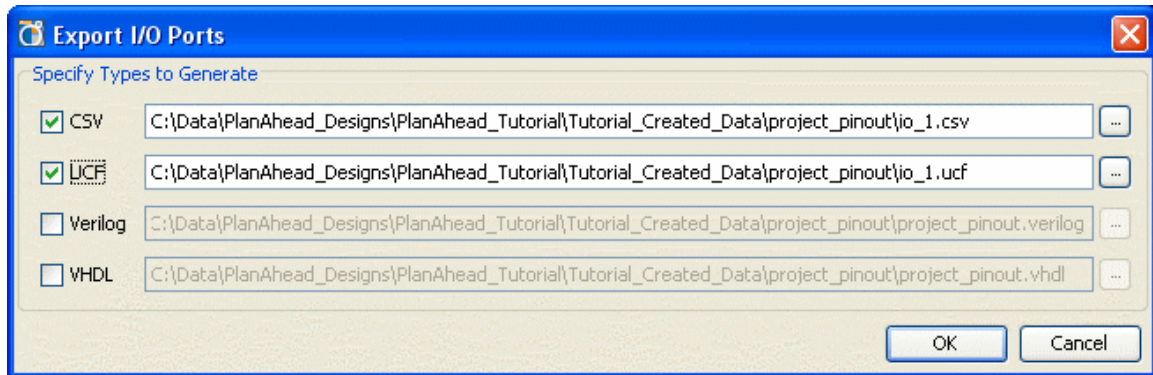


Figure 13: Exporting I/O Ports to a CSV Spreadsheet and UCF File

6-1-3. Click **OK** to accept the default file name and location.

6-1-4. Open a Windows Explorer window and browse to find and open the exported CSV file in:

<Install_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data/project_pinout/io_1.csv

as shown below.

IO Bank	Pin Numb	IOB Alias	Site Type	Min Trace	Max Trace	Prohibit	Interface	Signal Name	Direction	DiffPair T ₁	DiffPair SI	IO Standa	Drive (mA)	Slew Rate	Pull Type
#Top: design_netlist_EMPTY Floorplan: io_1 Part: xc6vx75tff784-3															
#Generated by: brianj on: Mon Jun 21 13:58:49 2010															
#Build: PlanAhead v12.2.MR0 by: hdbuild on: Sun Jun 20 21:53:42 PDT 2010															
6	14 V25	IOB_X0Y32	IO_L3N_14	49.602	57.869			DataIn_pad_0_i[7]	IN			LVCMOS2	12	SLOW	
7	14 W25	IOB_X0Y33	IO_L3P_14	56.874	66.353			DataIn_pad_0_i[6]	IN			LVCMOS2	12	SLOW	
8	14 U28	IOB_X0Y34	IO_L2N_14	57.912	67.564			DataIn_pad_0_i[5]	IN			LVCMOS2	12	SLOW	
9	14 V28	IOB_X0Y35	IO_L2P_14	66.642	77.749			DataIn_pad_0_i[4]	IN			LVCMOS2	12	SLOW	
10	14 U27	IOB_X0Y36	IO_L1N_14	52.968	61.796			DataIn_pad_0_i[3]	IN			LVCMOS2	12	SLOW	
11	14 T27	IOB_X0Y37	IO_L1P_14	51.204	59.738			DataIn_pad_0_i[2]	IN			LVCMOS2	12	SLOW	
12	14 R28	IOB_X0Y38	IO_L0N_14	50.226	58.597			DataIn_pad_0_i[1]	IN			LVCMOS2	12	SLOW	
13	14 R27	IOB_X0Y39	IO_L0P_14	48.678	56.791			DataIn_pad_0_i[0]	IN			LVCMOS2	12	SLOW	
14	14 Y24	IOB_X0Y24	IO_L7N_14	57.264	66.808			DataOut_pad_0_o[7]	OUT			LVCMOS2	12	SLOW	
15	14 Y25	IOB_X0Y25	IO_L7P_14	61.92	72.24			DataOut_pad_0_o[6]	OUT			LVCMOS2	12	SLOW	
16	14 Y27	IOB_X0Y26	IO_L6N_14	70.332	82.054			DataOut_pad_0_o[5]	OUT			LVCMOS2	12	SLOW	
17	14 W27	IOB_X0Y27	IO_L6P_14	65.628	76.566			DataOut_pad_0_o[4]	OUT			LVCMOS2	12	SLOW	
18	14 W28	IOB_X0Y28	IO_L5N_14	65.526	76.447			DataOut_pad_0_o[3]	OUT			LVCMOS2	12	SLOW	
19	14 Y28	IOB_X0Y29	IO_L5P_14	73.074	85.253			DataOut_pad_0_o[2]	OUT			LVCMOS2	12	SLOW	
20	14 V26	IOB_X0Y30	IO_L4N_VREF	48.12	56.14			DataOut_pad_0_o[1]	OUT			LVCMOS2	12	SLOW	
21	14 W26	IOB_X0Y31	IO_L4P_14	56.616	66.052			DataOut_pad_0_o[0]	OUT			LVCMOS2	12	SLOW	
22	14 P22	IOB_X0Y22	IO_L8N_SRCC	12.15	14.175			LineState_pad_0_i[1]	IN			LVCMOS2	12	SLOW	
23	14 P21	IOB_X0Y23	IO_L8P_SRCC	7.236	8.442			LineState_pad_0_i[0]	IN			LVCMOS2	12	SLOW	
24	14 W23	IOB_X0Y20	IO_L9N_MRC	49.152	57.344			OpMode_pad_0_o[1]	OUT			LVCMOS2	12	SLOW	
25	14 Y23	IOB_X0Y21	IO_L9P_MRC	58.05	67.725			OpMode_pad_0_o[0]	OUT			LVCMOS2	12	SLOW	
26	14 T25	IOB_X0Y8	IO_L15N_14	30.744	35.868			VControl_pad_0_o[3]	OUT			LVCMOS2	12	SLOW	
27	14 T24	IOB_X0Y9	IO_L15P_14	29.634	34.573			VControl_pad_0_o[2]	OUT			LVCMOS2	12	SLOW	
28	14 P20	IOB_X0Y10	IO_L14N_VRE	10.77	12.565			VControl_pad_0_o[1]	OUT			LVCMOS2	12	SLOW	
29	14 R20	IOB_X0Y11	IO_L14P_14	5.046	5.887			VControl_pad_0_o[0]	OUT			LVCMOS2	12	SLOW	
30	14 T22	IOB_X0Y0	IO_L19N_14	15.192	17.724			VStatus_pad_0_i[7]	IN			LVCMOS2	12	SLOW	

Figure 14: Examine Exported I/O Ports Spreadsheet

The Interface group names are included in the spreadsheet. Printed circuit board designers can use this spreadsheet to create Interface specific schematic symbols. Creation of I/O Port Interfaces is covered in an upcoming step.

6-1-5. Close the io_1.csv file.

6-1-6. If the Out-of-Date banner appears in the I/O Design view banner, select the Restore Design button.

6-2. Close the I/O Pin Planning Project.

6-2-1. Select **File > Close Project**.

6-2-2. If prompted to save, select **I/O Design – constr_1**.

6-2-3. Click **Save**.

6-2-4. Click **OK** in the Close Project dialog box.

Step 7: Analyzing I/O Port Placement

Step 7

The I/O Planner feature provides several ways to place the I/O Ports onto either package pins or I/O die pads. The automatic placement command tries to place all or the selected group of I/O Ports, adhering to I/O bank rules while grouping buses and Interfaces together.

For more control over I/O Port placement, three semi-automatic placement modes allow interactive dragging of selected I/O Ports into the Package or Device views:

- Place I/O Ports in an I/O Bank
- Place I/O Ports in an Area
- Place I/O Ports Sequentially

I/O Planner also enables interactive DRCs to be toggled on and off during I/O placement.

7-1. Open the Synthesized netlist based Project.

7-1-1. Select the Open Project link in the Getting Started view or select **File > Open Project**.

7-1-2. Browse to select the following Project:

```
<Install_Dir>/PlanAhead_Tutorial/Projects/project_cpu_netlist/project_cpu_netlist.ppr
```

Alternately, select **Open Example Design > CPU (Synthesized)** in the Getting Started view.

7-1-3. In the Sources view, ensure that the `constr_1 Constraint` folder is shown as (active). If not, select it, right-click, and select **Make Active**.

7-1-4. In the Flow Navigator, select **Netlist Design**.

7-1-5. Click **I/O Planner** in the Netlist Design view banner.

The I/O Planner view layout displays.

7-2. Split the Workspace to display the Package and Device view simultaneously.

The PlanAhead software graphical viewing area is called the Workspace. It can be split either horizontally or vertically to display multiple views simultaneously. This allows you to select I/O banks and Interfaces to see the physical package pin and internal die pad locations.

7-2-1. Click and drag the Package view tab to the right edge of the Workspace until the grey rectangle for the view appears as shown below.

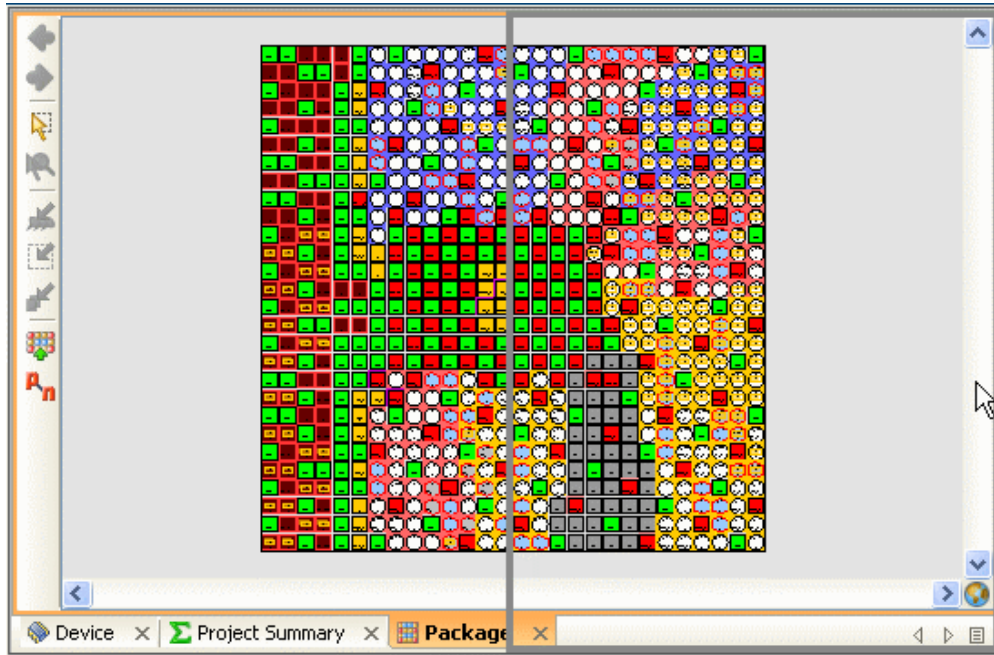


Figure 15: Workspace

- 7-2-2. Drop the view in place.
- 7-2-3. If necessary, click the Device view tab to bring it to the front.
- 7-2-4. Zoom Fit the Package and Device views by clicking in the view and dragging the cursor up and to the left.
- 7-2-5. Adjust the Workspace size if needed.

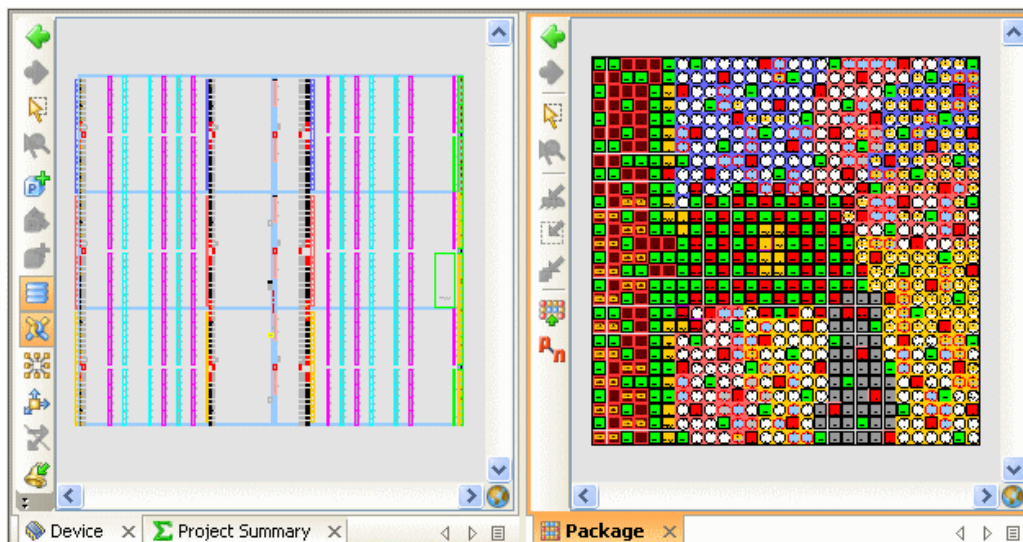




Figure 16: Displaying the Package and Device Views Simultaneously

- 7-2-6. In the I/O Ports view banner, click Maximize View. 
- 7-2-7. Click Expand All  in the I/O Ports view.

7-2-8. Scroll down the list of buses and signals.

The Neg Diff Pair fields are populated for some of the buses indicating they are differential pair buses.

7-2-9. In the I/O Ports view, click Group by Interface and Bus.

The I/O Ports now display as a flat list rather than grouped by bus.

7-2-10. Scroll down the list to display the I/O Standards values applied.

Id	Name	Dir	Interface	Neg Diff Pair	Site	Bank	I/O Std	Drive Strength	Slew Type	Pull Type	Phase
30	DataOut_pad_1_o[5]	Output			E19	15	LVCMOS25	12 SLOW			(default)
31	DataOut_pad_1_o[6]	Output			D19	15	LVCMOS25	12 SLOW			(default)
32	DataOut_pad_1_o[7]	Output			K19	15	LVCMOS25	12 SLOW			(default)
33	GTPRESET_IN	Input			A821	14	LVCMOS25	12 SLOW			(default)
34	LineState_pad_0_i[0]	Input			U21	14	LVCMOS25	12 SLOW			(default)
35	LineState_pad_0_i[1]	Input			T21	14	LVCMOS25	12 SLOW			(default)
36	LineState_pad_1_i[0]	Input			J19	15	LVCMOS25	12 SLOW			(default)
37	LineState_pad_1_i[1]	Input			D20	15	LVCMOS25	12 SLOW			(default)
38	OpMode_pad_0_o[0]	Output			P19	14	LVCMOS25	12 SLOW			(default)
39	OpMode_pad_0_o[1]	Output			P20	14	LVCMOS25	12 SLOW			(default)
40	OpMode_pad_1_o[0]	Output			E20	15	LVCMOS25	12 SLOW			(default)
41	OpMode_pad_1_o[1]	Output			D14	25	LVCMOS25	12 SLOW			(default)
42	RXP_IN[0]	Input		RXN_IN[0]	AB1		LVDS_25				(default)
43	RXP_IN[1]	Input		RXN_IN[1]	AA3		LVDS_25				(default)
44	RXP_IN[2]	Input		RXN_IN[2]	Y1		LVDS_25				(default)
45	RXP_IN[3]	Input		RXN_IN[3]	W3		LVDS_25				(default)
46	RXP_IN[4]	Input		RXN_IN[4]	G3		LVDS_25				(default)
47	RXP_IN[5]	Input		RXN_IN[5]	E3		LVDS_25				(default)
48	RXP_IN[6]	Input		RXN_IN[6]	C3		LVDS_25				(default)
49	RXP_IN[7]	Input		RXN_IN[7]	B1		LVDS_25				(default)
50	RxActive_pad_0_i	Input			T13	24	LVCMOS25	12 SLOW			(default)
51	RxActive_pad_1_i	Input			E14	25	LVCMOS25	12 SLOW			(default)
52	RxError_pad_0_i	Input			U13	24	LVCMOS25	12 SLOW			(default)
53	RxError_pad_1_i	Input			B15	25	LVCMOS25	12 SLOW			(default)
54	RxValid_pad_0_i	Input			T17	24	LVCMOS25	12 SLOW			(default)

Figure 17: Examining I/O Standard and Diff Pair Requirements

The RXP_IN, TXP_OUT, and TILE_REFCLK_PAD* buses are differential pairs and have unique I/O Standards applied.

Step 8: Creating I/O Port Interfaces

Step 8

It is often beneficial to group the I/O Ports associated with various I/O interfaces. The I/O Planner feature enables the definition of groups of pins, buses or other interfaces to be grouped together as an “Interface.” This ability helps with I/O Port management and with generating interface-specific PCB schematic symbols. It also forces the I/O Port automatic placement command to group the entire interface together on the device (where this is possible).

8-1. Create Interfaces for the similar I/O Port groups.

The design used in this tutorial has two USB interfaces, each containing many I/O ports. The I/O port names are differentiated by `_0` and `_1` as shown in the figure above. You will create Interfaces for all signals in USB0 and USB1.

8-1-1. Click Show Search. 

8-1-2. Type `_0` in the Search field.

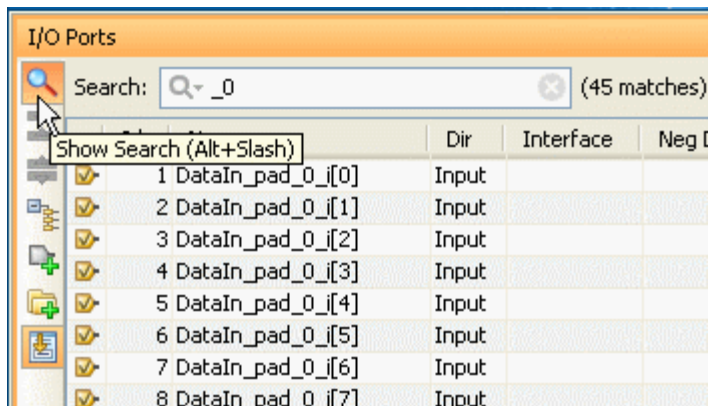


Figure 18: Selecting USB_0 Related Buses

8-1-3. Select one of the ports in the filtered list.

Press **Ctrl+A** to select all ports in the filtered list.

8-1-4. Right-click and select **Create I/O Port Interface**.

The Create I/O Port Interface dialog box opens.

8-1-5. Type `USB0` in the Name field.

8-1-6. Click **OK**.




Figure 19: Create I/O Port Interface

The USB0 folder now appears in the I/O Ports view.

8-1-7. In the Search field, change _0 to _1 and follow the same steps to create a USB1 I/O Port Interface.

8-1-8. Click Show Search  to remove the Search filter.

8-1-9. Click Group by Interface and Bus. 

8-1-10. Click Collapse All .

The I/O ports list is condensed with all of the USB related ports in Interface groups.

8-1-11. Expand the Scalar Ports folder to view the clocks resets and other items.

Name	Dir	Neg Diff Pair	Site	Bank	I/O Std	Drive Strength	Slew Type	Pull Type	Phase
All ports (144)									
USB0 (44)	(Multiple)			(Multiple)	LVC MOS25	12	SLOW		(default)
USB1 (44)	(Multiple)			(Multiple)	LVC MOS25	12	SLOW		(default)
RXP_IN (8)	Input	RXN_IN			LVDS_25				(default)
TXP_OUT (8)	Output	TXN_OUT			LVDS_25				(default)
or1200_pm_out (4)	Output			15	LVC MOS25	12	SLOW		(default)
Scalar ports (20)									
GTPRESET_IN	Input		J25	15	LVC MOS25	12	SLOW		(default)
TILE0_PLLKDET_OUT	Output		H26	15	LVC MOS25	12	SLOW		(default)
TILE0_REFCLK_PAD_P_IN	Input	TILE0_REFCLK_PAD_N_IN	P28	15	LVDS_25				(default)
TILE1_PLLKDET_OUT	Output		H25	15	LVC MOS25	12	SLOW		(default)
TILE1_REFCLK_PAD_P_IN	Input	TILE1_REFCLK_PAD_N_IN	M27	15	LVDS_25				(default)
TILE2_PLLKDET_OUT	Output		K23	15	LVC MOS25	12	SLOW		(default)
TILE2_REFCLK_PAD_P_IN	Input	TILE2_REFCLK_PAD_N_IN	M23	15	LVDS_25				(default)
TILE3_PLLKDET_OUT	Output		K22	15	LVC MOS25	12	SLOW		(default)
TILE3_REFCLK_PAD_P_IN	Input	TILE3_REFCLK_PAD_N_IN	J28	15	LVDS_25				(default)
cpuClk	Input		F20	25	LVC MOS25	12	SLOW		(default)
...

Figure 20: Viewing I/O Port Interface Groups and Scalar Ports

8-1-12. Click Restore View .

The I/O Ports view is restored to the original location.

8-2. Examine the I/O Placement.

8-2-1. In the I/O Ports view, select the USB0 Interface.

The I/O Port locations are highlighted in both Package and Device views. The Ports are grouped in the Package Pins view and enter the die in the lower left side of the Device.

8-2-2. In the I/O Ports view, select the USB1 Interface.

The Ports are grouped in the Package Pins view and enter the die in the upper left side of the Device.

8-2-3. Select the RXP_IN or TXP_OUT buses to observe the GT and GT I/O placement.

8-3. Examine Clock Logic Placement.

8-3-1. Click **Find**. 

8-3-2. Set the Find object type to **Instances** if not set already.

8-3-3. For criteria, select **Type, is, Gigabit IO**.

8-3-4. Click **OK**.

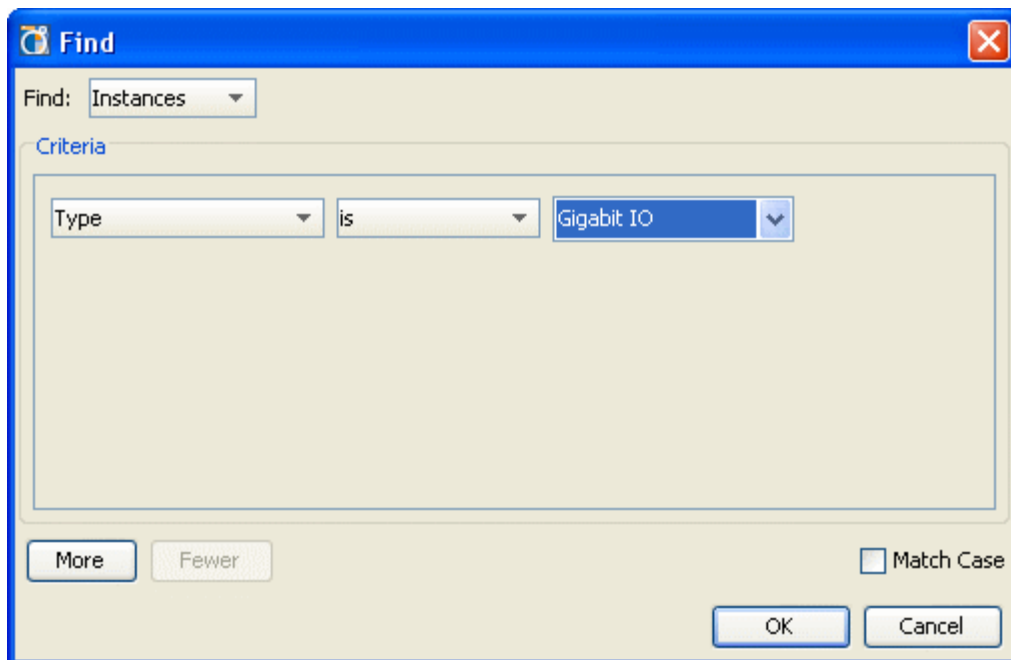


Figure 21: Searching for all Gigabit IO Logic in the Design

The Find Results view is displayed with all Gigabit IOs found in the design.

On the icons next to each clock logic object in the Find Results view, the blue stripe indicates that the logic object is placed and has a LOC constraint assigned.

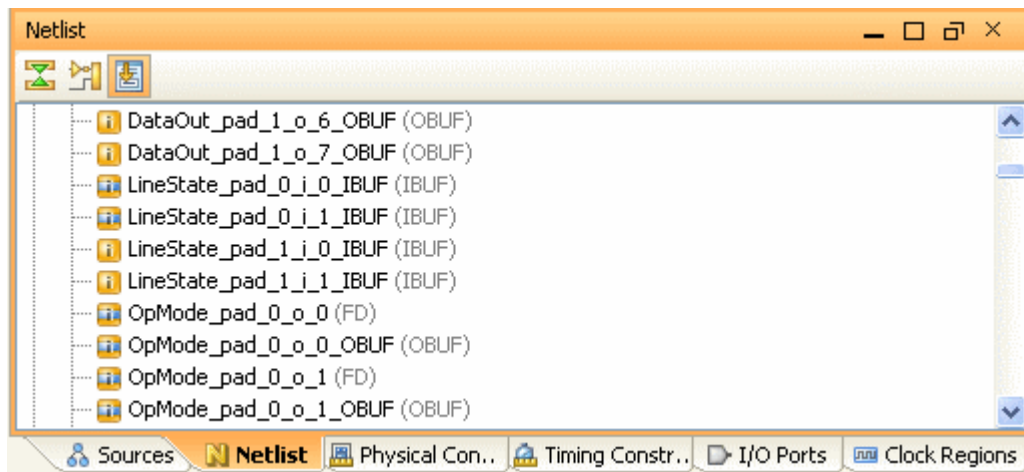


Figure 22: Blue-striped icon indicating Placed LOC

- 8-3-5.** Select one of the placed objects in the list.
The object is highlighted in the Device view.
- 8-3-6.** In the Find Results view, press **Ctrl+A** to select all objects in the view.
All of the Gigabit logic objects are highlighted in the Device view.

Step 9: Clearing Imported I/O Placement Constraints

Step 9

The PlanAhead software has a robust set of options and filters for keeping or removing placement constraints. As I/Os are manually assigned, the placed I/O and clock logic receive “fixed” LOC placement constraints. The PlanAhead software differentiates between user-assigned “fixed” or ISE implementation assigned “unfixed” placement. It is useful to have control of which logic types the LOCs can remove or preserve. All fixed placement will receive LOC constraints in the UCF file exported for ISE implementation.

In order to walk through the steps involved to create the pin assignment, you will first need to clear the existing I/O LOC constraints in this Project.

9-1. Clear imported I/O constraints using the Clear Placement Constraints command.

9-1-1. Click Unselect All. 

9-1-2. Select **Tools > Clear Placement**.

The Clear Placement Constraints wizard opens.

9-1-3. Select **I/O port placement**.

9-1-4. Click **Next**.

The Fixed Placement dialog box opens.

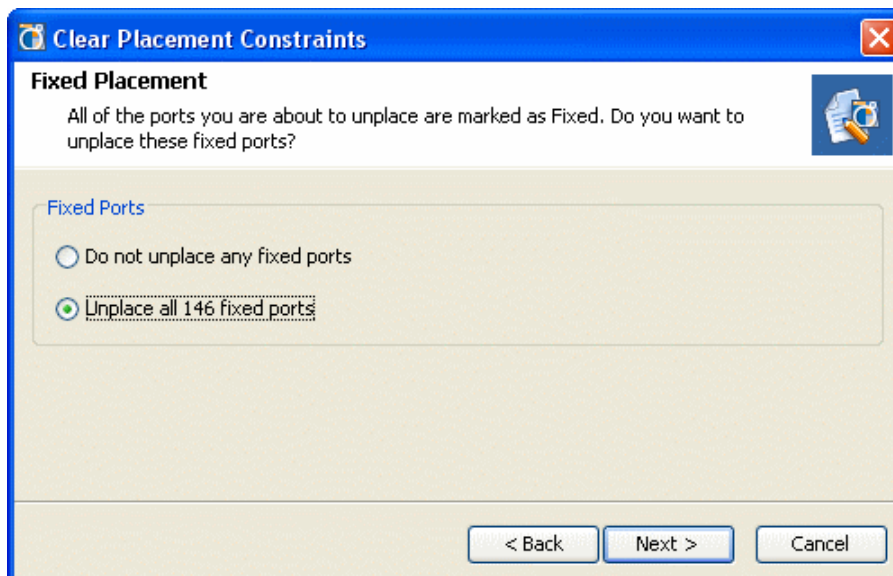


Figure 23: Selecting Fixed Filtering Options

9-1-5. Select **Unplace all 146 fixed ports**.

9-1-6. Click **Next**.

9-1-7. Review the Summary dialog box.


9-1-8. Click **Finish**.

The placement constraints are now removed in the Package view and I/O Ports view.

Step 10: Placing I/O Ports

Step 10

The PlanAhead software provides several ways to place the I/O Ports onto either package pins or I/O die pads. The automatic placement command tries to place all or the selected group of I/O Ports, adhering to I/O bank rules while grouping buses and Interfaces together.

By default, the PlanAhead software uses interactive DRCs during I/O placement. This checking can be disabled by toggling the Automatically Enforce Legal I/O Placement button  in the Device and Package views. It is also available to set in **Tools > Options > General**.

For more control over I/O Port placement, three semi-automatic placement modes allow interactive dragging of selected I/O Ports into the Package or Device views:

- Place I/O Ports in an I/O Bank
- Place I/O Ports in an Area
- Place I/O Ports Sequentially

10-1. Place the USB0 Port Interface using the Place I/O Ports in an I/O Bank placement mode.

10-1-1. Select the USB0 Interface.

10-1-2. In the Package view, click **Place I/O Ports in an I/O Bank**. 

10-1-3. Drag the cursor over the Package view.

As the cursor is dragged over the Package Pins, the assignment pattern displays and the number of pins to be placed is shown in the Tooltip.

The Information bar at the bottom of the PlanAhead software displays information about the objects being dragged over including I/O Banks and Package Pins.

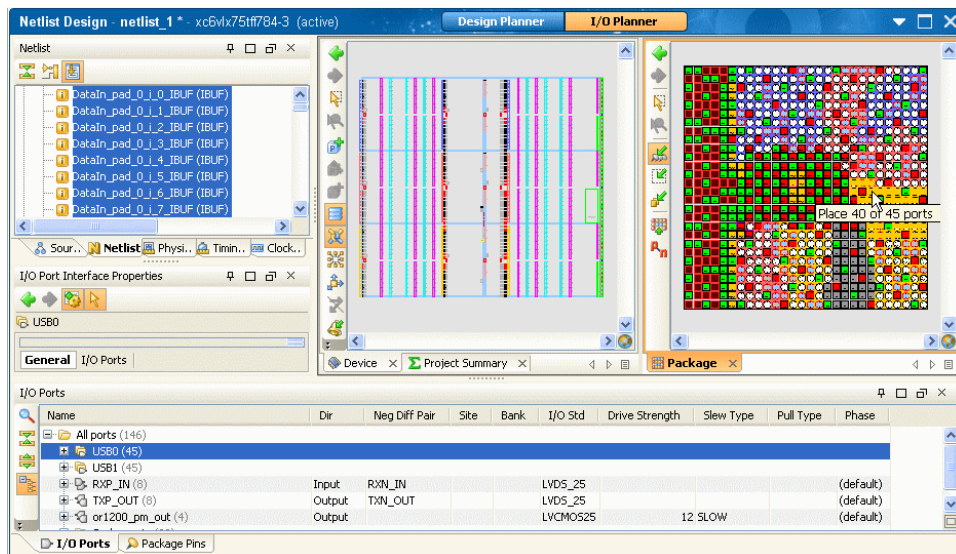


Figure 24: Place I/O Ports in an I/O Bank

10-1-4. Click on **I/O Bank 14** on the right side of the Package to drop the I/O Ports, as shown above.

10-1-5. Select the below adjacent I/O Bank 24 to place the remaining I/O Ports.



Figure 25: Continue to Place I/O Ports in I/O Banks

The I/O Ports are assigned in the order that they appear in the I/O Ports view. Assignment order is vectored out from the initial pin selected.

10-1-6. In the I/O Ports view, click **Collapse All**. 

10-2. Place the USB1 I/O Port Interface using the Place I/O Ports in an Area placement mode.

10-2-1. In the Device view, zoom in to the upper left quadrant of the device.

10-2-2. In the I/O Ports view, select the **USB1 Interface**.

10-2-3. In the Device view, click **Place I/O Ports in an Area**. 

The cursor displays a cross indicating draw rectangle mode.

10-2-4. Draw a rectangle starting above the upper left I/O bank and drag it down and to the right until all I/O Ports are placed in the rectangle within the top clock region.

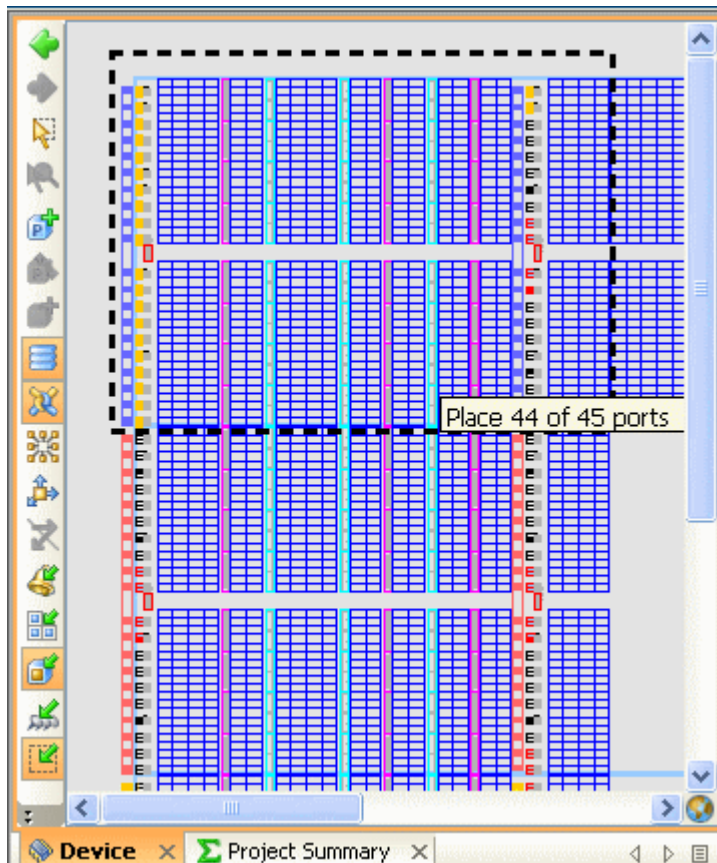



Figure 26: Place USB1 I/O Ports in an Area

There is still one unplaced I/O clock port dragging on the cursor. There is no global clock pad in this area of the device. Rather than trying to find a global clock pad, allow the automatic placement command to place it later.

10-2-5. Press **Esc** to exit the command.

10-3. Place the RXP_IN differential pair bus using the Place I/O Ports Sequentially placement mode.

10-3-1. In the Package view, toggle **Show Differential I/O pairs**. 

10-3-2. Zoom in to an area in the bottom left of the device where you can see the differential pair pins.

10-3-3. Select the RXP_IN bus in the I/O Ports view.

10-3-4. In the Package view, click **Place I/O Ports Sequentially**. 

10-3-5. Drag and click to place the first Diff pair I/O Port into one of the lower I/O Banks on a designated pin.

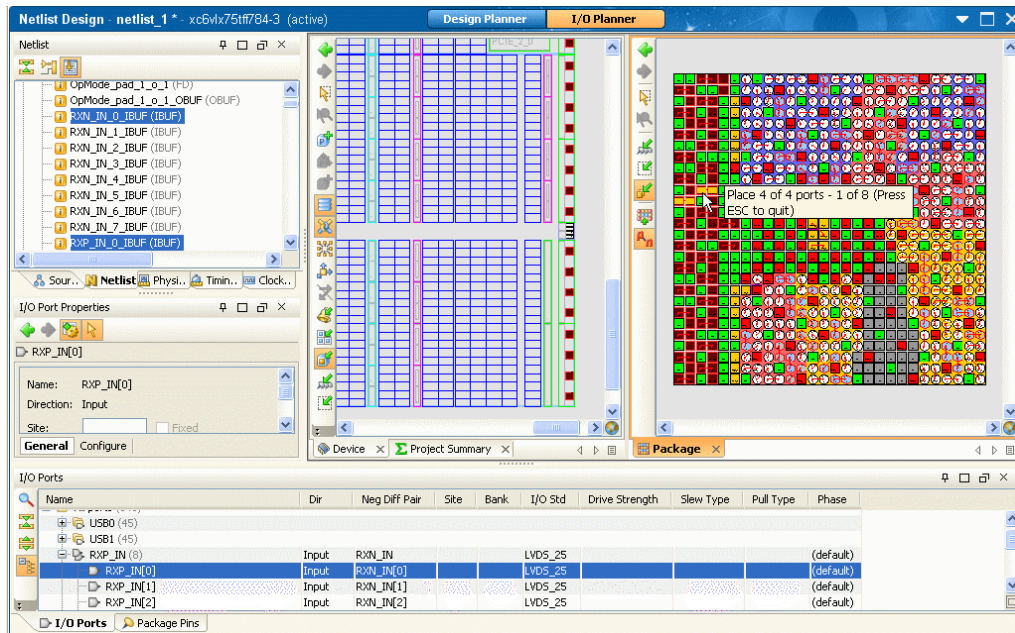


Figure 27: Place Diff Pair I/O Bus Ports Sequentially

Both diff pairs associated with the GTs were placed on legal sites. You might see a Tooltip indicating that the selected site is not legal and giving the reason why it is not legal.

You can manually enter a pin location in the Site field in the I/O Port Properties view.

10-3-6. Select another pin in the Package view to place the next Diff pair I/O bus port.

10-3-7. In the Device view, select the top pin of the bottom GT I/O sites.

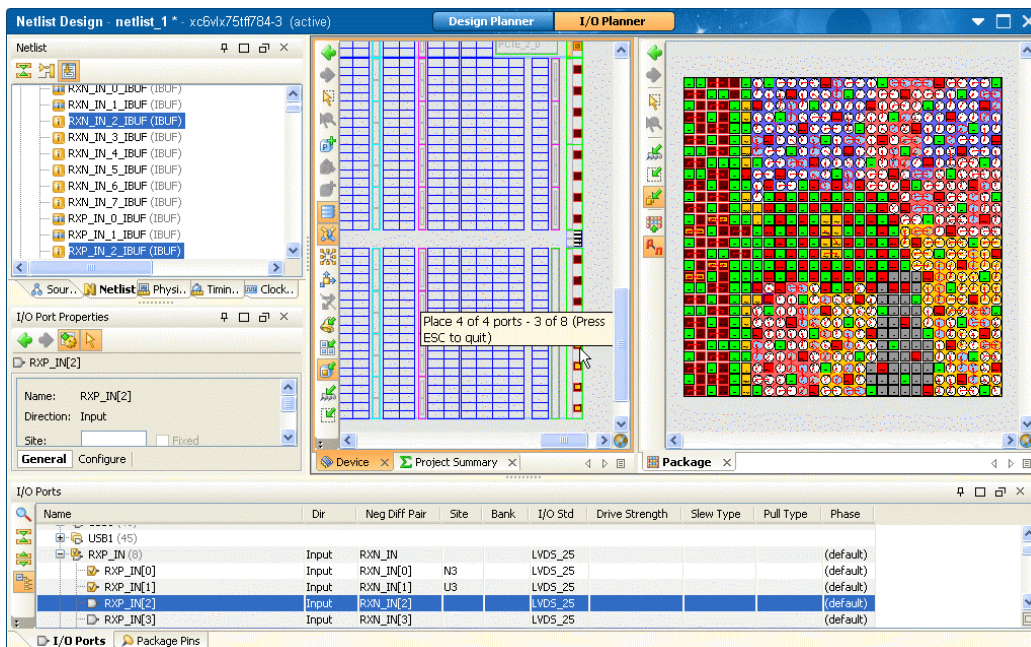


Figure 28: Place GT related I/Os Sequentially in the Device View

10-3-8. Press **Esc** to exit the command.

You will place the GTs and their related I/Os in the next step.

10-3-9. In the Package view, toggle **Show Differential I/O pairs**. 

10-3-10. Zoom Fit the Package and Device views.

10-4. Automatically place the remaining I/O Ports.

10-4-1. If active, click Unselect All. 

10-4-2. Run **Tools > Autoplace I/O Ports**.

10-4-3. In the Autoplace I/O Ports dialog box, click **Next**.

The Placed I/O Ports dialog box opens.

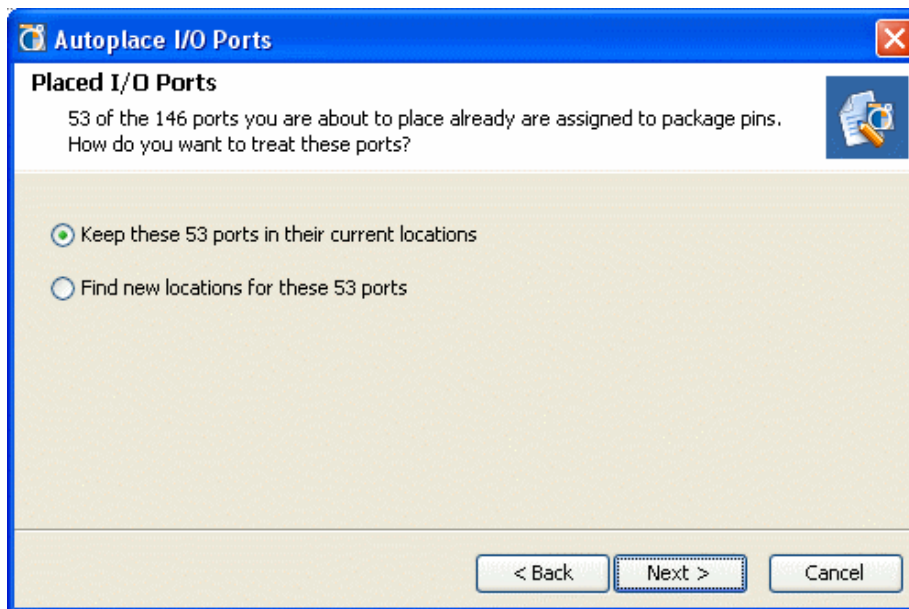


Figure 29: Autoplace I/O Ports Dialog Box

If any I/O Ports are selected when the command is run, they are seeded into the Autoplace I/O ports selection filter allowing selective auto placement.

10-4-4. Select **Keep these 53 ports in their current locations**.

10-4-5. Click **Next**.

The number of placed ports in your example design may vary from what is shown in the figure above.

10-4-6. In the Summary dialog box, click **Finish**.

The ports are placed.

10-4-7. In the I/O Ports view, click **Collapse All**.

10-4-8. In the I/O Ports view, select the various Interfaces and buses to observe how they are grouped during placement.

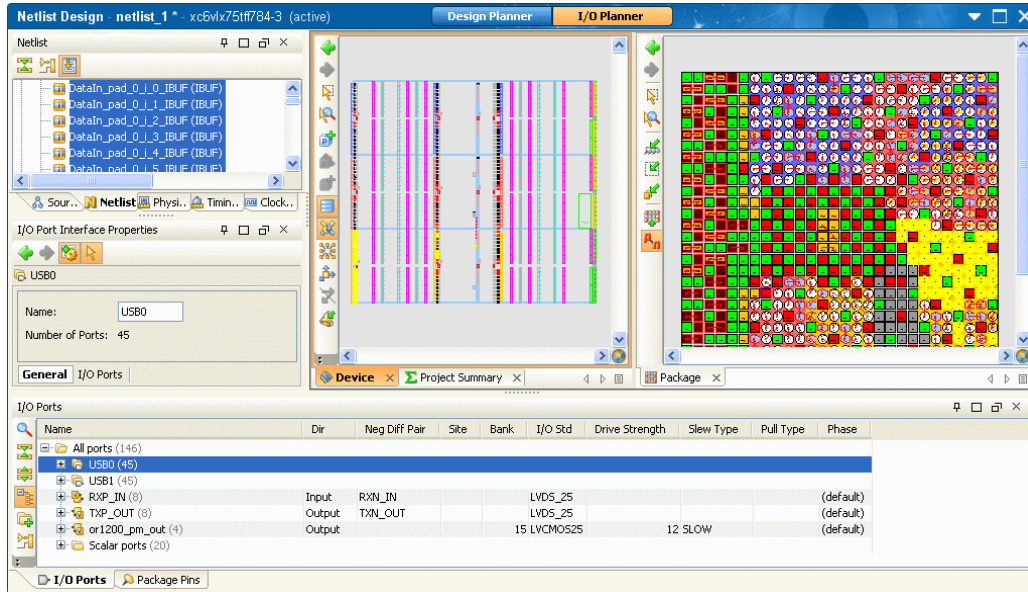


Figure 30: Examine Automatic Placement Results

Step 11: Placing Gigabit Transceivers and Clock Logic

Step 11

The PlanAhead software can be used to place critical clock or I/O related logic. After a synthesized netlist is imported, clocks and clock relationships can be explored and used to lock down these logic objects onto specific device sites. The PlanAhead software groups some logic, such as GTs and their associated I/O pin pairs automatically. This makes selection and placement of GTs and other related logic much less error prone.

11-1. Remove the split Workspace view for the Device and Package view.

Now that the I/O Ports are all placed, the Package view is no longer needed to share the Workspace view. The split view can easily be removed.

11-1-1. Select the Package view tab and drag it onto the Device view tab. The grey rectangle will encompass the entire Device view.

11-1-2. Drop the Package view onto the Device view tab.

11-1-3. Select the Device view to bring it to the front.

11-1-4. Adjust the view size, if needed.

11-2. Maximize the Netlist Design viewing area.

The Planner viewing area can be maximized by hiding the Flow Navigator and Messaging areas.

11-2-1. Click Maximize design view.

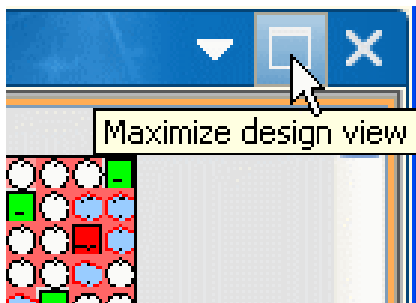


Figure 31: Maximize the Netlist Design Viewing Area

11-3. Search for the Gigabit I/O and Global Clock logic in the design.

11-3-1. Select **Edit > Find**.

The Find dialog box opens.

11-3-2. Click **More** to add another Instance Type to include in the search.

11-3-3. Set the Criteria option for the new filter line to **OR**.

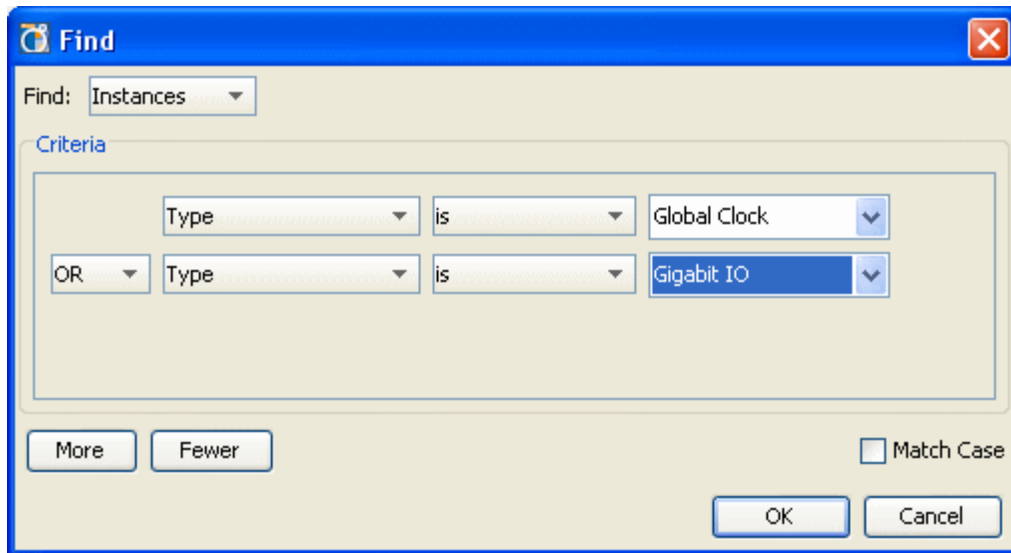


Figure 32: Searching for Global Clocks and Gigabit I/Os

11-3-4. Adjust the selection filters to match Figure 32.

11-3-5. Click **OK**.

The Find Results view opens.

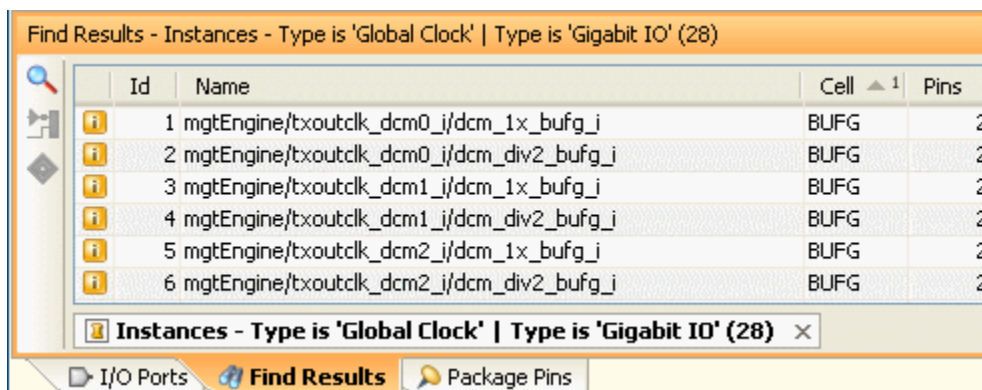


Figure 33: Sorting the Global Clock Object Types

11-3-6. Click the Cell column header to sort based on logic types. The results should match Figure 33.

11-3-7. Scroll down the list of objects. Observe the BUFGs, BUFPGs, DCM_ADVs, and GTXE1s. The objects that are already placed are displayed with a blue striped icon.

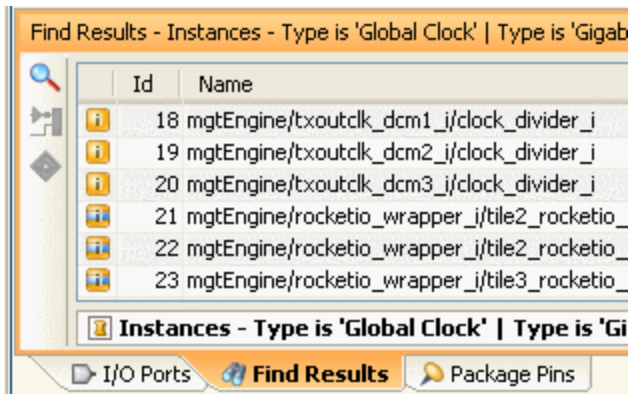


Figure 34: Placed and Unplaced Icons

The logic names of the GTs and DCMs are numbers 0-3. Place these objects in proper relation to each other.

11-3-8. Select each of the GTXE1 objects and observe the seemingly random order of the placement with regard to the logic 0-3 numbers.

11-4. Unplace the GTX interfaces and optimize their placement.

11-4-1. In the Find Results view, press **Shift** and select all of the GTXE1 objects.

11-4-2. Right-click and select **Unplace**.

11-4-3. To sort the Find Results view, click the Name column header to more easily see the numerical order of the names.

11-4-4. Zoom in to the upper right corner of the Device view.

11-4-5. In the Device view, select **Create Site Constraint Mode**.

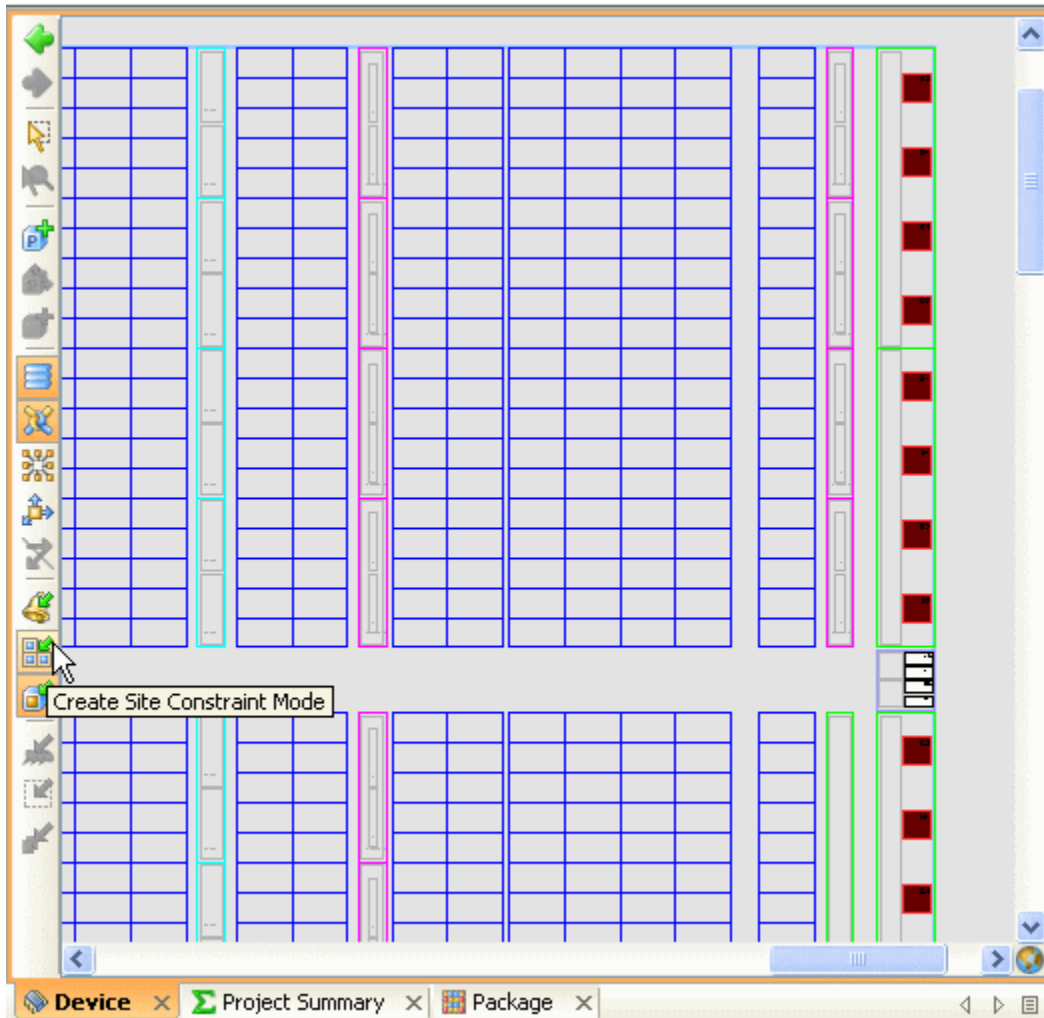


Figure 35: Setting Create Site Constraint Mode to Place LOC Constraints

11-4-6. In the Find Results view, select, drag, and place the first GTXE1 object onto the upper right GTX site.

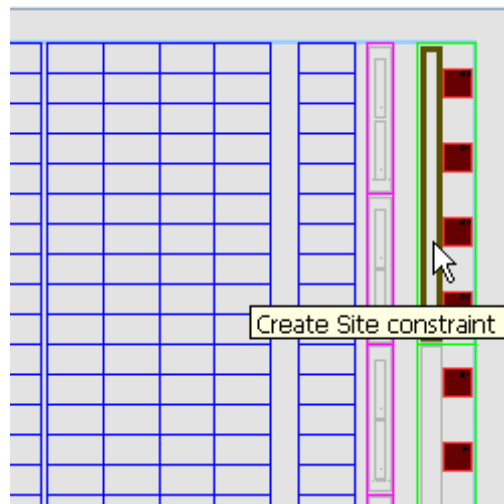


Figure 36: Placing the GTX LOC Constraint

The GT and the related I/Os are all placed together.

11-4-7. In the Find Results view, place the remainder of the GTXE1 objects in order down the right side of the device using the same method you just used.

Do not use the GTX sites directly adjacent to the PCI block if possible.

11-5. Search for DCM and BUFG device sites.

11-5-1. Select **Edit > Find**.

The Find dialog box opens.

11-5-2. Select **Sites** from the Find drop-down list.

11-5-3. Click **More**.

11-5-4. Set Criteria to **OR**.

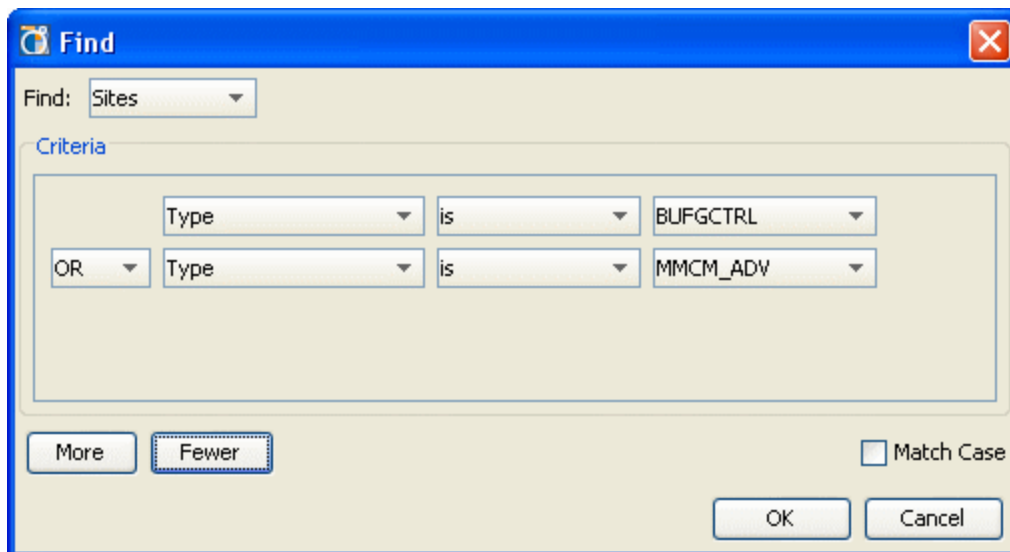


Figure 37: Locating GTP_Dual Sites on Device

11-5-5. Set the filter options to match Figure 37.

11-5-6. Click **OK**.

11-5-7. In the Find Results view, click on the various logic types to see where those logic objects exist on the device.

Device rules require related MMCMs and BUFGs to be placed on the same top or bottom half of the device.

11-6. Zoom in to the upper right quadrant of the Device view.

11-6-1. Press the **Ctrl+A** keys to select all results that are shown in the Find Results view.

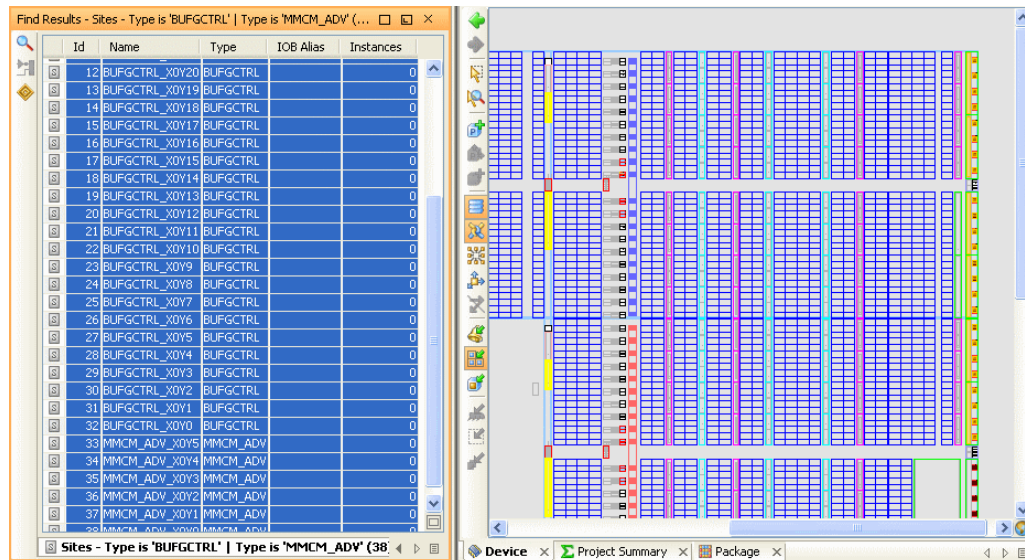


Figure 38: Locating GTP_DUAL, DCM and BUFG Sites on Device

The MMCMs are at the top center and the BUFGs are along the middle I/O column of the device.

11-6-2. Select **Mark** from the right-click menu to place markers on these sites.

11-7. Use the Schematic to trace clock logic

You have now identified where to drag the various logic object types.

There were two searches performed with the Find command. Select the tabs at the bottom of the Find Results view to select which results to display.

11-7-1. In the bottom of the Find Results view, select the Instances – Type is Global Clock tab.

11-7-2. In the Find Result view, select the first DCM_ADV Cell that appears in the list.

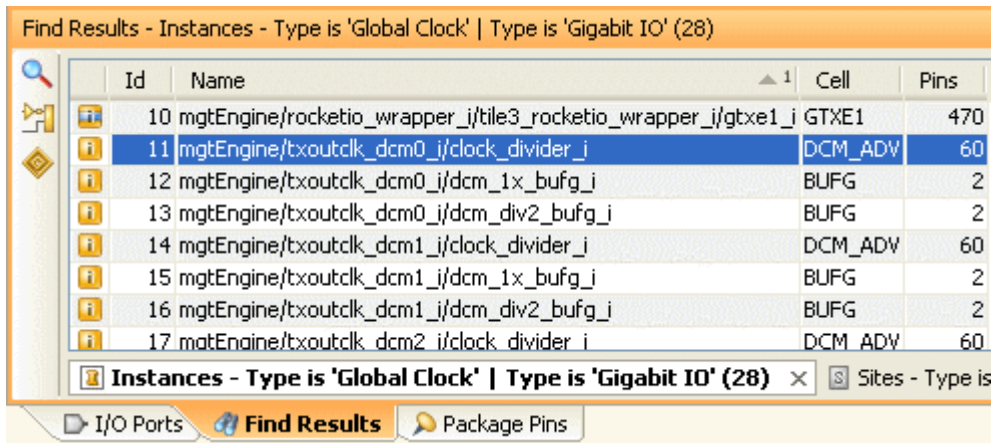




Figure 39: Selecting Clock Logic to Trace in the Schematic

11-7-3. In the Find Results view, click Schematic. 

Use the Schematic view and the Device view to observe net connectivity during clock logic placement.

11-7-4. In the Schematic view, select the Expand all logic outside selected the instance toolbar button .

Observe the logic connectivity of the two BUFGs.

11-7-5. Double click the CLK_IN port on the txoutclk_dcm0_1 module.

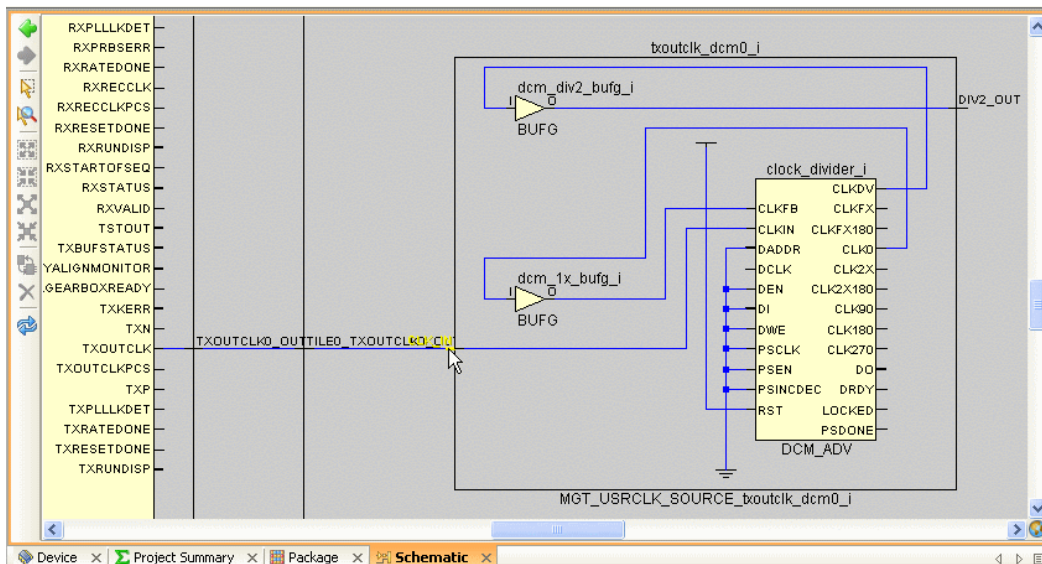



Figure 40: Exploring Clock Logic Connectivity


Observe the logic connection to the GTX instance.

11-7-6. Click **Close** in the Schematic view tab.

The Schematic view closes.

11-8. Place the first set of DCM_ADV and BUFGs.

11-8-1. In the Device view, click Show/Hide IO Nets. 

11-8-2. In the Device view, click Create Site Constraint Mode. 

11-8-3. From the Find Results view, select and drag the top DCM_ADV object onto the top MMCM site. As you drag the logic object, the cursor changes from a circle with slash to a “+” sign indicating that a legal site has been found.

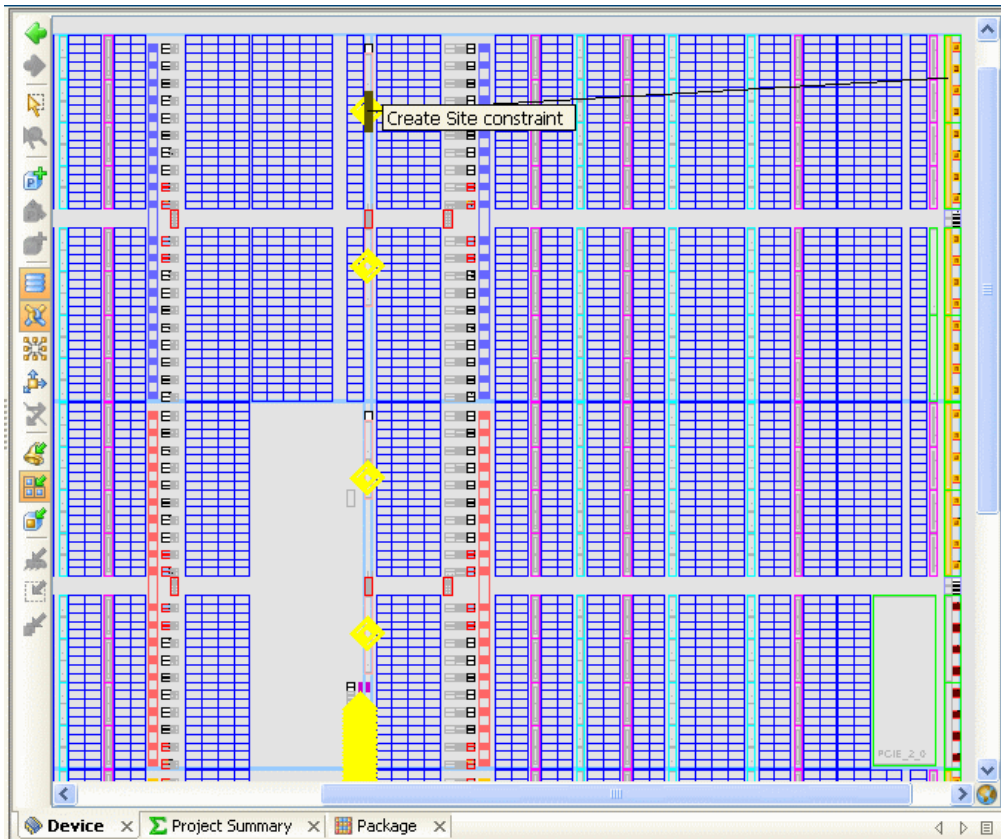


Figure 41: Placing the DCM_ADV in Relation to the GTXE1

11-8-4. In the Find Results view, select the BUFG directly under the DCM you just placed.

11-8-5. Drag the BUFG onto a BUFG site on the top half of the device.

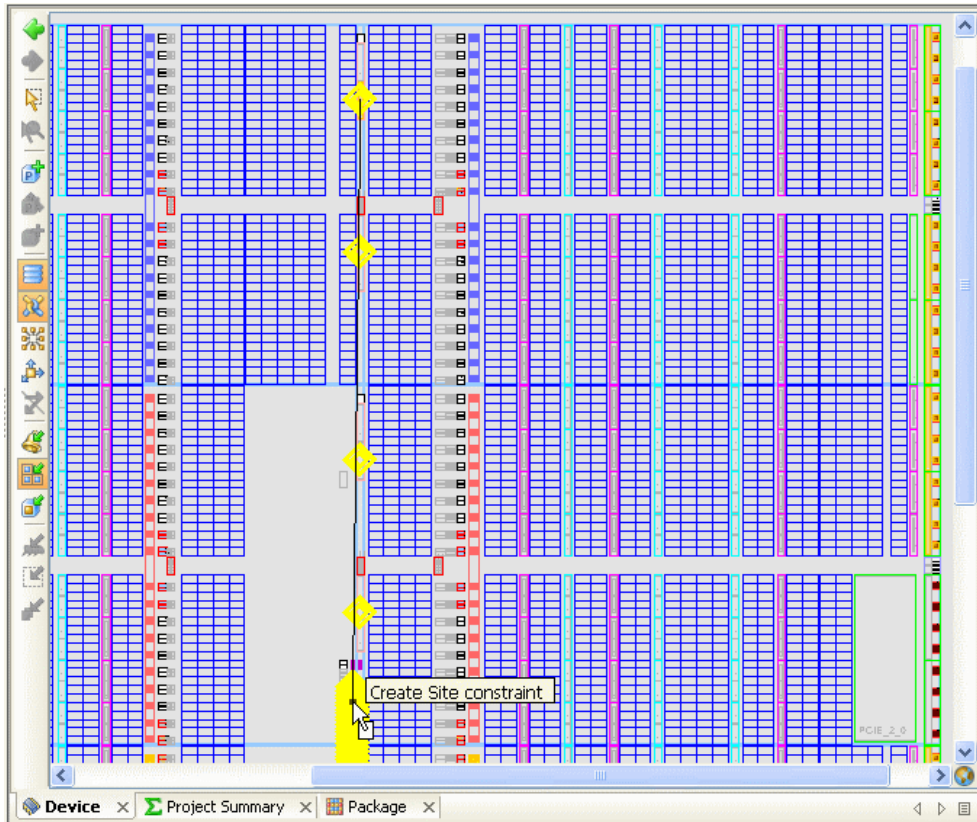



Figure 42: DCM on Top Half of Device

- 11-8-6.** Select and drag each of the DCM_ADV objects from the Find Results view onto a DCM site.
Use the Schematic view and the Device view to observe net connectivity during clock logic placement.
- 11-8-7.** In the Find Results view, go down the list of objects and place all of the DCM_ADVs, and BUFGs as you just did for the first one.
- 11-8-8.** Click Unmark All  to remove the markers on the Sites.
- 11-8-9.** Click **Close**.
The Find Results view closes.

Step 12: View Multi-function pins/set Device Config Mode Step 12

12-1. View Multi-function pins.

12-1-1. Select the Package Pins view tab.

The Package Pins view tab is brought to the front.

12-1-2. Click Maximize.

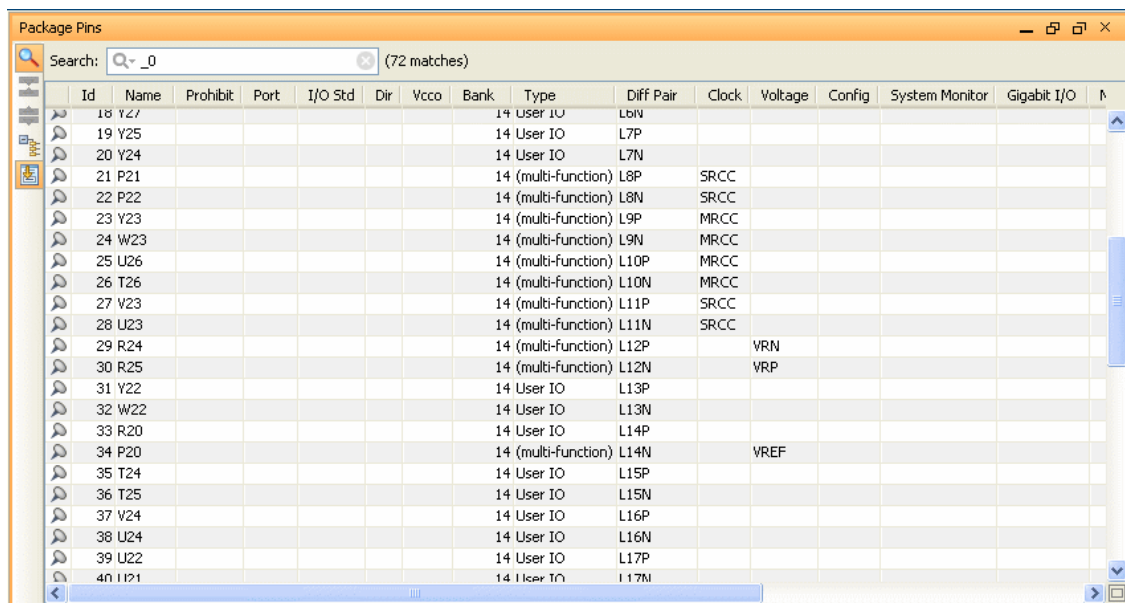
The Package Pins view is maximized.

12-1-3. Click Group by I/O Bank.

The list of Package pins is flattened.

12-1-4. Scroll over the columns in the list.

12-1-5. View the multi-function pins displayed under the Type field.



Id	Name	Prohibit	Port	I/O Std	Dir	Vcco	Bank	Type	Diff Pair	Clock	Voltage	Config	System Monitor	Gigabit I/O	
18	Y27						14	User IO	L6N						
19	Y25						14	User IO	L7P						
20	Y24						14	User IO	L7N						
21	P21						14	(multi-function)	L8P	SRCC					
22	P22						14	(multi-function)	L8N	SRCC					
23	Y23						14	(multi-function)	L9P	MRCC					
24	W23						14	(multi-function)	L9N	MRCC					
25	U26						14	(multi-function)	L10P	MRCC					
26	T26						14	(multi-function)	L10N	MRCC					
27	V23						14	(multi-function)	L11P	SRCC					
28	U23						14	(multi-function)	L11N	SRCC					
29	R24						14	(multi-function)	L12P		VRN				
30	R25						14	(multi-function)	L12N		VRP				
31	Y22						14	User IO	L13P						
32	W22						14	User IO	L13N						
33	R20						14	User IO	L14P						
34	P20						14	(multi-function)	L14N		VREF				
35	T24						14	User IO	L15P						
36	T25						14	User IO	L15N						
37	V24						14	User IO	L16P						
38	U24						14	User IO	L16N						
39	U22						14	User IO	L17P						
40	U21						14	User IO	L17N						

Figure 43: Viewing Multi-Function Pins

Examine the following columns:

- Device Configuration pins (Config)
- System Monitor
- Gigabit I/O

These logic objects can impact I/O assignment, since many of them rely on multi-function pins and have fixed I/O requirements. If the design used in this tutorial contained these logic objects, this table would be filled out allowing you to examine multi-function pins.

12-2. Set Device Configuration Modes.

The PlanAhead software allows you to set one or more device configuration options. Some Configuration modes can also have an impact on multi-function I/O pins. The related pins are displayed in the Config column of the Package Pins view.

12-2-1. Select **Set Configuration Modes** from the right-click menu (Figure 44).

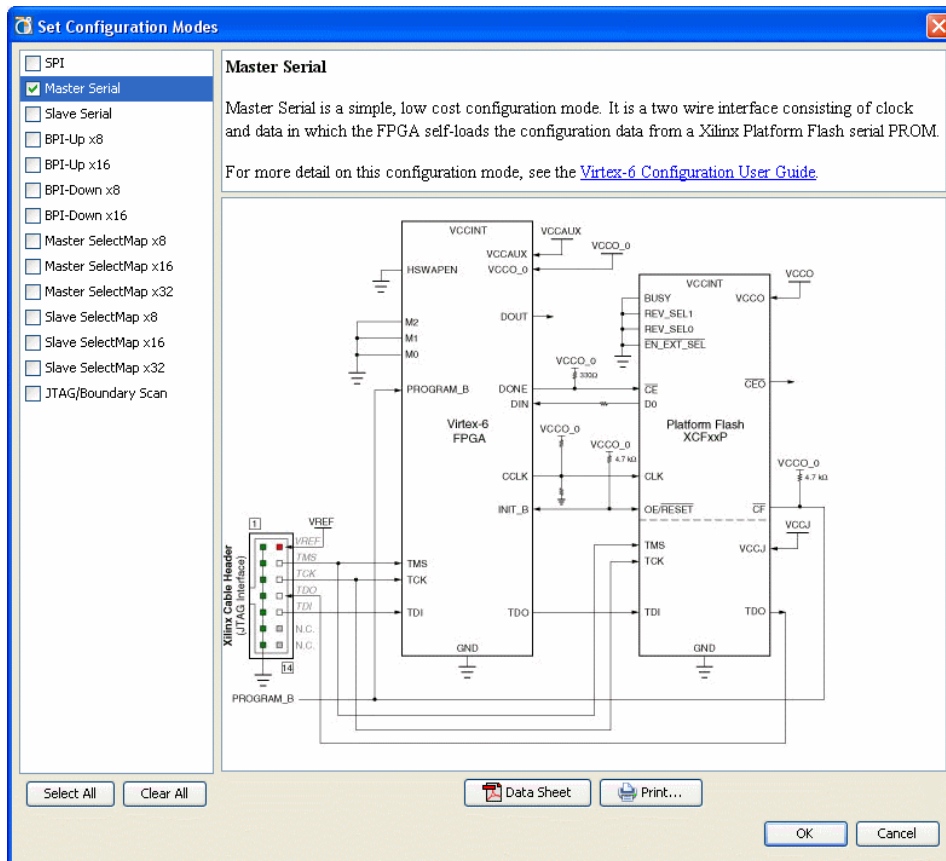


Figure 44: Selecting Device Configuration Modes

12-2-2. Select several of the Modes and view the descriptions, schematics, and Data Sheets.

12-2-3. Click **OK**.

The pins associated with the selected Device Configuration Modes are now displayed in the Package Pins view allowing you to examine potential multi-function pin conflicts. As shown in the last step, there are no PCI, MCB, or other logic that could cause conflicts in this design.

12-2-4. Click Restore. 

Package Pins view is minimized to the original location.

12-3. Restore the Netlist Design viewing area.

12-3-1. Click Restore design view.

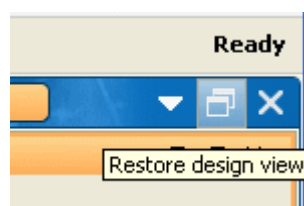


Figure 45: Restoring the View Layout back to the Original Size

Step 13: Running DRC and SSN Analysis

Step 13

The PlanAhead software has an extensive set of I/O related DRC checks to be sure that I/O Ports were assigned accordingly. You can then explore and resolve those violations interactively.

Simultaneous Switching Noise (SSN) Analysis can also be performed to help identify potential signal integrity concerns.

13-1. Run the I/O related DRC checks.

13-1-1. Select **Tools > Run DRC**.

13-1-2. Deselect the Floorplan, DSP48, RAMB16, and Netlist rule categories.

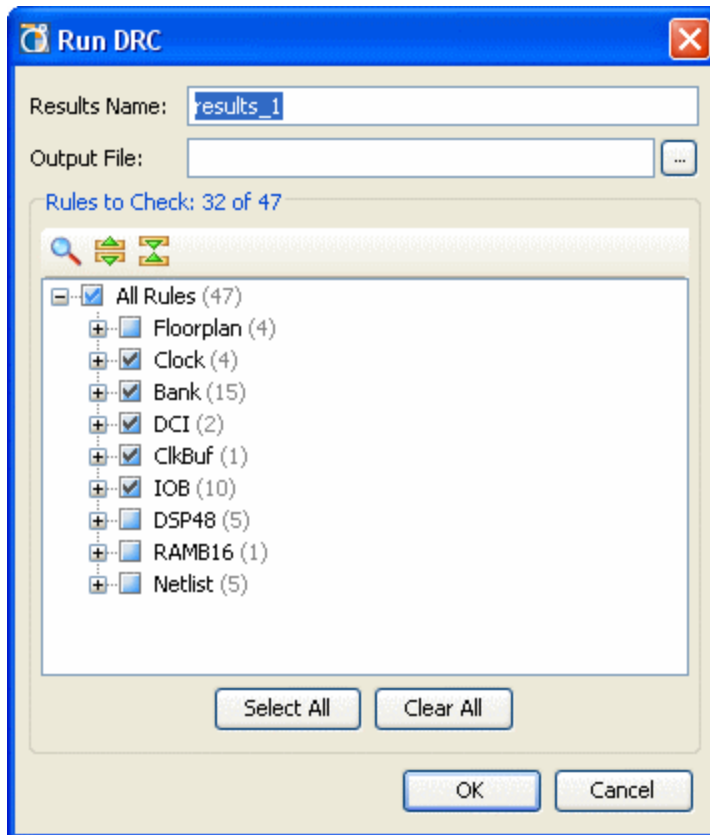


Figure 46: Run I/O Related DRCs

13-1-3. Expand the rules to examine the rule types.

13-1-4. Click **OK**.

In this case, no violations were found. If your design reports violations, proceed regardless for purposes of this tutorial.

13-2. Run the Run Noise Analysis command to check for potential signal integrity.

13-2-1. In the Flow Navigator, select **Run Noise Analysis**.

13-2-2. Click **OK** in the Run SSN Analysis dialog box.

The SSN Results view opens.

Name	I/O Std	Phase	Noise (V)		Margin (V)		Result	Notes
			Contributed	Bank Total	Available	Remaining		
I/O Bank 0 (0)							PASS	No output ports assigned to bank.
I/O Bank 14 (18)	LVC MOS25	(default)		0.184	0.350	0.166	PASS	
I/O Bank 15 (29)	LVC MOS25	(default)		0.208	0.350	0.142	PASS	
I/O Bank 16 (0)							PASS	No output ports assigned to bank.
I/O Bank 24 (3)	(multiple)	(default)		0.069	0.350	0.281	PASS	
Group 1 (3)	LVC MOS25	(default)	0.069	0.069	0.350	0.281		
phy_rst_pad_0_o	LVC MOS25	(default)						
inta_0_0	LVC MOS25	(default)						
XcvSelect_pad_0_o	LVC MOS25	(default)						
I/O Bank 25 (0)							PASS	No output ports assigned to bank.
I/O Bank 26 (0)							PASS	No output ports assigned to bank.
I/O Bank 34 (0)							PASS	No output ports assigned to bank.
I/O Bank 35 (0)							PASS	No output ports assigned to bank.
I/O Bank 36 (0)							PASS	No output ports assigned to bank.

Figure 47: Examine SSN Results View

13-2-3. Maximize the SSN Results View by scrolling down and expanding the list of I/O Banks.

View the Noise information in the report, including Contributed Noise for each Group, Bank Total, Available and Remaining. The Status is PASS for all of the I/O Banks.

13-3. Exit PlanAhead.

13-3-1. Select **File > Exit**.

13-3-2. Click **OK**.

Conclusion

In this tutorial, you:

- Used the I/O Planner I/O pin planning environment to explore device I/O resources and define alternate compatible devices for the design.
- Imported, created, and configured I/O Ports.
- Created Interfaces by grouping the related I/O Ports together.
- Used the semi-automatic placement modes to assign critical I/O Ports to package pins. Placement of the remaining I/O Ports was done using automatic placement.
- Exported and examined the I/O Ports list usable for HDL header or PCB schematic symbol generation.
- Opened a netlist-based project and placed GTs, DCMs, and BUFG objects using logic connectivity as a guide for correct placement.
- Ran DRCs and Noise Analysis to validate legal I/O placement.