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Introduction

This schematic guide is part of the ISE documentation collection. A separate version of this guide is available if you prefer to work with HDL.

This guide contains the following:

- Introduction.
- A list of design elements supported in this architecture, organized by functional categories.
- Individual descriptions of each available primitive.

About Design Elements

This version of the Libraries Guide describes design elements available for this architecture. There are several categories of design elements:

- **Primitives** - The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms." Examples of Xilinx primitives are the simple buffer, BUF, and the D flip-flop with clock enable and clear, FDCE.

- **Macros** - The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives or macros. For example, the FD4CE flip-flop macro is a composite of 4 FDCE primitives.

Xilinx maintains software libraries with hundreds of functional design elements (macros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. This guide is one in a series of architecture-specific libraries.
Chapter 2

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (primitives and macros) are listed in alphanumeric order under each functional category.

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<td>CLK_DIV16RSD</td>
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<td>COMP8</td>
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<td>CB8CLE</td>
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CB8RE | Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8RLE | Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8X1 | Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CB8X2 | Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset
CBD16CE | Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16CLE | Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16CLED | Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16RE | Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD16RLE | Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
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CBD2CLE | Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD2CLED | Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD2RE | Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD2RLE | Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD2X1 | Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
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CBD4CE | Macro: 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD4CLE | Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
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<td>CBD4RLE</td>
<td>Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset</td>
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<td>Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear</td>
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<td>CBD8CLE</td>
<td>Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear</td>
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<td>CBD8X2</td>
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<td>Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear</td>
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<td>CJ4CE</td>
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## Design Element

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<td>Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear</td>
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<td>Macro: 16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear</td>
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<tr>
<td>CR8CE</td>
<td>Macro: 8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>CRD16CE</td>
<td>Macro: 16-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear</td>
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<tr>
<td>CRD8CE</td>
<td>Macro: 8-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear</td>
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## Decoder

<table>
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<tr>
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<th>Description</th>
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<tbody>
<tr>
<td>D2_4E</td>
<td>Macro: 2- to 4-Line Decoder/Demultiplexer with Enable</td>
</tr>
<tr>
<td>D3_8E</td>
<td>Macro: 3- to 8-Line Decoder/Demultiplexer with Enable</td>
</tr>
<tr>
<td>D4_16E</td>
<td>Macro: 4- to 16-Line Decoder/Demultiplexer with Enable</td>
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## Flip Flop

<table>
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<tr>
<th>Design Element</th>
<th>Description</th>
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<tbody>
<tr>
<td>FD</td>
<td>Unknown type: D Flip-Flop</td>
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<tr>
<td>FD16</td>
<td>Macro: Multiple D Flip-Flop</td>
</tr>
<tr>
<td>FD16CE</td>
<td>Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear</td>
</tr>
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<td>Design Element</td>
<td>Description</td>
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<tr>
<td>FD16RE</td>
<td>Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>FD4</td>
<td>Macro: Multiple D Flip-Flop</td>
</tr>
<tr>
<td>FD4CE</td>
<td>Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>FD4RE</td>
<td>Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>FD8</td>
<td>Macro: Multiple D Flip-Flop</td>
</tr>
<tr>
<td>FD8CE</td>
<td>Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear</td>
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<tr>
<td>FD8RE</td>
<td>Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset</td>
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<tr>
<td>FDC</td>
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</tr>
<tr>
<td>FDCE</td>
<td>Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>FDCP</td>
<td>Primitive: D Flip-Flop with Asynchronous Preset and Clear</td>
</tr>
<tr>
<td>FDCPE</td>
<td>Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear</td>
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<tr>
<td>FDD</td>
<td>Macro: Dual Edge Triggered D Flip-Flop</td>
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<td>FDD16</td>
<td>Macro: Multiple Dual Edge Triggered D Flip-Flop</td>
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<tr>
<td>FDD16CE</td>
<td>Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear</td>
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<td>Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear</td>
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<td>FDD8</td>
<td>Macro: Multiple Dual Edge Triggered D Flip-Flop</td>
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<td>FDDC</td>
<td>Macro: D Dual Edge Triggered Flip-Flop with Asynchronous Clear</td>
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<td>Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear</td>
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<td>Primitive: Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear</td>
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<td>Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear</td>
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<td>FDDP</td>
<td>Macro: Dual Edge Triggered D Flip-Flop with Asynchronous Preset</td>
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<tr>
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<td>Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset</td>
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## Chapter 2: Functional Categories

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<tbody>
<tr>
<td>FDDR</td>
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## Chapter 2: Functional Categories

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<td>FTCLE</td>
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<tr>
<td>FTCLEX</td>
<td>Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear</td>
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<tr>
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<td>Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset</td>
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<tr>
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<td>Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear</td>
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<td>FTDCELEX</td>
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<tr>
<td>FTDRSE</td>
<td>Macro: Dual-Edge Triggered Toggle Flip-Flop with Synchronous Reset, Set, and Clock Enable</td>
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<tr>
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<tr>
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<td>Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset</td>
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<tr>
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### General

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<tr>
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<th>Description</th>
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<tr>
<td>GND</td>
<td>Primitive: Ground-Connection Signal Tag</td>
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<tr>
<td>KEEPER</td>
<td>Primitive: KEEPER Symbol</td>
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<tr>
<td>PULLDOWN</td>
<td>Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs</td>
</tr>
<tr>
<td>PULLUP</td>
<td>Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs</td>
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<tr>
<td>VCC</td>
<td>Primitive: VCC-Connection Signal Tag</td>
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### I/O

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<tr>
<td>IBUF16</td>
<td>Macro: 16-Bit Input Buffer</td>
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<tr>
<td>IBUF4</td>
<td>Macro: 4-Bit Input Buffer</td>
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<tr>
<td>IBUF8</td>
<td>Macro: 8-Bit Input Buffer</td>
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<td>IOBUFE</td>
<td>Primitive: Bi-Directional Buffer</td>
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<td>OBUF</td>
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<td>OBUF16</td>
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<td>Macro: 4-Bit Output Buffer</td>
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<tr>
<td>OBUF8</td>
<td>Macro: 8-Bit Output Buffer</td>
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<tr>
<td>OBUFE</td>
<td>Macro: 3-State Output Buffer with Active-High Output Enable</td>
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<td>Macro: 16-Bit 3-State Output Buffer with Active-High Output Enable</td>
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<td>Macro: 4-Bit 3-State Output Buffer with Active-High Output Enable</td>
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<td>OBUFE8</td>
<td>Macro: 8-Bit 3-State Output Buffer with Active-High Output Enable</td>
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<tr>
<td>OBUFT</td>
<td>Primitive: 3-State Output Buffer with Active Low Output Enable</td>
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<td>Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable</td>
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<td>OBUFT4</td>
<td>Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable</td>
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<td>OBUFT8</td>
<td>Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable</td>
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### Latch

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<td>Macro: Multiple Transparent DataLatch</td>
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<td>Macro: Multiple Transparent DataLatch</td>
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<td>LD8</td>
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</tr>
<tr>
<td>LDC</td>
<td>Primitive: Transparent DataLatch with Asynchronous Clear</td>
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<tr>
<td>LDCP</td>
<td>Primitive: Transparent DataLatch with Asynchronous Clear and Preset</td>
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<tr>
<td>LDP</td>
<td>Primitive: Transparent DataLatch with Asynchronous Preset</td>
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### Logic

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<tbody>
<tr>
<td>AND2</td>
<td>Primitive: 2-Input AND Gate with Non-Inverted Inputs</td>
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<tr>
<td>AND2B1</td>
<td>Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs</td>
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<tr>
<td>AND2B2</td>
<td>Primitive: 2-Input AND Gate with Inverted Inputs</td>
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<tr>
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<td>Primitive: 3-Input AND Gate with Non-Inverted Inputs</td>
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<td>Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs</td>
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<tr>
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<td>Primitive: 4-Input AND Gate with Non-Inverted Inputs</td>
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<td>Macro: 6-Input AND Gate with Non-Inverted Inputs</td>
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<tr>
<td>AND7</td>
<td>Macro: 7-Input AND Gate with Non-Inverted Inputs</td>
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<td>Macro: 8-Input AND Gate with Non-Inverted Inputs</td>
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<tr>
<td>INV16</td>
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<td>Macro: Four Inverters</td>
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<td>Macro: Eight Inverters</td>
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<td>Macro: 9-Input NAND Gate with Non-Inverted Inputs</td>
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<td>NOR2</td>
<td>Primitive: 2-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR2B1</td>
<td>Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR2B2</td>
<td>Primitive: 2-Input NOR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>NOR3</td>
<td>Primitive: 3-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR3B1</td>
<td>Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR3B2</td>
<td>Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR3B3</td>
<td>Primitive: 3-Input NOR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>NOR4</td>
<td>Primitive: 4-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR4B1</td>
<td>Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR4B2</td>
<td>Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR4B3</td>
<td>Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR4B4</td>
<td>Primitive: 4-Input NOR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>NOR5</td>
<td>Primitive: 5-Input NOR Gate with Non-Inverted Inputs</td>
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<td>NOR5B1</td>
<td>Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR5B2</td>
<td>Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs</td>
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<td>NOR5B3</td>
<td>Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs</td>
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<tr>
<td>NOR5B4</td>
<td>Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs</td>
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<td>NOR5B5</td>
<td>Primitive: 5-Input NOR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>NOR6</td>
<td>Macro: 6-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR7</td>
<td>Macro: 7-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR8</td>
<td>Macro: 8-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>NOR9</td>
<td>Macro: 9-Input NOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR2</td>
<td>Primitive: 2-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR2B1</td>
<td>Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR2B2</td>
<td>Primitive: 2-Input OR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>OR3</td>
<td>Primitive: 3-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR3B1</td>
<td>Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR3B2</td>
<td>Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>Design Element</td>
<td>Description</td>
</tr>
<tr>
<td>----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>OR3B3</td>
<td>Primitive: 3-Input OR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>OR4</td>
<td>Primitive: 4-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR4B1</td>
<td>Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR4B2</td>
<td>Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR4B3</td>
<td>Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR4B4</td>
<td>Primitive: 4-Input OR Gate with Inverted Inputs</td>
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<tr>
<td>OR5</td>
<td>Primitive: 5-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR5B1</td>
<td>Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR5B2</td>
<td>Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR5B3</td>
<td>Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR5B4</td>
<td>Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR5B5</td>
<td>Primitive: 5-Input OR Gate with Inverted Inputs</td>
</tr>
<tr>
<td>OR6</td>
<td>Macro: 6-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR7</td>
<td>Macro: 7-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR8</td>
<td>Macro: 8-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>OR9</td>
<td>Macro: 9-Input OR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XNOR2</td>
<td>Primitive: 2-Input XNOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XNOR3</td>
<td>Primitive: 3-Input XNOR Gate with Non-Inverted Inputs</td>
</tr>
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<td>XNOR4</td>
<td>Primitive: 4-Input XNOR Gate with Non-Inverted Inputs</td>
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<tr>
<td>XNOR5</td>
<td>Primitive: 5-Input XNOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XNOR6</td>
<td>Macro: 6-Input XNOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XNOR7</td>
<td>Macro: 7-Input XNOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XNOR8</td>
<td>Macro: 8-Input XNOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XNOR9</td>
<td>Macro: 9-Input XNOR Gate with Non-Inverted Inputs</td>
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<tr>
<td>XOR2</td>
<td>Primitive: 2-Input XOR Gate with Non-Inverted Inputs</td>
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<td>XOR3</td>
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<td>XOR8</td>
<td>Macro: 8-Input XOR Gate with Non-Inverted Inputs</td>
</tr>
<tr>
<td>XOR9</td>
<td>Macro: 9-Input XOR Gate with Non-Inverted Inputs</td>
</tr>
</tbody>
</table>
## Chapter 2: Functional Categories

### Mux

<table>
<thead>
<tr>
<th>Design Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M16_1E</td>
<td>Macro: 16-to-1 Multiplexer with Enable</td>
</tr>
<tr>
<td>M2_1</td>
<td>Macro: 2-to-1 Multiplexer</td>
</tr>
<tr>
<td>M2_1B1</td>
<td>Macro: 2-to-1 Multiplexer with D0 Inverted</td>
</tr>
<tr>
<td>M2_1B2</td>
<td>Macro: 2-to-1 Multiplexer with D0 and D1 Inverted</td>
</tr>
<tr>
<td>M2_1E</td>
<td>Macro: 2-to-1 Multiplexer with Enable</td>
</tr>
<tr>
<td>M4_1E</td>
<td>Macro: 4-to-1 Multiplexer with Enable</td>
</tr>
<tr>
<td>M8_1E</td>
<td>Macro: 8-to-1 Multiplexer with Enable</td>
</tr>
</tbody>
</table>

### Shift Register

<table>
<thead>
<tr>
<th>Design Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR16CE</td>
<td>Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR16CLE</td>
<td>Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR16CLED</td>
<td>Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR16RE</td>
<td>Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>SR16RLE</td>
<td>Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>SR16RLED</td>
<td>Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>SR4CE</td>
<td>Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR4CLE</td>
<td>Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR4CLED</td>
<td>Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR4RE</td>
<td>Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>SR4RLE</td>
<td>Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>SR4RLED</td>
<td>Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
<tr>
<td>SR8CE</td>
<td>Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR8CLE</td>
<td>Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR8CLED</td>
<td>Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear</td>
</tr>
<tr>
<td>SR8RE</td>
<td>Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset</td>
</tr>
</tbody>
</table>
### Design Element | Description
--- | ---
SR8RLE | Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLED | Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset
SRD16CE | Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD16CLE | Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD16CLED | Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD16RE | Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD16RLE | Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD16RLED | Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD4CE | Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD4CLE | Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD4CLED | Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD4RE | Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD4RLE | Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD4RLED | Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD8CE | Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD8CLE | Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD8CLED | Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD8RE | Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD8RLE | Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD8RLED | Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
# Shifter

<table>
<thead>
<tr>
<th>Design Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRLSHFT4</td>
<td>Macro: 4-Bit Barrel Shifter</td>
</tr>
<tr>
<td>BRLSHFT8</td>
<td>Macro: 8-Bit Barrel Shifter</td>
</tr>
</tbody>
</table>
This section describes the design elements that can be used with this architecture. The design elements are organized alphabetically.

The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic Table (if any)
- Port Descriptions (if any)
- Design Entry Method
- Available Attributes (if any)
- For more information

You can find examples of VHDL and Verilog instantiation code in the ISE software (in the main menu, select Edit > Language Templates or in the Libraries Guide for HDL Designs for this architecture.)
**ACC1**

Macro: 1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset

![Diagram of ACC1](image)

**Supported Architectures**

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element can add or subtract a 1-bit unsigned-binary word to or from the contents of a 1-bit data register and store the results in the register. The register can be loaded with a 1-bit word. The synchronous reset (R) has priority over all other inputs and, when High, causes the output to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

*Load*

When the load input (L) is High, CE is ignored and the data on the input D0 is loaded into the 1-bit register during the Low-to-High clock (C) transition.

*Add*

When control inputs ADD and CE are both High, the accumulator adds a 1-bit word (B0) and carry-in (CI) to the contents of the 1-bit register. The result is stored in the register and appears on output Q0 during the Low-to-High clock transition. The carry-out (CO) is not registered synchronously with the data output. CO always reflects the accumulation of input B0 and the contents of the register, which allows cascading of ACC1s by connecting CO of one stage to CI of the next stage. In add mode, CO acts as a carry-out, and CO and CI are active-High.

*Subtract*

When ADD is Low and CE is High, the 1-bit word B0 and CI are subtracted from the contents of the register. The result is stored in the register and appears on output Q0 during the Low-to-High clock transition. The carry-out (CO) is not registered synchronously with the data output. CO always reflects the accumulation of input B0 and the contents of the register, which allows cascading of ACC1s by connecting CO of one stage to CI of the next stage. In subtract mode, CO acts as a borrow, and CO and CI are active-Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Design Entry Method**

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ACC16

Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element can add or subtract a 16-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 16-bit data register and store the results in the register. The register can be loaded with the 16-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC16 loads the data on inputs D15 : D0 into the 16-bit register.

This design element operates on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when “overflow” occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when “overflow” occurs.

- For unsigned binary operation, ACC16 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B15 : B0 for ACC16). This allows the cascading of ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

  \[
  \text{unsigned overflow} = \text{CO XOR ADD}
  \]

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC16 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B15 :
B0 for ACC16) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two’s-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Q0: Previous value of Q
Bn: Value of Data input B
CI: Value of input CI

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ACC4

Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element can add or subtract a 4-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 4-bit data register and store the results in the register. The register can be loaded with the 4-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 : D0 into the 4-bit register.

This design element operates on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when “overflow” occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when “overflow” occurs.

- For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC4s by connecting CO of one stage to CI of the next stage. An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

  \[ \text{unsigned overflow} = \text{CO} \oplus \text{ADD} \]

  Ignore OFL in unsigned binary operation.
• For two’s-complement operation, ACC4 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC4) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two’s-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Q0: Previous value of Q
Bn: Value of Data input B
CI: Value of input CI

### Design Entry Method

This design element is only for use in schematics.

### For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
**ACC8**

Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element can add or subtract a 8-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 8-bit data register and store the results in the register. The register can be loaded with the 8-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC8 loads the data on inputs D7 : D0 into the 8-bit register.

This design element operates on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when “overflow” occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when “overflow” occurs.

- For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

  \[
  \text{unsigned overflow} = \text{CO XOR ADD}
  \]

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC8 represents numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 :
B0 for ACC8) and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two’s-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Q0: Previous value of Q
Bn: Value of Data input B
CI: Value of input CI

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

ADD1

Macro: 1-Bit Full Adder with Carry-In and Carry-Out

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a cascaddable 1-bit full adder with carry-in and carry-out. It adds two 1-bit words (A and B) and a carry-in (CI), producing a binary sum (S0) output and a carry-out (CO).

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ADD16

Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A15:A0, B15:B0 and CI, producing the sum output S15:S0 and CO (or OFL).

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>An</td>
<td>Bn</td>
</tr>
</tbody>
</table>

CI: Value of input CI.

Unsigned Binary Versus Two’s Complement - This design element can operate on either 16-bit unsigned binary numbers or 16-bit two’s-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two’s complement, the output can be interpreted as two’s complement. The only functional difference between an unsigned binary operation and a two’s-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while two’s-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two’s complement, follow the OFL output.

Unsigned Binary Operation - For unsigned binary operation, this element represents numbers between 0 and 65535, inclusive. OFL is ignored in unsigned binary operation.

Two’s-Complement Operation - For two’s-complement operation, this element can represent numbers between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two’s-complement operation.

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ADD4

Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A3:A0, B3:B0, and CI producing the sum output S3:S0 and CO (or OFL).

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>An</td>
<td>Bn</td>
</tr>
</tbody>
</table>

CI: Value of input CI.

Unsigned Binary Versus Two's Complement - This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation - For unsigned binary operation, this element represents numbers from 0 to 15, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation - For two's-complement operation, this element can represent numbers between -8 and +7, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ADD8

Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A7:A0, B7:B0, and CI, producing the sum output S7:S0 and CO (or OFL).

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>An</td>
<td>Bn</td>
</tr>
</tbody>
</table>

CI: Value of input CI.

Unsigned Binary Versus Two’s Complement - This design element can operate on either 8-bit unsigned binary numbers or 8-bit two’s-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two’s complement, the output can be interpreted as two’s complement. The only functional difference between an unsigned binary operation and a two’s-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while two’s-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two’s complement, follow the OFL output.

Unsigned Binary Operation - For unsigned binary operation, this element represents numbers between 0 and 255, inclusive. OFL is ignored in unsigned binary operation.

Two’s-Complement Operation - For two’s-complement operation, this element can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two’s-complement operation.

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ADSU1

Macro: 1-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

When the ADD input is High, this element adds two 1-bit words (A0 and B0) with a carry-in (CI), producing a 1-bit output (S0) and a carry-out (CO). When the ADD input is Low, B0 is subtracted from A0, producing a result (S0) and borrow (CO).

In add mode, CO represents a carry-out, and CO and CI are active-High. In subtract mode, CO represents a borrow, and CO and CI are active-Low.

Add Function, ADD=1

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A0</strong></td>
<td><strong>B0</strong></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
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<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Subtract Function, ADD=0

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A0</strong></td>
<td><strong>B0</strong></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
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<td>1</td>
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<tr>
<td>1</td>
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<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Chapter 3: About Design Elements

ADSU16
Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
When the ADD input is High, this element adds two 16-bit words (A15:A0 and B15:B0) and a carry-in (CI), producing a 16-bit sum output (S15:S0) and carry-out (CO) or overflow (OFL).

When the ADD input is Low, this element subtracts B15:B0 from A15:A0, producing a difference output and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>A</th>
<th>B</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>A</td>
<td>B</td>
<td>S</td>
</tr>
<tr>
<td>1</td>
<td>An</td>
<td>Bn</td>
<td>An+Bn+CI*</td>
</tr>
<tr>
<td>0</td>
<td>An</td>
<td>Bn</td>
<td>An-Bn-CI*</td>
</tr>
<tr>
<td>CI*:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADD = 0, CI, CO active LOW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CI*:</td>
<td>ADD = 1, CI, CO active HIGH</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unsigned Binary Versus Two’s Complement - This design element can operate on either 16-bit unsigned binary numbers or 16-bit two’s-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two’s complement, the output can be interpreted as two’s complement. The only functional difference between an unsigned binary operation and a two’s-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while two’s complement uses OFL to determine when “overflow” occurs.

With adder/subtracters, either unsigned binary or two’s-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.
**Unsigned Binary Operation** - For unsigned binary operation, this element can represent numbers between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

\[
\text{unsigned overflow} = \text{CO} \oplus \text{ADD}
\]

OFL is ignored in unsigned binary operation.

**Two’s-Complement Operation** - For two’s-complement operation, this element can represent numbers between -32768 and +32767, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two’s-complement operation.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ADSU4
Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
When the ADD input is High, this element adds two 4-bit words (A3:A0 and B3:B0) and a carry-in (CI), producing a 4-bit sum output (S3:S0) and a carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B3:B0 from A3:A0, producing a 4-bit difference output (S3:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>A</td>
</tr>
<tr>
<td>1</td>
<td>An</td>
</tr>
<tr>
<td>0</td>
<td>An</td>
</tr>
</tbody>
</table>

CI*: ADD = 0, CI, CO active LOW
CI*: ADD = 1, CI, CO active HIGH

Unsigned Binary Versus Two’s Complement - This design element can operate on either 4-bit unsigned binary numbers or 4-bit two’s-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two’s complement, the output can be interpreted as two’s complement. The only functional difference between an unsigned binary operation and a two’s-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while two’s complement uses OFL to determine when “overflow” occurs.
With adder/subtracters, either unsigned binary or two’s-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

**Unsigned Binary Operation** - For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

\[
\text{unsigned overflow} = \text{CO } \text{XOR } \text{ADD}
\]

OFL is ignored in unsigned binary operation.

**Two’s-Complement Operation** - For two’s-complement operation, this element can represent numbers between -8 and +7, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
ADSU8
Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
When the ADD input is High, this element adds two 8-bit words (A7:A0 and B7:B0) and a carry-in (CI), producing, an 8-bit sum output (S7:S0) and carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B7:B0 from A7:A0, producing an 8-bit difference output (S7:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>A</th>
<th>B</th>
<th>S</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>An</td>
<td>Bn</td>
<td>An+Bn+CI*</td>
</tr>
<tr>
<td>0</td>
<td>An</td>
<td>Bn</td>
<td>An-Bn-Cl*</td>
</tr>
</tbody>
</table>

CI*: ADD = 0, CI, CO active LOW
CI*: ADD = 1, CI, CO active HIGH

Unsigned Binary Versus Two’s Complement - This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when “overflow” occurs.

With adder/subtracters, either unsigned binary or two’s-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.
**Unsigned Binary Operation** - For unsigned binary operation, this element can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

\[ \text{unsigned overflow} = \text{CO} \oplus \text{ADD} \]

OFL is ignored in unsigned binary operation.

**Two’s-Complement Operation** - For two’s-complement operation, this element can represent numbers between -128 and +127, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two’s-complement operation.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND2

Primitive: 2-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

AND2B1

Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND2B2

**Primitive: 2-Input AND Gate with Inverted Inputs**

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND3

Primitive: 3-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND3B1

Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

AND3B2

Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND3B3

Primitive: 3-Input AND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

AND4

Primitive: 4-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND4B1

Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
AND4B2

Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND4B3

Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND4B4

Primitive: 4-Input AND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

AND5

Primitive: 5-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**Chapter 3: About Design Elements**

**AND5B1**

Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND5B2

Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND5B3

Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND5B4

Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

AND5B5

Primitive: 5-Input AND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
AND6

Macro: 6-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND7

Macro: 7-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND8

Macro: 8-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
AND9

Macro: 9-Input AND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
BRLSHFT4

Macro: 4-Bit Barrel Shifter

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a 4-bit barrel shifter that can rotate four inputs (I3 : I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 : O0) reflect the shifted data inputs.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>S0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
BRLSHFT8

Macro: 8-Bit Barrel Shifter

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit barrel shifter, can rotate the eight inputs (I7 : I0) up to eight places. The control inputs (S2 : S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 : O0) reflect the shifted data inputs.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2 S1 S0 I0 I1 I2 I3 I4 I5 I6 I7</td>
<td>O0 O1 O2 O3 O4 O5 O6 O7</td>
</tr>
<tr>
<td>0 0 0 a b c d e f g h</td>
<td>a b c d e f g h</td>
</tr>
<tr>
<td>0 0 1 a b c d e f g h</td>
<td>b c d e f g h a</td>
</tr>
<tr>
<td>0 1 0 a b c d e f g h</td>
<td>c d e f g h a b</td>
</tr>
<tr>
<td>0 1 1 a b c d e f g h</td>
<td>d e f g h a b c</td>
</tr>
<tr>
<td>1 0 0 a b c d e f g h</td>
<td>e f g h a b c d</td>
</tr>
<tr>
<td>1 0 1 a b c d e f g h</td>
<td>f g h a b c d e</td>
</tr>
<tr>
<td>1 1 0 a b c d e f g h</td>
<td>g h a b c d e f</td>
</tr>
<tr>
<td>1 1 1 a b c d e f g h</td>
<td>h a b c d e f g</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
BF

Primitive: General Purpose Buffer

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This is a general-purpose, non-inverting buffer.
This element is not necessary and is removed by the partitioning software (MAP).

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
BUF16

Macro: 16-Bit General Purpose Buffer

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This is a 16-bit, general purpose, non-inverting buffer. In working with CPLDs, this element is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the symbol, or by using the LOGIC_OPT=OFF global attribute.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUF4

Macro: 4-Bit General Purpose Buffer

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This is a 4-bit, general purpose, non-inverting buffer. In working with CPLDs, this element is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the symbol, or by using the LOGIC_OPT=OFF global attribute.

Design Entry Method
This design element is only for use in schematics.

For More Information
• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUF8

Macro: 8-Bit General Purpose Buffer

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This is a 8-bit, general purpose, non-inverting buffer. In working with CPLDs, this element is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the symbol, or by using the LOGIC_OPT=OFF global attribute.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUFE

Primitive: Internal 3-State Buffer with Active High Enable

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a single, 3-state buffer with input I and output O, and an active-High output enable (E). When E is High, data on the input of the buffer is transferred to the corresponding output. When E is Low, the output is high impedance (Z state or Off).

The outputs of separate symbols for this entity can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any given time. If none of the E inputs is active-High, a “weak-keeper” circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it. BUFE output nets assume the High logic level when all connected BUFE buffers are disabled.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
BUFE16

Macro: 16-Bit Internal 3-State Buffer with Active High Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs of I15 : I0 and outputs of O15 : O0 and an active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs.

The outputs of separate symbols for this entity can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any given time. If none of the E inputs is active-High, a “weak-keeper” circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it. BUFE output nets assume the High logic level when all connected BUFE buffers are disabled.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUFE4
Macro: 4-Bit Internal 3-State Buffer with Active High Enable

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™ XPLA3

Introduction
This design element is a multiple 3-state buffer with inputs of I3 : I0 and outputs of O3 : O0 and an active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. The outputs of separate symbols for this entity can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any given time. If none of the E inputs are active-High, a “weak-keeper” circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it. BUFE output nets assume the High logic level when all connected BUFE buffers are disabled.

Logic Table

<table>
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<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

For More Information
• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
BUFE8

Macro: 8-Bit Internal 3-State Buffer with Active High Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs of I7 : I0 and outputs of O7 : O0 and an active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs.

The outputs of separate symbols for this entity can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any given time. If none of the E inputs is active-High, a “weak-keeper” circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it. BUFE output nets assume the High logic level when all connected BUFE buffers are disabled.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUFG

Primitive: Global Clock Buffer

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFGs are typically used on clock nets as well other high fanout nets like sets/resets and clock enables.

Port Descriptions

<table>
<thead>
<tr>
<th>Port</th>
<th>Type</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Input</td>
<td>1</td>
<td>Clock buffer input</td>
</tr>
<tr>
<td>O</td>
<td>Output</td>
<td>1</td>
<td>Clock buffer output</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th>Method</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- BUFG: Global Clock Buffer (source by an internal signal)
-- Xilinx HDL Libraries Guide, version 13.1

BUFG_inst : BUFG
port map (  
  O => O,  -- Clock buffer output
  I => I   -- Clock buffer input
);
```

-- End of BUFG_inst instantiation
Verilog Instantiation Template

// BUFG: Global Clock Buffer (source by an internal signal)

BUFG BUFG_inst {
    .O(O),  // Clock buffer output
    .I(I)   // Clock buffer input
};

// End of BUFG_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUFGSR

Primitive: Global Set/Reset Input Buffer

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element distributes Global Set/Reset (GSR) signals throughout selected flip-flops of an XC9500/XV/XL, CoolRunner™ XPLA3, or CoolRunner™-II device. Global Set/Reset (GSR) control pins are available on these CPLD devices. Consult device data sheets for availability.

This design element always acts as an input buffer. To use it in a schematic, connect the input of the design element symbol to an IPAD or an IOPAD representing the GSR signal source. GSR signals generated on-chip must be passed through an OBUF-type buffer before they are connected to the design element.

For Global Set/Reset (GSR) control, the output of the design element normally connects to the CLR or PRE input of a flip-flop symbol, like FDCP, or any registered symbol with asynchronous clear or preset. The Global Set/Reset (GSR) control signal may pass through an inverter to perform an active-low set/reset. The output of the design element may also be used as an ordinary input signal to other logic elsewhere in the design. This design element can control any number of flip-flops in a design.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUFGTS

Primitive: Global 3-State Input Buffer

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element distributes global output-enable signals throughout the output pad drivers of CPLD devices. Global Three-State (GTS) control pins are available on these CPLD devices. Consult device data sheets for availability.

This element always acts as an input buffer. To use it in a schematic, connect the input of the BUFGTS symbol to an IPAD or an IOPAD representing the GTS signal source. GTS signals generated on-chip must be passed through an OBUF-type buffer before they are connected to this element.

For global 3-state control, the output of this element normally connects to the E input of a 3-state output buffer symbol, OBUFE. The global 3-state control signal may pass through an inverter or control an OBUFT symbol to perform an active-low output-enable. The same 3-state control signal may even be used both inverted and non-inverted to enable alternate groups of device outputs. The output of BUFGTS may also be used as an ordinary input signal to other logic elsewhere in the design. Each BUFGTS can control any number of output buffers in a design.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**BUFT**

**Primitive: Internal 3-State Buffer with Active Low Enable**

![BUFT Symbol]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

**Introduction**

This design element is a single 3-state buffer with input I and an output of O and active-Low output enable (T). When T is Low, data on the input of the buffer is transferred to the corresponding output. When T is High, the output is high impedance (Z state or off).

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at any given time. BUFT output nets assume the High logic level when all connected BUFT buffers are disabled.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>I</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
BUFT16

Macro: 16-Bit Internal 3-State Buffers with Active Low Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs I15:10 and outputs O15:00 and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off).

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at any given time. BUFT output nets assume the High logic level when all connected BUFT buffers are disabled.

Logic Table

<table>
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<tr>
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</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

BUFT4

Macro: 4-Bit Internal 3-State Buffers with Active Low Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs I3:I0 and outputs O3:O0 and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off).

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at any given time. BUFT output nets assume the High logic level when all connected BUFT buffers are disabled.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
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<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**BUFT8**

*Macro: 8-Bit Internal 3-State Buffers with Active Low Enable*

![BUFT8 Symbol](image)

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

**Introduction**

This design element is a multiple 3-state buffer with inputs I7:I0 and outputs O7:O0 and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off).

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at any given time. BUFT output nets assume the High logic level when all connected BUFT buffers are disabled.

**Logic Table**

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</thead>
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<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CB16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEO = TC \cdot CE \)

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB16CLE

Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]
\[ TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdots Q0 \]
\[ CEO = TC \cdot CE \]

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

$z = \text{bit width} - 1$

$TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \cdot UP)$

$CEO = TC \cdot CE$

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB16RE
Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \left( t_{CE-TC} \right) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot ... \cdot Q0 \)

\( CEO = TC \cdot CE \)

Design Entry Method
This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB16RLE

Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
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<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1

TC = Qz•Q(z-1)•Q(z-2)•...•Q0

CEO = TC•CE

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB16X1

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEOU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CEOD is High, provided CLR and L are Low. The counter ignores clock transitions when CEOU and CEOD are Low. Both CEOU and CEOD should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEOU and CEOD are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEOU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
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<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1
TCU = Qz•Q(z-1)•Q(z-2)•...•Q0
TCD = Qz•Q(z-1)•Q(z-2)•...•Q0
CEOU = TCU•CEU
CEOD = TCD•CED

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB16X2

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizeable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
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<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

TCU = QzQ(z-1)Q(z-2)...Q0
TCD = QzQ(z-1)Q(z-2)...Q0
CEOU = TCUCEU
CEOD = TCDCED

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2CE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \) \( (t_{CE,TC}) \), where \( n \) is the number of stages and the time \( t_{CE,TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEO = TC \cdot CE \)

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2CLE

Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
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</tr>
<tr>
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</tbody>
</table>

z = bit width - 1
TC = Qz•Q(z-1)•Q(z-2)•...•Q0
CE0 = TC•CE

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
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</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
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<td>1</td>
</tr>
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</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1

TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP)

CEO = TC•CE

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2RE
Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE\rightarrow TC}) \), where \( n \) is the number of stages and the time \( t_{CE\rightarrow TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R, CE, C</td>
<td>Qz-Q0, TC, CEO</td>
</tr>
<tr>
<td>1, X, ↑</td>
<td>0, 0, 0</td>
</tr>
<tr>
<td>0, 0, X</td>
<td>No change, No change, 0</td>
</tr>
<tr>
<td>0, 1, ↑</td>
<td>Inc, TC, CEO</td>
</tr>
</tbody>
</table>

\( z = \text{bit width - 1} \)
\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)
\( CEO = TC \cdot CE \)

Design Entry Method
This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2RLE

Macro: 2-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]
\[ TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]
\[ CEO = TC \cdot CE \]

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2X1

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizeable AND gates within the component. This results in zero propagation from the CEO and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.
The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ \text{TCU} = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q_0 \]

\[ \text{TCD} = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q_0 \]

\[ \text{CEOU} = \text{TCU} \cdot \text{CEU} \]

\[ \text{CEOD} = \text{TCD} \cdot \text{CED} \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB2X2

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimize AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.
The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
<td>CEU</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
</tr>
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<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit width - 1  
TCU = QzQ(z-1)Q(z-2)...Q0  
TCD = QzQ(z-1)Q(z-2)...Q0  
CEOU = TCUCEU  
CEOD = TCDCED

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB4CE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times (t_{CE\rightarrow TC}) \), where \( n \) is the number of stages and the time \( t_{CE\rightarrow TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEO = TC \cdot CE \)
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**Chapter 3: About Design Elements**

**CB4CLE**

Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \) \((t_{CE-TC})\), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
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<tr>
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<th>Outputs</th>
</tr>
</thead>
<tbody>
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<td>L</td>
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<tr>
<td>1</td>
<td>X</td>
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<td>0</td>
<td>1</td>
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<table>
<thead>
<tr>
<th>CE</th>
<th>C</th>
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</thead>
<tbody>
<tr>
<td>X</td>
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<tr>
<td>↑</td>
<td>↑</td>
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<td>X</td>
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<table>
<thead>
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<th>Qz-Q0</th>
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</thead>
<tbody>
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<tr>
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<td>No change</td>
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<tr>
<td>X</td>
<td>Inc</td>
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</table>

<table>
<thead>
<tr>
<th>TC</th>
<th>CEO</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>TC</td>
<td>CEO</td>
</tr>
<tr>
<td>No change</td>
<td>0</td>
</tr>
<tr>
<td>TC</td>
<td>CEO</td>
</tr>
</tbody>
</table>

z = bit width - 1

TC = Qz•Q(z-1)•Q(z-2)…•Q0

CEO = TC•CE

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \cdot \text{UP}) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \cdot \text{UP}) \]

\[ \text{CEO} = TC \cdot CE \]

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB4RE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R )</td>
<td>( CE )</td>
</tr>
<tr>
<td>1</td>
<td>( X )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot ... \cdot Q0 \)

\( CEO = TC \cdot CE \)
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB4RLE

Macro: 4-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \cdot (t_{CE-TC})$, where $n$ is the number of stages and the time $t_{CE-TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R L CE C</td>
<td>Dz-D0 Qz-Q0 TC CEO</td>
</tr>
<tr>
<td>1 X X ↑</td>
<td>X 0 0 0</td>
</tr>
<tr>
<td>0 1 X ↑</td>
<td>Dn Dn TC CEO</td>
</tr>
<tr>
<td>0 X</td>
<td>No change No change 0</td>
</tr>
<tr>
<td>X Inc</td>
<td>TC CEO</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]
\[ \text{TC} = Qz\cdot Q(z-1)\cdot Q(z-2)\cdot...\cdot Q0 \]
\[ \text{CEO} = \text{TC}\cdot CE \]

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CB4X1

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEU and CED go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEU and CED outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEU and CED outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.
When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1

TCU = Qz • Q(z-1) • Q(z-2) • ... • Q0

TCD = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEOU = TCU • CEU

CEOD = TCD • CED

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB4X2
Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is Low. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimized AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.
The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>-----</td>
<td>---</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1
TCU = QzQ(z-1)Q(z-2)...Q0
TCD = QzQ(z-1)Q(z-2)...Q0
CEOU = TCUCEO
CEOD = TCDCED

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)
\( TC = Qz\cdot Q(z-1)\cdot Q(z-2)\cdot \ldots \cdot Q0 \)
\( CEO = TC\cdot CE \)

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB8CLE

Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \cdot t_{CE-TC}$, where n is the number of stages and the time $t_{CE-TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

$z = \text{bit width} - 1$

$TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0$
### Inputs

<table>
<thead>
<tr>
<th>CLR</th>
<th>L</th>
<th>CE</th>
<th>C</th>
<th>Dz-D0</th>
<th>Qz-Q0</th>
<th>TC</th>
<th>CEO</th>
</tr>
</thead>
</table>

CEO = TC • CE

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \cdot t_{CE-TC}$, where $n$ is the number of stages and the time $t_{CE-TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

$z = \text{bit width} - 1$

$TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \cdot UP)$

$CEO = TC \cdot CE$

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \cdot t_{CE-TC}$, where $n$ is the number of stages and the time $t_{CE-TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
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<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

$z = \text{bit width} - 1$

$TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0$

$CEO = TC \cdot CE$

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CB8RLE

Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times t_{CE\rightarrow TC} \), where \( n \) is the number of stages and the time \( t_{CE\rightarrow TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width - 1} \]

\[ TC = Qz\cdot Q(z-1)\cdot Q(z-2)\cdot ...\cdot Q0 \]

\[ CEO = TC\cdot CE \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB8X1

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
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<td>0</td>
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</tr>
</tbody>
</table>

z = bit width - 1

TCU = Qz•Q(z-1)•Q(z-2)•...•Q0

TCD = Qz•Q(z-1)•Q(z-2)•...•Q0

CEOU = TCU•CEU

CEOD = TCD•CED

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CB8X2

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEU and CED go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CED output might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs and CED is High. To cascade counters, the CEOU and CED outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEU, and CED outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1
TCU = QzQ(z-1)Q(z-2)...Q0
TCD = QzQ(z-1)Q(z-2)...Q0
CEOU = TCUCEU
CEOD = TCDCED

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD16CE

Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width - 1} \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEO = TC \cdot CE \)

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD16CLE
Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \) \((t_{CE-TC}\)) where \( n \) is the number of stages and the time \( t_{CE-TC}\) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR L</td>
<td>CE C Dz : D0 Qz : Q0 TC CEO</td>
</tr>
<tr>
<td>1 X X X X</td>
<td>0 0 0</td>
</tr>
<tr>
<td>0 1 X ↑</td>
<td>Dn Dn TC CEO</td>
</tr>
<tr>
<td>0 1 X ↓</td>
<td>Dn Dn TC CEO</td>
</tr>
<tr>
<td>0 0 0 X</td>
<td>No change No change 0</td>
</tr>
<tr>
<td>0 0 1 ↑</td>
<td>Inc TC CEO</td>
</tr>
<tr>
<td>0 0 1 ↓</td>
<td>Inc TC CEO</td>
</tr>
</tbody>
</table>
Inputs | Outputs
--- | ---
CLR | L | CE | C | Dz : D0 | Qz : Q0 | TC | CEO

\[ z = \text{bit width} - 1 \]
\[ TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]
\[ CEO = TC \cdot CE \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \) \( t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\[ TC = (Q_{z}Q(z-1)Q(z-2)...Q0UP) + (Q_{z}Q(z-1)Q(z-2)...Q0UP) \]

\[ CEO = TCCE \]

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD16RE
Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>X ( \uparrow )</td>
</tr>
<tr>
<td>1</td>
<td>X ( \downarrow )</td>
</tr>
<tr>
<td>0</td>
<td>0 ( X )</td>
</tr>
<tr>
<td>0</td>
<td>1 ( \uparrow )</td>
</tr>
<tr>
<td>0</td>
<td>1 ( \downarrow )</td>
</tr>
</tbody>
</table>

\( z = \) bit width - 1
\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot ... \cdot Q0 \)
\( CEO = TC \cdot CE \)
Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD16RLE

Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
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<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
### Inputs vs. Outputs

<table>
<thead>
<tr>
<th>R</th>
<th>L</th>
<th>CE</th>
<th>C</th>
<th>Dz : D0</th>
<th>Qz : Q0</th>
<th>TC</th>
<th>CEO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>X</td>
<td>Inc</td>
<td>TC</td>
<td>CEO</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>↓</td>
<td>X</td>
<td>Inc</td>
<td>TC</td>
<td>CEO</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]

\[ CEO = TC \cdot CE \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD16X1

Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEOU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEOU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1
TCU = Qz•Q(z-1)•Q(z-2)•...•Q0
TCD = Qz•Q(z-1)•Q(z-2)•...•Q0
CEOU = TCU•CEU
CEOD = TCD•CED

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD16X2

Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizeable AND gates within the component. This results in zero propagation from the CEOU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1

TCU = Qz • Q(z-1) • Q(z-2) • ... • Q0

TCD = Qz • Q(z-1) • Q(z-2) • ... • Q0

CEOU = TCU • CEU

CEOD = TCD • CED

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD2CE
Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdots \cdot Q0 \]

\[ CEO = TC \cdot CE \]
Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CBD2CLE

Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
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<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1
TC = Qz•Q(z-1)•Q(z-2)•...•Q0
CEO = TC•CE

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD2CLED

Macro: 2-Bit Loadable Cascadeable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadeable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadeable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
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</tbody>
</table>

$x = \text{bit width} - 1$

$TC = (QzQ(z-1)Q(z-2)...Q0UP) + (QzQ(z-1)Q(z-2)...Q0UP)$

$CEO = TCCE$

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD2RE

Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<tr>
<th>Inputs</th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CE</td>
<td>C</td>
</tr>
<tr>
<td>R 1</td>
<td>X</td>
<td>↑</td>
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<tr>
<td>R 1</td>
<td>X</td>
<td>↓</td>
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<tr>
<td>0</td>
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<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>↓</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEO = TC \cdot CE \)
Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD2RLE

Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>R</strong></td>
<td><strong>L</strong></td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]
\[ TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]
\[ CEO = TC \cdot CE \]

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD2X1

Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
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</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TCU = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( TCD = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEOU = TCU \cdot CEU \)

\( CEOD = TCD \cdot CED \)

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CBD2X2**

Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

![CBD2X2 Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CED go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CED outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CED outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CED outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
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<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1

TCU = Qz•Q(z-1)•Q(z-2)•...•Q0

TCD = Qz•Q(z-1)•Q(z-2)•...•Q0

CEOU = TCU•CEU

CEOD = TCD•CED

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### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD4CE

Macro: 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<td>0</td>
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\( z = \text{bit width} - 1 \)

\( TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot ... \cdot Q_0 \)

\( CEO = TC \cdot CE \)
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD4CLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
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z = bit width - 1
TC = Qz•Q(z-1)•Q(z-2)•...•Q0
CEO = TC•CE

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \) \( (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
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</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = (QzQ(z-1)Q(z-2)...Q0UP) + (QzQ(z-1)Q(z-2)...Q0UP) \)

\( CEO = TCCE \)

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CBD4RE**

**Macro:** 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

![CBD4RE Diagram](image)

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
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<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \)

\( CEO = TC \cdot CE \)
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD4RLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \times (t_{CE-TC})$, where $n$ is the number of stages and the time $t_{CE-TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
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</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
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<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
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<tr>
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<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bit width - 1
TC = Qz•Q(z-1)•Q(z-2)•...•Q0
CEO = TC•CE

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD4X1

Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CED go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEDD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEDD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEDD outputs are produced by optimizeable AND gates within the component. This results in zero propagation from the CEOU and CEDD inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.
This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
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</tbody>
</table>

z = bit width - 1

TCU = Qz•Q(z-1)•Q(z-2)•...•Q0

TCD = Qz•Q(z-1)•Q(z-2)•...•Q0

CEOU = TCU•CEU

CEOD = TCD•CED

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD4X2

Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs and CED are High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.
This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
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</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TCU = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]

\[ TCD = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]

\[ CEOU = TCU \cdot CEU \]

\[ CEOD = TCD \cdot CED \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD8CE

Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
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</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
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<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
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</tbody>
</table>

\( z = \text{bit width - 1} \)

\( TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \ldots \cdot Q_0 \)

\( CEO = TC \cdot CE \)

Design Entry Method

This design element is only for use in schematics.
For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CBD8CLE

Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times (t_{CE,TC}) \), where \( n \) is the number of stages and the time \( t_{CE,TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
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<tr>
<td>CLR</td>
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</tr>
<tr>
<td>0</td>
<td>1</td>
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</table>

\[ z = \text{bit width} - 1 \]

\[ TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot ... \cdot Q_0 \]

\[ CEO = TC \cdot CE \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
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</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TC = (QzQ(z-1)Q(z-2)\ldots Q0UP) + (QzQ(z-1)Q(z-2)\ldots Q0UP) \]

\[ CEO = TCCE \]

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD8RE

Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R )</td>
<td>( CE )</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
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<tr>
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<td>0</td>
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<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

\( TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot ... \cdot Q0 \)

\( CEO = TC \cdot CE \)
Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CBD8RLE

Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th></th>
<th></th>
<th></th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Qz : Q0</td>
</tr>
<tr>
<td>R</td>
<td>L</td>
<td>CE</td>
<td>C</td>
<td>Dz : D0</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>↓</td>
<td>X</td>
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<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>↑</td>
<td>Dn</td>
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<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>↓</td>
<td>Dn</td>
</tr>
</tbody>
</table>
### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
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</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TC = Q_z \cdot Q(z-1) \cdot Q(z-2) \cdot ... \cdot Q_0 \]

\[ CEO = TC \cdot CE \]
CBD8X1

Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
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</tr>
</tbody>
</table>

z = bit width - 1

TCU = Qz•Q(z-1)•Q(z-2)•...•Q0
TCD = Qz•Q(z-1)•Q(z-2)•...•Q0
CEOU = TCU•CEU
CEOD = TCD•CED

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CBD8X2

Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEDO go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEDO outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CED output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEDO outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEDO outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
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<tr>
<td>1</td>
<td>X</td>
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<td>0</td>
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</tbody>
</table>

\[ z = \text{bit width} - 1 \]

\[ TCU = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]

\[ TCD = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \ldots \cdot Q0 \]

\[ CEOU = TCU \cdot CEU \]

\[ CEOD = TCD \cdot CED \]

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CD4CE

Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4CE is a 4-bit (stage), asynchronous clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

TC = Q3•!Q2•!Q1•Q0  
CEO = TC•CE

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CD4CLE**

**Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear**

![Diagram of CD4CLE](image)

**Supported Architectures**

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binarycoded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When (CLR) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the (D) inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The (Q) outputs increment when clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

![State Diagram](image)

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \cdot t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.
This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

TC = Q3 • !Q2 • !Q1 • Q0  
CEO = TC • CE

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CD4RE

Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4RE is a 4-bit (stage), synchronous resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When (R) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The (Q) outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>CE</th>
<th>C</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
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<td>R</td>
<td>CE</td>
<td>C</td>
<td>Q3</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>Inc</td>
</tr>
<tr>
<td>0</td>
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<td>X</td>
<td>No Change</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>1</td>
</tr>
</tbody>
</table>

TC = Q3•!Q2•!Q1•Q0  
CEO = TC•CE

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CD4RLE

Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4RLE is a 4-bit (stage), synchronous loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( n \times t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.
Chapter 3: About Design Elements

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
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</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

TC = Q3•!Q2•!Q1•Q0
CEO = TC•CE

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CDD4CE**

**Macro:** 4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

CDD4CE is a 4-bit (stage), asynchronous clearable, cascadable dual edge triggered Binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \times t_{CE-TC}$, where $n$ is the number of stages and the time $t_{CE-TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

TC = Q3•!Q2•!Q1•Q0

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CDD4CLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

CDD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, dual edge triggered Binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transitions. The Q outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period.

The clock period must be greater than \( n (t_{CE-TC}) \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.
This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
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</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
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</tr>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

TC = Q3•!Q2•!Q1•Q0
CEO = TC•CE

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CDD4RE

Macro: 4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

CDD4RE is a 4-bit (stage), synchronous resettable, cascadable dual edge triggered binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High or High-to-Low clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than \( t_{CE-TC} \), where \( n \) is the number of stages and the time \( t_{CE-TC} \) is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
</tr>
<tr>
<td>-----</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

TC = Q3!Q2!Q1Q0
CEO = TCCE

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CDD4RLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This is a 4-bit (stage), synchronous loadable, resettable, dual edge triggered binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High or High-to-Low clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n(tCE-TC), where n is the number of stages and the time tCE-TC is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CJ4CE

Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJ4RE

Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CJ5CE

Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJ5RE

Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJ8CE

Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJ8RE
Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE</td>
<td>C</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJD4CE

Macro: 4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This element is a dual edge triggered clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJD4RE
Macro: 4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a resettable dual edge triggered Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<tr>
<th>Inputs</th>
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<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJD5CE

Macro: 5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This element is a dual edge triggered clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<th>Outputs</th>
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</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJD5RE

Macro: 5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a resettable dual edge triggered Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CJD8CE

Macro: 8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This element is a dual edge triggered clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<tr>
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</thead>
<tbody>
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<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CJD8RE
Macro: 8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a resettable dual edge triggered Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<tr>
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<th>Outputs</th>
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<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

q = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV10

**Primitive:** Simple Global Clock Divide by 10

![CLK_DIV10 Diagram](image)

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLkin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV10: Simple clock Divide by 10
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV10_inst : CLK_DIV10
port map (  
  CLKDV => CLKDV,    -- Divided clock output  
  CLkin => CLkin    -- Clock input
);

-- End of CLK_DIV10_inst instantiation
```

Verilog Instantiation Template

// CLK_DIV10: Simple clock Divide by 10
//    CoolRunner-II

CLK_DIV10 CLK_DIV10_inst (  
    .CLKDV(CLKDV),  // Divided clock output
    .CLKIN(CLKIN)   // Clock input
);

// End of CLK_DIV10_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV10R

Primitive: Global Clock Divide by 10 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV10R: Clock Divide by 10 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV10R_inst : CLK_DIV10R
port map (  
  CLKDV => CLKDV,  -- Divided clock output
  CDRST => CDRST,  -- Synchronous reset input
  CLKin => CLKin   -- Clock input
);
-- End of CLK_DIV10R_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV10R: Clock Divide by 10 with synchronous reset
// CoolRunner-II
CLK_DIV10R CLK_DIV10R_inst (  
  .CLKDV(CLKDV),  // Divided clock output  
  .CDRST(CDRST),  // Synchronous reset input  
  .CLKIN(CLKIN)   // Clock input  
);

// End of CLK_DIV10R_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV10RSD

Primitive: Global Clock Divide by 10 with Synchronous Reset and Start Delay

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV10RSD: Clock Divide by 10 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV10RSD_inst : CLK_DIV10RSD
generic map (    DIVIDER_DELAY => 1)
port map (     CLKDV => CLKDV, -- Divided clock output     CDRST => CDRST, -- Synchronous reset input     CLKin => CLKin -- Clock input );

-- End of CLK_DIV10RSD_inst instantiation
```

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Verilog Instantiation Template

// CLK_DIV10RSD: Clock Divide by 10 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV10RSD #(  
  .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting
) CLK_DIV10RSD_inst (  
  .CLKDV(CLKDV), // Divided clock output
  .CDRST(CDRST), // Synchronous reset input
  .CLKin(CLKin) // Clock input
);

// End of CLK_DIV10RSD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
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CLK_DIV10SD

**Primitiv:** Global Clock Divide by 10 with Start Delay

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV10SD: Clock Divide by 10 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV10SD_inst : CLK_DIV10SD
generic map (
  DIVIDER_DELAY => 1)
port map (
  CLKDV => CLKDV,  -- Divided clock output
  CLKin => CLKin   -- Clock input
);

-- End of CLK_DIV10SD_inst instantiation
```

---

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Verilog Instantiation Template

// CLK_DIV10SD: Clock Divide by 10 with start delay
// CoolRunner-II

CLK_DIV10SD #(  
  .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting  
) CLK_DIV10SD_inst (  
  .CLKDV(CLKDVs), // Divided clock output  
  .CDRST(CDRST),  // Synchronous reset input  
  .CLKin(CLKin)   // Clock input  
);

// End of CLK_DIV10SD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV12

Primitive: Simple Global Clock Divide by 12

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV12: Simple clock Divide by 12
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV12_inst : CLK_DIV12
port map (  
  CLKDV => CLKDV, -- Divided clock output
  CLKIN => CLKIN -- Clock input
);

-- End of CLK_DIV12_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV12: Simple clock Divide by 12
// CoolRunner-II

CLK_DIV12 CLK_DIV12_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CLKIN(CLKIN) // Clock input
);

// End of CLK_DIV12_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV12R

Primitive: Global Clock Divide by 12 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV12R: Clock Divide by 12 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV12R_inst : CLK_DIV12R
port map (
  CLKDV => CLKDV, -- Divided clock output
  CDRST => CDRST, -- Synchronous reset input
  CLKIN => CLKIN -- Clock input
);
-- End of CLK_DIV12R_inst instantiation
```
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Verilog Instantiation Template

// CLK_DIV12R: Clock Divide by 12 with synchronous reset
// CoolRunner-II

CLK_DIV12R CLK_DIV12R_inst(
    .CLKDV(CLKDV), // Divided clock output
    .CDRST(CDRST), // Synchronous reset input
    .CLKIN(CLKIN)  // Clock input
);

// End of CLK_DIV12R_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CLK_DIV12RSD**

**Primitive: Global Clock Divide by 12 with Synchronous Reset and Start Delay**

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV12RSD: Clock Divide by 12 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV12RSD_inst : CLK_DIV12RSD
generic map (   DIVIDER_DELAY => 1)
port map (   CLKDV => CLKDV, -- Divided clock output   CDRST => CDRST, -- Synchronous reset input   CLKin => CLKin -- Clock input   );
-- End of CLK_DIV12RSD_inst instantiation
```

---

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Verilog Instantiation Template

// CLK_DIV12RSD: Clock Divide by 12 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV12RSD #( // Number of clock cycles to delay before starting
    .DIVIDER_DELAY(1), // Number of clock cycles to delay before starting
    .CLKDV(CLKDVF), // Divided clock output
    .CDRST(CDRST), // Synchronous reset input
    .CLKIN(CLKIN) // Clock input
) CLK_DIV12RSD_inst;

// End of CLK_DIV12RSD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV12SD

**Primitive:** Global Clock Divide by 12 with Start Delay

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal $gclk<2>$ by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device $gclk<2>$ pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by $(n + 1)$ clocks, where $n$ is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV12SD: Clock Divide by 12 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV12SD_inst : CLK_DIV12SD
generic map (    DIVIDER_DELAY => 1)
port map (    CLKDV => CLKDV, -- Divided clock output
             CLKin => CLkin -- Clock input
);
-- End of CLK_DIV12SD_inst instantiation
```

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Verilog Instantiation Template

```verilog
// CLK_DIV12SD: Clock Divide by 12 with start delay
// CoolRunner-II
CLK_DIV12SD #(// Number of clock cycles to delay before starting
    .DIVIDER_DELAY(1)
) CLK_DIV12SD_inst (// Divided clock output
    .CLKDV(CLKDV),
    .CDRST(CDRST), // Synchronous reset input
    .CLKin(CLKin) // Clock input
);
// End of CLK_DIV12SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV14

Primitive: Simple Global Clock Divide by 14

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV14: Simple clock Divide by 14
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV14Instantiate : CLK_DIV14
port map (  
  CLKDV => CLKDV,  -- Divided clock output
  CLKIN => CLKIN   -- Clock input
);  
-- End of CLK_DIV14Instantiate instantiation
```

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Verilog Instantiation Template

// CLK_DIV14: Simple clock Divide by 14
// CoolRunner-II

CLK_DIV14 CLK_DIV14_inst (  
   .CLKDV(CLKDV), // Divided clock output  
   .CLKIN(CLKIN)  // Clock input  
);

// End of CLK_DIV14_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV14R

Primitive: Global Clock Divide by 14 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV14R: Clock Divide by 14 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV14R_inst : CLK_DIV14R
port map (  
  CLKDV => CLKDV, -- Divided clock output  
  CDRST => CDRST, -- Synchronous reset input  
  CLKIN => CLKIN -- Clock input  
);
-- End of CLK_DIV14R_inst instantiation
```

Verilog Instantiation Template

// CLK_DIV14R: Clock Divide by 14 with synchronous reset
// CoolRunner-II

CLK_DIV14R CLK_DIV14R_inst (  
   .CLKDV(CLKD),  // Divided clock output
   .CDRST(CDRST),  // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);  

// End of CLK_DIV14R_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV14RSD

Primitive: Global Clock Divide by 14 with Synchronous Reset and Start Delay

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n+1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV14RSD: Clock Divide by 14 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV14RSD_inst : CLK_DIV14RSD
generic map (DIVIDER_DELAY => 1)
port map (CLKDV => CLKDV, -- Divided clock output
CDRST => CDRST, -- Synchronous reset input
CLKIN => CLKin -- Clock input);
```

-- End of CLK_DIV14RSD_inst instantiation
Verilog Instantiation Template

```verilog
// CLK_DIV14RSD: Clock Divide by 14 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV14RSD #( // Number of clock cycles to delay before starting
  .DIVIDER_DELAY(1),
  .CLKDV(CLKDV), // Divided clock output
  .CDRST(CDRST), // Synchronous reset input
  .CLKin(CLKin)  // Clock input
)
CLK_DIV14RSD_inst;

// End of CLK_DIV14RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CLK_DIV14SD

Primitive: Global Clock Divide by 14 with Start Delay

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV14SD: Clock Divide by 14 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV14SD_inst : CLK_DIV14SD
generic map (DIVIDER_DELAY => 1)
port map (CLKDV => CLKDV, -- Divided clock output
CLKin => CLKin -- Clock input );

-- End of CLK_DIV14SD_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV14SD: Clock Divide by 14 with start delay
// CoolRunner-II

CLK_DIV14SD #(  
    .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting
) CLK_DIV14SD_inst (  
    .CLKDV(CLKDV), // Divided clock output
    .CDRST(CDRST), // Synchronous reset input
    .CLKin(CLKin)  // Clock input
);

// End of CLK_DIV14SD_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLKDIV16

Primitive: Simple Global Clock Divide by 16

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

When using this component, the dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method
This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template
Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV16: Simple clock Divide by 16
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV16_inst : CLK_DIV16
port map (   
    CLKD => CLKD,   -- Divided clock output
    CLKin => CLKin   -- Clock input
);
-- End of CLK_DIV16_inst instantiation
```
Verilog Instantiation Template

```verilog
// CLK_DIV16: Simple clock Divide by 16
// CoolRunner-II

CLK_DIV16 CLK_DIV16_inst (  
    .CLKDV(CLKDV), // Divided clock output  
    .CLKIN(CLKIN)  // Clock input  
);
// End of CLK_DIV16_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CLK_DIV16R

Primitive: Global Clock Divide by 16 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV16R: Clock Divide by 16 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV16R_inst : CLK_DIV16R
port map (  
  CLKDV => CLKDV, -- Divided clock output  
  CDRST => CDRST, -- Synchronous reset input  
  CLKin => CLKin -- Clock input
);

-- End of CLK_DIV16R_inst instantiation
```

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Verilog Instantiation Template

// CLK_DIV16R: Clock Divide by 16 with synchronous reset
// CoolRunner-II

CLK_DIV16R CLK_DIV16R_inst (  
  .CLKDV(CLKDV), // Divided clock output  
  .CDRST(CDRST), // Synchronous reset input  
  .CLKIN(CLKIN) // Clock input
);

// End of CLK_DIV16R_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CLK_DIV16RSD**

**Primitive: Global Clock Divide by 16 with Synchronous Reset and Start Delay**

![CLK_DIV16RSD Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV16RSD: Clock Divide by 16 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV16RSD_inst : CLK_DIV16RSD
generic map (
    DIVIDER_DELAY => 1)
port map (  
    CLKDV => CLKDV, -- Divided clock output
    CDRST => CDRST, -- Synchronous reset input
    CLKIN => CLKIN -- Clock input
);

-- End of CLK_DIV16RSD_inst instantiation
```

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Verilog Instantiation Template

// CLK_DIV16RSD: Clock Divide by 16 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV16RSD #(  
  .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting  
) CLK_DIV16RSD_inst (  
  .CLKDV(CLKDV),  // Divided clock output  
  .CDRST(CDRST),  // Synchronous reset input  
  .CLKin(CLKin)  // Clock input
);

// End of CLK_DIV16RSD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV16SD

Primitive: Global Clock Divide by 16 with Start Delay

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV16SD: Clock Divide by 16 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV16SD_inst : CLK_DIV16SD
generic map (DIVIDER_DELAY => 1)
port map (CLKDV => CLKDV, -- Divided clock output
          CLKin => CLKin, -- Clock input
          );
-- End of CLK_DIV16SD_inst instantiation
```

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Verilog Instantiation Template

// CLK_DIV16SD: Clock Divide by 16 with start delay
//              CoolRunner-II

CLK_DIV16SD #(  
  .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting  
) CLK_DIV16SD_inst (  
  .CLKDV(CLKD), // Divided clock output  
  .CDRST(CDRST), // Synchronous reset input  
  .CLIN(CLKIN) // Clock input  
);
// End of CLK_DIV16SD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV2

Primitive: Simple Global Clock Divide by 2

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method
This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template
Unless they already exist, copy the following two statements and paste them before the entity declaration.

Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV2: Simple clock Divide by 2
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV2_inst : CLK_DIV2
port map (  
  CLKDV => CLKDV, -- Divided clock output  
  CLKin => CLKin -- Clock input
);

-- End of CLK_DIV2_inst instantiation
Verilog Instantiation Template

// CLK_DIV2: Simple clock Divide by 2
// CoolRunner-II

CLK_DIV2 CLK_DIV2_inst (  
    .CLKDV(CLKDV),     // Divided clock output
    .CLKin(CLKin)      // Clock input
);

// End of CLK_DIV2_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV2R

Primitive: Global Clock Divide by 2 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV2R: Clock Divide by 2 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV2R_inst : CLK_DIV2R
port map (    CLKD => CLKDV, -- Divided clock output
  CDRST => CDRST, -- Synchronous reset input
  CLKIN => CLKin, -- Clock input
);
-- End of CLK_DIV2R_inst instantiation
```
Verilog Instantiation Template

// CLKDIV2R: Clock Divide by 2 with synchronous reset
//                CoolRunner-II

CLK_DIV2R CLK_DIV2R_inst (  
    .CLKDV(CLKDv),  // Divided clock output
    .CDRST(CDRST),  // Synchronous reset input
    .CLKIN(CLKIN)   // Clock input
);

// End of CLK_DIV2R_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV2RSD

**Primitive: Global Clock Divide by 2 with Synchronous Reset and Start Delay**

<table>
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<tr>
<td>CLKDV</td>
</tr>
</tbody>
</table>

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRSt inputs can only be connected to the device gclk<2> and CDRSt pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRSt input is an active High synchronous reset. If CDRSt is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV2RSD: Clock Divide by 2 with synchronous reset and start delay
--  CoolRunner-II
--  Xilinx HDL Libraries Guide, version 13.1

CLK_DIV2RSD_inst : CLK_DIV2RSD
generic map (   
  DIVIDER_DELAY  => 1)
port map (   
  CLKDV  => CLKDV,   -- Divided clock output
  CDRST  => CDRST,   -- Synchronous reset input
  CLKin  => CLKin    -- Clock input
);
-- End of CLK_DIV2RSD_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV2RSD: Clock Divide by 2 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV2RSD #(   
    .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting
) CLK_DIV2RSD_inst ( 
    .CLKDV(CLKDv), // Divided clock output
    .CDRST(CDRST), // Synchronous reset input
    .CLKIN(CLKIN)  // Clock input
);

// End of CLK_DIV2RSD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CLK_DIV2SD**

*Primitive: Global Clock Divide by 2 with Start Delay*

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKD V output is 50-50. The CLKD V output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKD V output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKD V output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV2SD: Clock Divide by 2 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV2SD_inst : CLK_DIV2SD
generic map (  
  DIVIDER_DELAY => 1)
port map (  
  CLKD V => CLKD V,  
  CLKin => CLKin  
);  

-- End of CLK_DIV2SD_inst instantiation
```

---

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Verilog Instantiation Template

// CLK_DIV2SD: Clock Divide by 2 with start delay
//         CoolRunner-II

CLK_DIV2SD #(  
  .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting  
) CLK_DIV2SD_inst (  
  .CLKDV(CLKD),    // Divided clock output  
  .CDRST(CDRST),  // Synchronous reset input  
  .CLKIN(CLKIN)   // Clock input  
);

// End of CLK_DIV2SD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV4

Primitive: Simple Global Clock Divide by 4

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV4: Simple clock Divide by 4
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV4_inst : CLK_DIV4
port map (    
  CLKDV => CLKDV, -- Divided clock output
  CLKIN => CLKIN -- Clock input
);

-- End of CLK_DIV4_inst instantiation
```
Verilog Instantiation Template

```verilog
// CLK_DIV4: Simple clock Divide by 4
//             CoolRunner-II

CLK_DIV4 CLK_DIV4_inst (  
    .CLKDV(CLKD),     // Divided clock output
    .CLKIN(CKI)       // Clock input
);

// End of CLK_DIV4_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV4R

Primitive: Global Clock Divide by 4 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV4R: Clock Divide by 4 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV4R_inst : CLK_DIV4R
port map (  
  CLKDV => CLKDV, -- Divided clock output  
  CDRST => CDRST, -- Synchronous reset input  
  CLKIN => CLKIN  -- Clock input
);
-- End of CLK_DIV4R_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV4R: Clock Divide by 4 with synchronous reset
//             CoolRunner-II

CLK_DIV4R CLK_DIV4R_inst (  
    .CLKDV(CLKDV),   // Divided clock output  
    .CDRST(CDRST),  // Synchronous reset input  
    .CLKIN(CLKIN)   // Clock input  
);

// End of CLK_DIV4R_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV4RSD

Primitive: Global Clock Divide by 4 with Synchronous Reset and Start Delay

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method
This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template
Unless they already exist, copy the following two statements and paste them before the entity declaration.

Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV4RSD: Clock Divide by 4 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV4RSD_inst : CLK_DIV4RSD
generic map (    DIVIDER_DELAY => 1)
port map (    CLKDV => CLKDV, -- Divided clock output
            CDRST => CDRST, -- Synchronous reset input
            CLKin => CLKin -- Clock input
            );
-- End of CLK_DIV4RSD_inst instantiation
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Verilog Instantiation Template

// CLK_DIV4RSD: Clock Divide by 4 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV4RSD #(  
  .DIVIDER_DELAY(1),  // Number of clock cycles to delay before starting
) CLK_DIV4RSD_inst (  
  .CLKDV(CLKDV),     // Divided clock output
  .CDRST(CDRST),    // Synchronous reset input
  .CLKin(CLKin)     // Clock input
);

// End of CLK_DIV4RSD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV4SD

Primitive: Global Clock Divide by 4 with Start Delay

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by \((n + 1)\) clocks, where \(n\) is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV4SD: Clock Divide by 4 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV4SD_inst : CLK_DIV4SD
generic map (DIVIDER_DELAY => 1)
port map (CLKDV => CLKDV, CLKIN => CLKIN);  

-- End of CLK_DIV4SD_inst instantiation
```

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Verilog Instantiation Template

// CLK_DIV4SD: Clock Divide by 4 with start delay
//             CoolRunner-II

CLK_DIV4SD #(  
  .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting  
) CLK_DIV4SD_inst (    
  .CLKDV(CLKDV), // Divided clock output  
  .CDRST(CDRST), // Synchronous reset input  
  .CLKin(CLKin)  // Clock input
);

// End of CLK_DIV4SD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CLK_DIV6**

**Primitive: Simple Global Clock Divide by 6**

![CLK_DIV6 Diagram](image)

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV6: Simple clock Divide by 6
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV6_inst : CLK_DIV6
port map (  
    CLKDV => CLKDV, -- Divided clock output  
    CLKin => CLKin -- Clock input
);

-- End of CLK_DIV6_inst instantiation
```

---

**CPLD Libraries Guide**

UG606 (v 13.1) March 1, 2011  
[www.xilinx.com](http://www.xilinx.com)
Verilog Instantiation Template

// CLK_DIV6: Simple clock Divide by 6
//               CoolRunner-II

CLK_DIV6 CLK_DIV6_inst (  
  .CLKDV(CLKDV), // Divided clock output  
  .CLKIN(CLKIN)  // Clock input  
);

// End of CLK_DIV6_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV6R

Primitive: Global Clock Divide by 6 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal \( gclk<2> \) by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device \( gclk<2> \) and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV6R: Clock Divide by 6 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV6R_inst : CLK_DIV6R
port map (
    CLKDV => CLKDV, -- Divided clock output
    CDRST => CDRST, -- Synchronous reset input
    CLKIN => CLKIN -- Clock input
);
-- End of CLK_DIV6R_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV6R: Clock Divide by 6 with synchronous reset
// CoolRunner-II

CLK_DIV6R CLK_DIV6R_inst (
    .CLKDV(CLKDV),  // Divided clock output
    .CDRST(CDRST),  // Synchronous reset input
    .CLKIN(CLKIN)   // Clock input
);

// End of CLK_DIV6R_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**CLK_DIV6RSD**

**Primitive:** Global Clock Divide by 6 with Synchronous Reset and Start Delay

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element divides a user-provided external clock signal gclk<2> by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

**Design Entry Method**

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV6RSD: Clock Divide by 6 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV6RSD_inst : CLK_DIV6RSD
generic map (    DIVIDER_DELAY => 1)
port map (    CLKDV => CLKDV, -- Divided clock output    CDRST => CDRST, -- Synchronous reset input    CLKIN => CLKIN -- Clock input    );
-- End of CLK_DIV6RSD_inst instantiation
```

---

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www.xilinx.com
Verilog Instantiation Template

// CLK_DIV6RSD: Clock Divide by 6 with synchronous reset and start delay
//                  CoolRunner-II

CLK_DIV6RSD #(  // Number of clock cycles to delay before starting
  .DIVIDER_DELAY(1)
) CLK_DIV6RSD_inst (  // Divided clock output
  .CLKDV(CLKDV),
  .CDRST(CDRST),  // Synchronous reset input
  .CLKIN(CLKIN)   // Clock input
);

// End of CLK_DIV6RSD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV6SD

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKin input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV6SD: Clock Divide by 6 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV6SD_inst : CLK_DIV6SD
generic map (DIVIDER_DELAY => 1)
port map (CLKDV => CLKD, -- Divided clock output
          CLKin => CLKin -- Clock input)

-- End of CLK_DIV6SD_inst instantiation
```
Verilog Instantiation Template

```verilog
// CLK_DIV6SD: Clock Divide by 6 with start delay
// CoolRunner-II
CLK_DIV6SD #(// Number of clock cycles to delay before starting
   .DIVIDER_DELAY(1)) // Divided clock output
   .CLKDV(CLKDV), // Synchronous reset input
   .CDRST(CDRST), // Clock input
   .CLKin(CLKin)
CLK_DIV6SD_inst(
);
// End of CLK_DIV6SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CLK_DIV8

Primitive: Simple Global Clock Divide by 8

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV8: Simple clock Divide by 8
--  CoolRunner-II
--  Xilinx HDL Libraries Guide, version 13.1
CLK_DIV8_inst : CLK_DIV8
port map (  
    CLKDV => CLKDV, -- Divided clock output  
    CLKIN => CLKIN   -- Clock input
);

-- End of CLK_DIV8_inst instantiation
Verilog Instantiation Template

// CLK_DIV8: Simple clock Divide by 8
// CoolRunner-II

CLK_DIV8 CLK_DIV8_inst (  
  .CLKDV(CLKDV), // Divided clock output  
  .CLKIN(CLKIN)  // Clock input
);

// End of CLK_DIV8_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV8R

Primitive: Global Clock Divide by 8 with Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV8R: Clock Divide by 8 with synchronous reset
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV8R_inst : CLK_DIV8R
port map (  
  CLKDV => CLKDV,  -- Divided clock output   
  CDRST => CDRST,  -- Synchronous reset input   
  CLKIN => CLKIN   -- Clock input
);

-- End of CLK_DIV8R_inst instantiation
Verilog Instantiation Template

// CLK_DIV8R: Clock Divide by 8 with synchronous reset
// CoolRunner-II

CLK_DIV8R CLK_DIV8R_inst (   .CLKDV(CLKDV), // Divided clock output
    .CDRST(CDRST), // Synchronous reset input
    .CLKIN(CLKIN) // Clock input
);

// End of CLK_DIV8R_inst instantiation

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
CLK_DIV8RSD

Primitive: Global Clock Divide by 8 with Synchronous Reset and Start Delay

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32A or XC2C64A. The CLKin and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method
This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template
Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV8RSD: Clock Divide by 8 with synchronous reset and start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1

CLK_DIV8RSD_inst : CLK_DIV8RSD
generic map (  
  DIVIDER_DELAY => 1)
port map (  
  CLKDV => CLKDV, -- Divided clock output  
  CDRST => CDRST, -- Synchronous reset input  
  CLKin => CLKin -- Clock input
);
-- End of CLK_DIV8RSD_inst instantiation
```
Verilog Instantiation Template

```verilog
// CLK_DIV8RSD: Clock Divide by 8 with synchronous reset and start delay
// CoolRunner-II

CLK_DIV8RSD #(  
    .DIVIDER_DELAY(1)   // Number of clock cycles to delay before starting
) CLK_DIV8RSD_inst (  
    .CLKDV(CLKDV),      // Divided clock output
    .CDRST(CDRST),      // Synchronous reset input
    .CLKin(CLKin)       // Clock input
);

// End of CLK_DIV8RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

CLK_DIV8SD

Primitive: Global Clock Divide by 8 with Start Delay

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32A or XC2C64A. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- CLK_DIV8SD: Clock Divide by 8 with start delay
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
CLK_DIV8SD_inst : CLK_DIV8SD
generic map (DIVIDER_DELAY => 1)
port map (CLKDV => CLKDV, -- Divided clock output
         CLKIN => CLKIN -- Clock input
         );
-- End of CLK_DIV8SD_inst instantiation
```
Verilog Instantiation Template

// CLK_DIV8SD: Clock Divide by 8 with start delay
//     CoolRunner-II

CLK_DIV8SD #(  
   .DIVIDER_DELAY(1) // Number of clock cycles to delay before starting
) CLK_DIV8SD_inst (  
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLkin(CLKIN) // Clock input
);

// End of CLK_DIV8SD_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**COMP16**

*Macro: 16-Bit Identity Comparator*

![Diagram of COMP16](image)

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a 16-bit identity comparator. The equal output (EQ) is high when A15 : A0 and B15 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
COMP2

Macro: 2-Bit Identity Comparator

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 2-bit identity comparator. The equal output (EQ) is High when the two words A1 : A0 and B1 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
COMP4

Macro: 4-Bit Identity Comparator

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit identity comparator. The equal output (EQ) is high when A3 : A0 and B3 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
COMP8

Macro: 8-Bit Identity Comparator

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit identity comparator. The equal output (EQ) is high when A7 : A0 and B7 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
COMPM16

Macro: 16-Bit Magnitude Comparator

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a 16-bit magnitude comparator that compare two positive Binary-weighted words. It compares A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7, B7</td>
<td>A6, B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>X</td>
</tr>
<tr>
<td>A7&lt;B7</td>
<td>X</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
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<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
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<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
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<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
</tbody>
</table>
Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
COMPM2

Macro: 2-Bit Magnitude Comparator

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a 2-bit magnitude comparator that compare two positive binary-weighted words. It compares A1 : A0 and B1 : B0, where A1 and B1 are the most significant bits.

The greater-than output (GT) is High when \( A > B \), and the less-than output (LT) is High when \( A < B \) When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>B1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
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<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
COMPM4

Macro: 4-Bit Magnitude Comparator

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit magnitude comparator that compares two positive Binary-weighted words. It compares \( A_3 : A_0 \) and \( B_3 : B_0 \), where \( A_3 \) and \( B_3 \) are the most significant bits.

The greater-than output (GT) is High when \( A > B \), and the less-than output (LT) is High when \( A < B \). When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_3, B_3 )</td>
<td>( A_2, B_2 )</td>
</tr>
<tr>
<td>( A_3&gt;B_3 )</td>
<td>X</td>
</tr>
<tr>
<td>( A_3&lt;B_3 )</td>
<td>X</td>
</tr>
<tr>
<td>( A_3=B_3 )</td>
<td>( A_2&gt;B_2 )</td>
</tr>
<tr>
<td>( A_3=B_3 )</td>
<td>( A_2&lt;B_2 )</td>
</tr>
<tr>
<td>( A_3=B_3 )</td>
<td>( A_2=B_2 )</td>
</tr>
<tr>
<td>( A_3&gt;B_3 )</td>
<td>( A_2=B_2 )</td>
</tr>
<tr>
<td>( A_3&gt;B_3 )</td>
<td>( A_2=A_2 )</td>
</tr>
<tr>
<td>( A_3&gt;B_3 )</td>
<td>( A_2=B_2 )</td>
</tr>
<tr>
<td>( A_3&gt;B_3 )</td>
<td>( A_2=B_2 )</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

COMPM8
Macro: 8-Bit Magnitude Comparator

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This design element is an 8-bit magnitude comparator that compare two positive Binary-weighted words. It compares A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7, B7</td>
<td>A6, B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>X</td>
</tr>
<tr>
<td>A7&lt;B7</td>
<td>X</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7=B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&gt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&lt;B6</td>
</tr>
<tr>
<td>A7&gt;B7</td>
<td>A6&lt;B6</td>
</tr>
</tbody>
</table>
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CR16CE

Macro: 16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-bit cascadable, clearable, binary ripple counter with clock enable and asynchronous clear.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is \( n(t_{C\rightarrow Q}) \), where \( n \) is the number of stages and the time \( t_{C\rightarrow Q} \) is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CR8CE

Macro: 8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit cascadable, clearable, binary, ripple counter with clock enable and asynchronous clear.

The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is \( n(t_{C \rightarrow Q}) \), where \( n \) is the number of stages and the time \( t_{C \rightarrow Q} \) is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CRD16CE
Macro: 16-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a dual edge triggered 16-bit cascadable, clearable, binary ripple counter.
The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low and Low-to-High clock (C) transitions. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is n(tC→Q), where n is the number of stages and the time tC→Q is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit width - 1

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
CRD8CE
Macro: 8-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a dual edge triggered 8-bit cascadable, clearable, binary ripple counter.
The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low and Low-to-High clock (C) transitions. The counter ignores clock transitions when CE is Low.
Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is \( n(t_{C-Q}) \), where \( n \) is the number of stages and the time \( t_{C-Q} \) is the C-to-Qz propagation delay of each stage.
This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\( z = \text{bit width} - 1 \)

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

D2_4E
Macro: 2- to 4-Line Decoder/Demultiplexer with Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this element is High, one of four active-High outputs (D3 : D0) is selected with a 2-bit binary address (A1 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
D3_8E
Macro: 3- to 8-Line Decoder/Demultiplexer with Enable

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
When the enable (E) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 : D0) is selected with a 3-bit binary address (A2 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>A1</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
D4_16E

Macro: 4- to 16-Line Decoder/Demultiplexer with Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this design element is High, one of 16 active-High outputs (D15: D0) is selected with a 4-bit binary address (A3: A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD

Macro: D Flip-Flop

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FD16

Macro: Multiple D Flip-Flop

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple D-type flip-flops with data inputs (D) and data outputs (Q), with a 16-bit register, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dz : D0</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD16CE
Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a 16-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ z = \text{bit-width} - 1 \]

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 16-bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD16RE
Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a 16-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 16-bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD4

Macro: Multiple D Flip-Flop

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple D-type flip-flops with data inputs (D) and data outputs (Q), with a 4-bit register, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
</tbody>
</table>

$z = \text{bit-width} - 1$

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD4CE

Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 4-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD4RE

Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 4-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD8

Macro: Multiple D Flip-Flop

```
  D[7:0]  FD8  Q[7:0]
   |      |      |
   C      |
```

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple D-type flip-flops with data inputs (D) and data outputs (Q), with a 8-bit register, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dz : D0</td>
<td>C</td>
</tr>
<tr>
<td></td>
<td>Qz : Q0</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FD8CE**

Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear

![FD8CE Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a 8-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

**Design Entry Method**

This design element is only for use in schematics.

**Available Attributes**

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 8-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FD8RE

Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 8-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDC

Macro: D Flip-Flop with Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

For XC9500XL and XC9500XV devices, logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDCE and FDPE flip-flops may take advantage of the clock-enable p-term.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th>Method</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
LIBRARY UNISIM;
USE UNISIM.VCOMPONENTS.ALL;

-- FDCE: Single Data Rate D Flip-Flop with Asynchronous Clear and
--      Clock Enable (posedge clk). All families.
-- Xilinx HDL Libraries Guide, version 13.1

FDCE_INST : FDCE
  GENERIC MAP (
    INIT => '0') -- Initial value of register ('0' or '1')
  PORT MAP (
    Q => Q, -- Data output
    C => C, -- Clock input
    CE => CE, -- Clock enable input
    CLR => CLR, -- Asynchronous clear input
    D => D -- Data input
  );

-- End of FDCE_INST instantiation
```

Verilog Instantiation Template

```verilog
// FDCE: Single Data Rate D Flip-Flop with Asynchronous Clear and
//       Clock Enable (posedge clk).
//       All families.

FDCE #(
  .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDCE_INST (
    .Q(Q), // Data output
    .C(C), // Clock input
    .CE(CE), // Clock enable input
    .CLR(CLAR), // Asynchronous clear input
    .D(D) // Data input
);

// End of FDCE_INST instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDCP

Primitive: D Flip-Flop with Asynchronous Preset and Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the (Q) output High; CLR, when High, resets the output Low. Data on the (D) input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDCPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs. The asynchronous active high PRE sets the Q output High; that active high CLR resets the output Low and has precedence over the PRE input. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored and the previous value is retained. The FDCPE is generally implemented as a slice or IOB register within the device.

For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net. For FPGA devices, upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Note While this device supports the use of asynchronous set and reset, it is not generally recommended to be used for in most cases. Use of asynchronous signals pose timing issues within the design that are difficult to detect and control and also have an adverse affect on logic optimization causing a larger design that can consume more power than if a synchronous set or reset is used.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Chapter 3: About Design Elements

Port Descriptions

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q</td>
<td>Output</td>
<td>1</td>
<td>Data output</td>
</tr>
<tr>
<td>C</td>
<td>Input</td>
<td>1</td>
<td>Clock input</td>
</tr>
<tr>
<td>CE</td>
<td>Input</td>
<td>1</td>
<td>Clock enable input</td>
</tr>
<tr>
<td>CLR</td>
<td>Input</td>
<td>1</td>
<td>Asynchronous clear input</td>
</tr>
<tr>
<td>D</td>
<td>Input</td>
<td>1</td>
<td>Data input</td>
</tr>
<tr>
<td>PRE</td>
<td>Input</td>
<td>1</td>
<td>Asynchronous set input</td>
</tr>
</tbody>
</table>

Design Entry Method

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0,1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration and on GSR.</td>
</tr>
</tbody>
</table>

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- FDCPE: Single Data Rate D Flip-Flop with Asynchronous Clear, Set and Clock Enable (posedge clk). All families.
-- Xilinx HDL Libraries Guide, version 13.1

FDCPE_inst : FDCPE
generic map (
    INIT => '0') -- Initial value of register ('0' or '1')
port map (  
    Q => Q, -- Data output
    C => C, -- Clock input
    CE => CE, -- Clock enable input
    CLR => CLR, -- Asynchronous clear input
    D => D, -- Data input
    PRE => PRE, -- Asynchronous set input
);

-- End of FDCPE_inst instantiation
```
Verilog Instantiation Template

// FDCPE: Single Data Rate D Flip-Flop with Asynchronous Clear, Set and
//       Clock Enable (posedge clk).
//       Virtex-4/5, Spartan-3/3E/3A/3A DSP

FDCPE #(
  .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDCPE_inst ( //
  .Q(Q), // Data output
  .C(C), // Clock input
  .CE(CE), // Clock enable input
  .CLR(CLR), // Asynchronous clear input
  .D(D), // Data input
  .PRE(PRE) // Asynchronous set input
);

// End of FDCPE_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDD
Macro: Dual Edge Triggered D Flip-Flop

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a single dual edge triggered D-type flip-flop with data input (D) and data output (Q). The data on the D input is loaded into the flip-flop during the Low-to-High and the High-to-Low clock (C) transitions.
This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
<tr>
<td>1</td>
<td>↓</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDD16

Macro: Multiple Dual Edge Triggered D Flip-Flop

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a multiple dual edge triggered D-type flip-flop with data inputs (D) and data outputs (Q). It is a 16-bit register with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dz : D0</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
<tr>
<td>1</td>
<td>↓</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FDD16CE

Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a 16-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDD16RE
Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a 16-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>CE</th>
<th>Dz : D0</th>
<th>C</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>↓</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>No Change</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Dn</td>
<td>↑</td>
<td>Dn</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Dn</td>
<td>↓</td>
<td>Dn</td>
</tr>
</tbody>
</table>

\( z = \text{bit-width} - 1 \)

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDD4

Multiple Dual Edge Triggered D Flip-Flop

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a multiple dual edge triggered D-type flip-flop with data inputs (D) and data outputs (Q). It is a 4-bit register with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dz : D0</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
<tr>
<td>1</td>
<td>↓</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FDD4CE**

Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear

![Diagram of FDD4CE](image)

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a 4-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDD4RE

Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a 4-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>R</strong></td>
<td><strong>CE</strong></td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

*$z = \text{bit-width} - 1$

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDD8
Macro: Multiple Dual Edge Triggered D Flip-Flop

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a multiple dual edge triggered D-type flip-flop with data inputs (D) and data outputs (Q).
It is an 8-bit register with a common clock (C). The data on the D inputs is loaded into the flip-flop during the
Low-to-High and High-to-Low clock (C) transitions.
This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can
simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dz : D0</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>1</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
<tr>
<td>1</td>
<td>↓</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FDD8CE

Macro: 8-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a 8-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FDD8RE
Macro: 8-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit-width - 1

Design Entry Method
This design element is only for use in schematics.

For More Information
• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FDDC

Macro: D Dual Edge Triggered Flip-Flop with Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a single dual edge triggered D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low on the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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</tr>
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<td>0</td>
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</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDCE

Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of FDDCE is transferred to the corresponding data output (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

Logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDDCE and FDDPE flip-flops can take advantage of the clock-enable p-term.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
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<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FDDCP

Primitive: Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
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</tr>
<tr>
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</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDCPE

Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

Library UNISIM;
use UNISIM.vcomponents.all;

-- FDDCPE: Double Data Rate Register with Asynchronous Clear and Set
-- and Clock Enable (Clear has priority). CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
FDDCPE_inst : FDDCPE
port map (  
  Q => Q, -- Data output
  C => C, -- Clock input
  CE => CE, -- Clock enable input
  CLR => CLR, -- Asynchronous clear input
  D => D, -- Data input
  PRE => PRE -- Asynchronous set input
);
-- End of FDDCPE_inst instantiation

Verilog Instantiation Template

// FDDCPE: Double Data Rate Register with Asynchronous Clear and Set
// and Clock Enable (Clear has priority).
// CoolRunner-II
FDDCPE FDDCPE_inst (  
  .Q(Q), // Data output
  .C(C), // Clock input
  .CE(CE), // Clock enable input
  .CLR(CLR), // Asynchronous clear input
  .D(D), // Data input
  .PRE(PRE) // Asynchronous set input
);
// End of FDDCPE_inst instantiation

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FDDP**

**Macro: Dual Edge Triggered D Flip-Flop with Asynchronous Preset**

![FDDP Diagram](image)

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a single dual edge triggered D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRE</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
</tbody>
</table>

**Design Entry Method**

This design element is only for use in schematics.

**Available Attributes**

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDPE

Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, the clock transitions are ignored.

Logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDDCE and FDDPE flip-flops primitives may take advantage of the clock-enable p-term.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRE</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDR
Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a single dual edge triggered D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High and High-to-Low clock (C) transitions. The data on the D input is loaded into the flip-flop when R is Low during the Low-to-High or High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
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<tr>
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</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
Chapter 3: About Design Elements

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FDDRE**

Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Synchronous Reset

![FDDRE Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

FDDRE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
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<tbody>
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**Design Entry Method**

This design element can be used in schematics.

**Available Attributes**

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<td>Sets the initial value of Q output after configuration</td>
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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDRS

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

FDDRS is a single dual edge triggered D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High or High-to-Low clock (C) transitions. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High or High-to-Low clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<thead>
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<th>Inputs</th>
<th>Outputs</th>
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Design Entry Method

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</thead>
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<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDRSE

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set and Clock Enable

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

FDDRSE is a single dual edge triggered D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High or High-to-Low clock transitions. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High or High-to-Low clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<tr>
<th>Inputs</th>
<th>Outputs</th>
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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDS
Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
FDDS is a single dual edge triggered D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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Design Entry Method
This design element is only for use in schematics.

Available Attributes

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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDSE

Macro: D Flip-Flop with Clock Enable and Synchronous Set

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

FDDSE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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Design Entry Method

This design element is only for use in schematics.
Available Attributes

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<td>Sets the initial value of Q output after configuration.</td>
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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FDDSR**

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

FDDSR is a single dual edge triggered D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High or High-to-Low clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High or High-to-Low clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
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**Design Entry Method**

This design element is only for use in schematics.
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<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDDSRE

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset and Clock Enable

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

FDDSRE is a single dual edge triggered D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High or High-to-Low clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High or High-to-Low clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
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<tr>
<th>Inputs</th>
<th>Outputs</th>
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<tbody>
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Design Entry Method

This design element is only for use in schematics.
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<th>Description</th>
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<td>INIT</td>
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<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FDP

Macro: D Flip-Flop with Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the (Q) output High. The data on the (D) input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
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Design Entry Method

This design element is only for use in schematics.

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<td>Sets the initial value of Q output after configuration. For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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Design Entry Method

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This design element can be used in schematics.
### Available Attributes

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<tbody>
<tr>
<td>INIT</td>
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<td>1</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td>For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>

#### For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FDR**

Macro: D Flip-Flop with Synchronous Reset

![FDR Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
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**Design Entry Method**

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**Available Attributes**

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<td>Sets the initial value of Q output after configuration</td>
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**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDRE
Macro: D Flip-Flop with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<th>Inputs</th>
<th>Outputs</th>
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Design Entry Method

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<td>CORE Generator™ and wizards</td>
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<td>Macro support</td>
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Available Attributes

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<th>Description</th>
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<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDRS
Macro: D Flip-Flop with Synchronous Reset and Set

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
FDRS is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low during the Low-to-High clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R S D C Q</td>
<td></td>
</tr>
<tr>
<td>1 X X ↓ 0</td>
<td></td>
</tr>
<tr>
<td>0 1 X ↓ 1</td>
<td></td>
</tr>
<tr>
<td>0 0 D ↓ D</td>
<td></td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

**FDRSE**

Macro: D Flip-Flop with Synchronous Reset and Set and Clock Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDRSE is a single D-type flip-flop with synchronous reset (R), synchronous set (S), clock enable (CE) inputs. The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High clock transition.

Upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>S</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th>Method</th>
<th>Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>
This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

### Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0,1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration and on GSR.</td>
</tr>
</tbody>
</table>

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDS

Macro: D Flip-Flop with Synchronous Set

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDSE

Macro: D Flip-Flop with Clock Enable and Synchronous Set

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For Spartan®-6, Xilinx recommends that the INIT value always matches the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>polarity of the set or reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For this element, the INIT should be 1. If set to 0, additional</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>asynchronous circuitry will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDSR

D Flip-Flop with Synchronous Set and Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDSR is a single D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>R</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FDSRE

Macro: D Flip-Flop with Synchronous Set and Reset and Clock Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDSRE is a single D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-high clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
### Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FJKC

Macro: J-K Flip-Flop with Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR J K C</td>
<td>Q</td>
</tr>
<tr>
<td>1 X X</td>
<td>0</td>
</tr>
<tr>
<td>0 0 0</td>
<td>↑ No Change</td>
</tr>
<tr>
<td>0 0 1</td>
<td>↑ 0</td>
</tr>
<tr>
<td>0 1 0</td>
<td>↑ 1</td>
</tr>
<tr>
<td>0 1 1</td>
<td>↑ Toggle</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Chapter 3: About Design Elements

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FJKCE**

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear

![Diagram](image)

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Design Entry Method**

This design element is only for use in schematics.
## Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FJKCP

Macro: J-K Flip-Flop with Asynchronous Clear and Preset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), and asynchronous preset (PRE) inputs and data output (Q). When the asynchronous clear (CLR) is High, all other inputs are ignored and Q is reset 0. The asynchronous preset (PRE), when High, and CLR set to Low overrides all other inputs and sets the Q output High. When CLR and PRE are Low, Q responds to the state of the J and K inputs during the Low-to-High clock transition, as shown in the following logic table.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.
Chapter 3: About Design Elements

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FJKCPE
Macro: J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), asynchronous preset (PRE), and clock enable (CE) inputs and data output (Q). When the asynchronous clear (CLR) is High, all other inputs are ignored and Q is reset 0. The asynchronous preset (PRE), when High, and CLR set to Low overrides all other inputs and sets the Q output High. When CLR and PRE are Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.
## Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FJKP

Macro: J-K Flip-Flop with Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low, the (Q) output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRE</td>
<td>J</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

**FJKPE**

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low and (CE) is High, the (Q) output responds to the state of the J and K inputs, as shown in the logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRE</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FJKRSE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). When synchronous reset (R) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is reset Low. When synchronous set (S) is High and (R) is Low, output (Q) is set High. When (R) and (S) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, according to the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>S</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FJKSRE
Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a single J-K-type flip-flop with J, K, synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is set High. When synchronous reset (R) is High and (S) is Low, output (Q) is reset Low. When (S) and (R) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>R</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTC
Macro: Toggle Flip-Flop with Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The (Q) output toggles, or changes state, when the toggle enable (T) input is High and (CLR) is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>T</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method
You can instantiate this element when targeting a CPLD, but not when you are targeting an FPGA.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTCE
Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTCLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FTCLEX**

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Supported Architectures**

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR L CE T D C</td>
<td>Q</td>
</tr>
<tr>
<td>1 X X X X X</td>
<td>0</td>
</tr>
<tr>
<td>0 1 X X D ↑</td>
<td>D</td>
</tr>
<tr>
<td>0 0 0 X X X</td>
<td>No Change</td>
</tr>
<tr>
<td>0 0 1 0 X X</td>
<td>No Change</td>
</tr>
<tr>
<td>0 0 1 1 X ↑</td>
<td>Toggle</td>
</tr>
</tbody>
</table>

**Design Entry Method**

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTCP

Primitive: Toggle Flip-Flop with Asynchronous Clear and Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTCPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the toggle enable input (T) and the clock enable input (CE) are High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FTCPLE

Macro: Loadable Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset

Supported Architectures

This design element is supported in the following architectures:

• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction

This design element is a loadable toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the load input (L) is High, the clock enable input (CE) is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and the clock enable input (CE) are High and CLR, PRE, and L are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR: 1</td>
<td>PRE: X</td>
</tr>
<tr>
<td>CLR: 0</td>
<td>PRE: 1</td>
</tr>
<tr>
<td>CLR: 0</td>
<td>PRE: 0</td>
</tr>
<tr>
<td>CLR: 0</td>
<td>PRE: 0</td>
</tr>
<tr>
<td>CLR: 0</td>
<td>PRE: 0</td>
</tr>
<tr>
<td>CLR: 0</td>
<td>PRE: 0</td>
</tr>
<tr>
<td>CLR: 0</td>
<td>PRE: 0</td>
</tr>
</tbody>
</table>

Note: ↑ indicates a toggle or change state.
Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTDCE
Macro: Dual-Edge Triggered Toggle Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a dual edge triggered toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, clock transitions are ignored. This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table
<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes
<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTDCLE

Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
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<tbody>
<tr>
<td>CLR</td>
<td>L</td>
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<td>1</td>
<td>X</td>
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Design Entry Method

This design element is only for use in schematics.
Available Attributes

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<th>Attribute</th>
<th>Type</th>
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<th>Default</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTDCLEX

Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<td>0, 1</td>
<td>0</td>
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</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTDCP

Primitive: Dual-Edge Triggered Toggle Flip-Flop with Asynchronous Clear and Preset

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<tbody>
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<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
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</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTDRSE

Macro: Dual-Edge Triggered Toggle Flip-Flop with Synchronous Reset, Set, and Clock Enable

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a dual edge triggered toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and R is Low, clock enable input (CE) is overridden and output Q is set High. (Reset has precedence over Set.) When toggle enable input (T) and CE are High and R and S are Low, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<tbody>
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<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**FTDRSLE**

Macro: Dual-Edge Triggered Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set

![Diagram of FTDRSLE](image)

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock transitions. When R, S, and L are Low and CE is High, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.
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</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTP

Macro: Toggle Flip-Flop with Asynchronous Preset

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This design element is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When toggle-enable input (T) is High and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
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<td>PRE</td>
<td>T</td>
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Design Entry Method
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuity will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FTPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

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<th>Inputs</th>
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<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration. For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTPLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output (Q) is set High. When the load enable input (L) is High and (PRE) is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and (CE) are High, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

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<tr>
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<td>Sets the initial value of Q output after configuration. For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.</td>
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### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FTRSE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and (R) is Low, clock enable input (CE) is overridden and output (Q) is set High. (Reset has precedence over Set.) When toggle enable input (T) and (CE) are High and (R) and (S) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FTRSLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When R, S, and L are Low, CE is High and T is High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
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For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
FTSRE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input, when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset input (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When toggle enable input (T) and CE are High and S and R are Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

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<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

FTSRLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input (S), when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset (R) is High and (S) is Low, clock enable input (CE) is overridden and output (Q) is reset Low. When load enable input (L) is High and S and R are Low, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and (CE) are High and (S), (R), and (L) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>R</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

GND

Primitive: Ground-Connection Signal Tag

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
IBUF

Primitive: Input Buffer

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>Output</td>
<td>1</td>
<td>Buffer output</td>
</tr>
<tr>
<td>I</td>
<td>Input</td>
<td>1</td>
<td>Buffer input</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th>Method</th>
<th>Yes</th>
<th>Recommended</th>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
<td>Recommended</td>
<td>No</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element is usually inferred by the synthesis tool for any specified top-level input port to the design, and therefore it is generally not necessary to specify the element in source code. However, if desired, this element may be manually instantiated by copying the instantiation code from below and pasting it into the top-level entity/module of your code. Xilinx recommends that you put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet.</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>
**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- IBUF: Single-ended Input Buffer
-- All devices
-- Xilinx HDL Libraries Guide, version 13.1
IBUF_inst : IBUF
generic map (  
  IOSTANDARD => "DEFAULT")
port map (  
  O => O, -- Buffer output  
  I => I -- Buffer input (connect directly to top-level port)
);
-- End of IBUF_inst instantiation
```

**Verilog Instantiation Template**

```verilog
// IBUF: Single-ended Input Buffer
// All devices

IBUF #(  
  .IOSTANDARD("DEFAULT") // Specify the input I/O standard
) IBUF_inst (  
  .O(O), // Buffer output  
  .I(I) // Buffer input (connect directly to top-level port)
);
// End of IBUF_inst instantiation
```

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
IBUF16

Macro: 16-Bit Input Buffer

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element is usually inferred by the synthesis tool for any specified top-level input port to the design, and therefore it is generally not necessary to specify the element in source code. However, if desired, this element may be manually instantiated by copying the instantiation code from below and pasting it into the top-level entity/module of your code. Xilinx recommends that you put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet.</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

IBUF4

Macro: 4-Bit Input Buffer

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element is usually inferred by the synthesis tool for any specified top-level input port to the design, and therefore it is generally not necessary to specify the element in source code. However, if desired, this element may be manually instantiated by copying the instantiation code from below and pasting it into the top-level entity/module of your code. Xilinx recommends that you put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet.</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
IBUF8

Macro: 8-Bit Input Buffer

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element is usually inferred by the synthesis tool for any specified top-level input port to the design, and therefore it is generally not necessary to specify the element in source code. However, if desired, this element may be manually instantiated by copying the instantiation code from below and pasting it into the top-level entity/module of your code. Xilinx recommends that you put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet.</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
INV

**Primitive: Inverter**

![Inverter Symbol]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a single inverter that identifies signal inversions in a schematic.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
INV16

Macro: 16 Inverters

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
INV4

Macro: Four Inverters

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method
This design element is only for use in schematics.

For More Information
• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
INV8

Macro: Eight Inverters

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

IOBUFE

Primitive: Bi-Directional Buffer

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a bi-directional buffer that is a composite of the IBUF and OBUFE elements. The O output is X (unknown) when IO (input/output) is Z. You can also implement JOBUFEs as interconnections of their component elements.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>E</th>
<th>I</th>
<th>IO</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Z</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Z</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th></th>
<th>Instantiation</th>
<th>Inference</th>
<th>CORE Generator™ and wizards</th>
<th>Macro support</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Yes</td>
<td>Recommended</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
KEEPER

Primitive: KEEPER Symbol

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>Output</td>
<td>1-Bit</td>
<td>Keeper output</td>
</tr>
</tbody>
</table>

Design Entry Method

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>No</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element can be connected to a net in the following locations on a top-level schematic file:
• A net connected to an input IO Marker
• A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.
**VHDL Instantiation Template**

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- KEEPER: I/O Buffer Weak Keeper
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
KEEPER_inst : KEEPER
port map (O => O -- Keeper output (connect directly to top-level port));

-- End of KEEPER_inst instantiation
```

**Verilog Instantiation Template**

// KEEPER: I/O Buffer Weak Keeper
// All FPGA, CoolRunner-II
KEEPER_KEEPER_inst (O(O) // Keeper output (connect directly to top-level port));

// End of KEEPER_inst instantiation

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LD

Primitive: Transparent Data Latch

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>↓</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LD16

Macro: Multiple Transparent Data Latch

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element has 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>Dn</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>↓</td>
<td>Dn</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 16-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LD4

Macro: Multiple Transparent Data Latch

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This design element has four transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>Dn</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>↓</td>
<td>Dn</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 4-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LD8

Macro: Multiple Transparent Data Latch

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element has 8 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>Dn</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>↓</td>
<td>Dn</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>Any 8-Bit Value</td>
<td>All zeros</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LDC

Primitive: Transparent Data Latch with Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input is High and (CLR) is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>G</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LDCP

Primitive: Transparent Data Latch with Asynchronous Clear and Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

The design element is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. For XC9500 devices, when PRE is High and CLR is low, it presets the data (Q) output High. For CoolRunner™-II and CoolRunner™ XPLA3, PRE is a lower precedence than the gate (G) or data (D) inputs, and so has no influence on them. Q reflects the data (D) input while the gate (G) input is High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>PRE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Integer</td>
<td>0, 1</td>
<td>0</td>
<td>Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LDG

Primitive: Transparent Datagate Latch

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a transparent DataGate latch used for gating input signals to decrease power dissipation. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device’s DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>↑</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>0</td>
<td>Sets the initial value of Q output after configuration</td>
</tr>
</tbody>
</table>
For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

LDG16

Macro: 16-bit Transparent Datagate Latch

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element has 16 transparent DataGate latches with a common gate enable (G). These latches are used to gate input signals in order to decrease power dissipation during periods when activity on the input pins is not of interest to the CPLD. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device's DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>↑</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LDG4

Macro: 4-Bit Transparent Datagate Latch

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element has 4 transparent DataGate latches with a common gate enable (G). These latches are used to gate input signals in order to decrease power dissipation during periods when activity on the input pins is not of interest to the CPLD. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device’s DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>↑</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LDG8

Macro: 8-Bit Transparent Datagate Latch

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element has 8 transparent DataGate latches with a common gate enable (G). These latches are used to gate input signals in order to decrease power dissipation during periods when activity on the input pins is not of interest to the CPLD. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device’s DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>G</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>↑</td>
<td>D</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
LDP

Primitive: Transparent Data Latch with Asynchronous Preset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a transparent data latch with asynchronous preset (PRE). For XC9500 devices, when PRE is High it overrides the other inputs and presets the data (Q) output High. For CoolRunner™-II and CoolRunner™ XPLA3, PRE is a lower precedence than the gate (G) or data (D) inputs, and so has no influence on them. Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRE</td>
<td>G</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>↓</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>Binary</td>
<td>0, 1</td>
<td>1</td>
<td>Specifies the initial value upon power-up or the assertion of GSR for the Q port.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
M16_1E

Macro: 16-to-1 Multiplexer with Enable

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 : D0) under the control of the select inputs (S3 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>S3</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
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<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
M2_1

Macro: 2-to-1 Multiplexer

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>D1</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

M2_1B1
Macro: 2-to-1 Multiplexer with D0 Inverted

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of (D0). When S0 is High, (O) reflects the state of D1.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>D1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

For More Information
• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
M2_1B2

Macro: 2-to-1 Multiplexer with D0 and D1 Inverted

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of D0. When S0 is High, O reflects the inverted value of D1.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>D1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
M2_1E

Macro: 2-to-1 Multiplexer with Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When Low, S0 selects D0 and when High, S0 selects D1. When (E) is Low, the output is Low.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>S0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
M4_1E

Macro: 4-to-1 Multiplexer with Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>S1</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
M8_1E

Macro: 8-to-1 Multiplexer with Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 : D0) under the control of the select inputs (S2 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>E</th>
<th>S2</th>
<th>S1</th>
<th>S0</th>
<th>D7-D0</th>
<th>Outputs</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>D0</td>
<td>D0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>D1</td>
<td>D1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>D2</td>
<td>D2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
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Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND2

Primitive: 2-Input NAND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND2B1

Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND2B2

Primitive: 2-Input NAND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND3

Primitive: 3-Input NAND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND3B1

Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

NAND3B2

Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND3B3

Primitive: 3-Input NAND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND4

Primitive: 4-Input NAND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND4B1

Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND4B2

Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND4B3

Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND4B4

Primitive: 4-Input NAND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

NAND5

Primitive: 5-Input NAND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND5B1

Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND5B2

Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND5B3

Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND5B4

Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
NAND5B5

Primitive: 5-Input NAND Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND6

Macro: 6-Input NAND Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

NAND7
Macro: 7-Input NAND Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND8

Macro: 8-Input NAND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NAND9

Macro: 9-Input NAND Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR2

Primitive: 2-Input NOR Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR2B1

Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR2B2

Primitive: 2-Input NOR Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

NOR3

Primitive: 3-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR3B1

Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR3B2

Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR3B3

Primitive: 3-Input NOR Gate with Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR4

Primitive: 4-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR4B1

Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR4B2

Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR4B3

Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR4B4

Primitive: 4-Input NOR Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR5

Primitive: 5-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR5B1

Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR5B2

Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR5B3

Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR5B4

Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR5B5

Primitive: 5-Input NOR Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR6

Macro: 6-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR7

Macro: 7-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR8

Macro: 8-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
NOR9

Macro: 9-Input NOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

**OBUF**

*Primitive: Output Buffer*

![OBUF Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

**Port Descriptions**

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>Output</td>
<td>1</td>
<td>Output of OBUF to be connected directly to top-level output port.</td>
</tr>
<tr>
<td>I</td>
<td>Input</td>
<td>1</td>
<td>Input of OBUF. Connect to the logic driving the output port.</td>
</tr>
</tbody>
</table>

**Design Entry Method**

<table>
<thead>
<tr>
<th>Method</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.

**Available Attributes**

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>
VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```vhdl
Library UNISIM;
use UNISIM.vcomponents.all;

-- OBUF: Single-ended Output Buffer
-- All devices
-- Xilinx HDL Libraries Guide, version 13.1
OBUF_inst: OBUF
  generic map (SLEW => "SLOW")
  port map (O => O, -- Buffer output (connect directly to top-level port)
            I => I  -- Buffer input)

-- End of OBUF_inst instantiation
```

Verilog Instantiation Template

```verilog
// OBUF: Single-ended Output Buffer
// All devices
OBUF #( .SLEW("SLOW") // Specify the output slew rate
        ) OBUF_inst (
          .O(O), // Buffer output (connect directly to top-level port)
          .I(I)  // Buffer input
        );

// End of OBUF_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

OBUF16

Macro: 16-Bit Output Buffer

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Supported Architectures

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUF4

Macro: 4-Bit Output Buffer

Supported Architectures
This design element is supported in the following architectures:
• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction
This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LV TTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information
• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
OBUF8

Macro: 8-Bit Output Buffer

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUF

Macro: 3-State Output Buffer with Active-High Output Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I, output O, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUFE16

Macro: 16-Bit 3-State Output Buffer with Active-High Output Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I15-I0, output O15-O0, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUFE4

Macro: 4-Bit 3-State Output Buffer with Active-High Output Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I3-I0, output O3-O0, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUF8

Macro: 8-Bit 3-State Output Buffer with Active-High Output Enable

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a 3-state buffer with input I7-I0, output O7-O0, and active-High output enable (E).
When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>I</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUFT

**Primitive: 3-State Output Buffer with Active Low Output Enable**

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>I</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Port Descriptions

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>Output</td>
<td>1</td>
<td>Buffer output (connect directly to top-level port)</td>
</tr>
<tr>
<td>I</td>
<td>Input</td>
<td>1</td>
<td>Buffer input</td>
</tr>
<tr>
<td>T</td>
<td>Input</td>
<td>1</td>
<td>3-state enable input</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th>Method</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>Recommended</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>
This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

### Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

### VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

Library UNISIM;
use UNISIM.vcomponents.all;

```
-- OBUFT: Single-ended 3-state Output Buffer
-- All devices
-- Xilinx HDL Libraries Guide, version 13.1

OBUFT_inst : OBUFT
port map ( 
  O => O,   -- Buffer output (connect directly to top-level port)
  I => I,   -- Buffer input
  T => T    -- 3-state enable input
);

-- End of OBUFT_inst instantiation
```

### Verilog Instantiation Template

```
// OBUFT: Single-ended 3-state Output Buffer
// All devices

OBUFT OBUFT_inst ( 
  .O(O),  // Buffer output (connect directly to top-level port)
  .I(I),  // Buffer input
  .T(T)   // 3-state enable input
);

// End of OBUFT_inst instantiation
```

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

OBUFT16

Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>I</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUFT4

Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>T I O</td>
<td></td>
</tr>
<tr>
<td>T I O</td>
<td></td>
</tr>
<tr>
<td>1 X Z</td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td></td>
</tr>
<tr>
<td>0 0 0</td>
<td></td>
</tr>
</tbody>
</table>

Design Entry Method
This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>&quot;DEFAULT&quot;</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OBUFT8

Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>I</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

Available Attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Type</th>
<th>Allowed Values</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOSTANDARD</td>
<td>String</td>
<td>See Data Sheet</td>
<td>“DEFAULT”</td>
<td>Assigns an I/O standard to the element.</td>
</tr>
</tbody>
</table>

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR2

Primitive: 2-Input OR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR2B1

Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR2B2

Primitive: 2-Input OR Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR3

Primitive: 3-Input OR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR3B1

Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

OR3B2

Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR3B3

Primitive: 3-Input OR Gate with Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR4

Primitive: 4-Input OR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR4B1

Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR4B2

Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR4B3

Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR4B4

Primitive: 4-Input OR Gate with Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**OR5**

**Primitive: 5-Input OR Gate with Non-Inverted Inputs**

**Supported Architectures**

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR5B1

Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

• XC9500
• CoolRunner™-II
• CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
OR5B2

Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**OR5B3**

Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs

![OR5B3 Diagram](image)

### Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

### Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR5B4

Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR5B5

Primitive: 5-Input OR Gate with Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR6

Macro: 6-Input OR Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR7

Macro: 7-Input OR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR8

Macro: 8-Input OR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
OR9

Macro: 9-Input OR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>Output</td>
<td>1</td>
<td>Pulldown output (connect directly to top level port)</td>
</tr>
</tbody>
</table>

Design Entry Method

<table>
<thead>
<tr>
<th>Instantiation</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inference</td>
<td>No</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker.
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
PULLUP

Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

Supported Architectures

This design element is supported in the following architectures:
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Width</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>Output</td>
<td>1</td>
<td>Pullup output (connect directly to top level port)</td>
</tr>
</tbody>
</table>

Design Entry Method

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiation</td>
<td>Yes</td>
</tr>
<tr>
<td>Inference</td>
<td>No</td>
</tr>
<tr>
<td>CORE Generator™ and wizards</td>
<td>No</td>
</tr>
<tr>
<td>Macro support</td>
<td>No</td>
</tr>
</tbody>
</table>

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element can be connected to a net in the following locations on a top-level schematic file:
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.
VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- PULLUP: I/O Buffer Weak Pull-up
-- CoolRunner-II
-- Xilinx HDL Libraries Guide, version 13.1
PULLUP_inst : PULLUP
port map (  
  O => O -- Pullup output (connect directly to top-level port)
);
-- End of PULLUP_inst instantiation
```

Verilog Instantiation Template

```
// PULLUP: I/O Buffer Weak Pull-up
// All FPGA, CoolRunner-II
PULLUP PULLUP_inst (  
  .O(O) -- Pullup output (connect directly to top-level port)
);
// End of PULLUP_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR16CE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit width - 1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR16CLED

Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR16RE
Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>CE</th>
<th>SLI</th>
<th>C</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>Q0</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>No Change</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>SLI</td>
<td>↑</td>
<td>SLI</td>
</tr>
</tbody>
</table>

$z = \text{bitwidth} -1$

$qn-1 = \text{state of referenced output one setup time prior to active clock transition}$

Design Entry Method
This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR16RLED

Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right ) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

## Design Entry Method

This design element is only for use in schematics.

## For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR4CE
Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bit width - 1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**SR4CLED**

Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear

![Diagram of SR4CLED]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

*qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition.*

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR4RE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bitwidth -1
q0-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

SR4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bitwidth} - 1 \]

\[ qn-1 = \text{state of referenced output one setup time prior to active clock transition} \]

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR4RLED

Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
<td>CE</td>
<td>LEFT</td>
<td>SLI</td>
<td>SRI</td>
<td>D3 : D0</td>
<td>C</td>
<td>Q0</td>
<td>Q3</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>D3 : D0</td>
<td>↑</td>
<td>D0</td>
<td>D3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>SLI</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>SLI</td>
<td>q2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>SRI</td>
<td>X</td>
<td>↑</td>
<td>q1</td>
<td>SRI</td>
</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR8CE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ z = \text{bit width} - 1 \]
\[ qn-1 = \text{state of referenced output one setup time prior to active clock transition} \]

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn-D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SL1→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
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</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

SR8CLED

Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
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</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.


**SR8RE**

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

![SR8RE Diagram]

### Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

### Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

### Logic Table

| Inputs | Outputs | | |
|---|---|---|---|---|---|
| R | CE | SLI | C | Q0 | Qn : Q1 |
| 1 | X | X | ↑ | 0 | 0 |
| 0 | 0 | X | X | No Change | No Change |
| 0 | 1 | SLI | ↑ | SLI | qn-1 |

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

### Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SR8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
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<tr>
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</tbody>
</table>

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

SR8RLED

Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right ) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
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<td>1</td>
<td>X</td>
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<tr>
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</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD16CE

Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
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<td>X</td>
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<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

SRD16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn:D0 inputs is loaded into the corresponding Qn:Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
## Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
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<tbody>
<tr>
<td>CLR</td>
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</tbody>
</table>

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD16CLED

Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
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</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
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<td>X</td>
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<tr>
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</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD16RE

Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
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<tr>
<td>1</td>
<td>X</td>
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<tr>
<td>1</td>
<td>X</td>
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<td>1</td>
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</tbody>
</table>

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition
Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
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<tbody>
<tr>
<td>R</td>
<td>L</td>
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<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bitwidth -1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD16RLED

Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, etc.) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
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</tr>
</thead>
<tbody>
<tr>
<td>R</td>
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</tr>
<tr>
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<td>X</td>
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<tr>
<td>1</td>
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</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD4CE

Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
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</tr>
</tbody>
</table>

\( z = \text{bitwidth} - 1 \)

\( qn-1 = \text{state of referenced output one setup time prior to active clock transition} \)

Design Entry Method

This design element is only for use in schematics.
For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
SRD4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn:D0 inputs is loaded into the corresponding Qn:Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
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<tbody>
<tr>
<td>CLR:0</td>
<td>Q0:0</td>
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<tr>
<td>CLR:1</td>
<td>Q0:0</td>
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<tr>
<td>CLR:0</td>
<td>Q0:0</td>
</tr>
<tr>
<td>CLR:0</td>
<td>Q0:0</td>
</tr>
<tr>
<td>CLR:0</td>
<td>Q0:0</td>
</tr>
<tr>
<td>CLR:0</td>
<td>Q0:0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLR</th>
<th>L</th>
<th>CE</th>
<th>SLI</th>
<th>Dn:D0</th>
<th>C</th>
<th>Q0</th>
<th>Qz:Q1</th>
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<td>SLI</td>
<td>X</td>
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<td>SLI</td>
<td>qn-1</td>
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<tr>
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<td>0</td>
<td>1</td>
<td>SLI</td>
<td>X</td>
<td>↓</td>
<td>SLI</td>
<td>qn-1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>No Change</td>
<td>No Change</td>
</tr>
</tbody>
</table>

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD4CLED

Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

q1n-1 and qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

SRD4RE

Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition
Design Entry Method

This design element is only for use in schematics.

For More Information

• See the appropriate CPLD User Guide.
• See the appropriate CPLD Data Sheets.
**SRD4RLE**

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

![SRD4RLE Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bitwidth} - 1 \]

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**SRD4RLED**

Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, etc.) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD8CE

Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures
This design element is supported in the following architectures:
CoolRunner™-II

Introduction
This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bitwidth - 1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method
This design element is only for use in schematics.
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:
CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn:D0 inputs is loaded into the corresponding Qn:Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
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<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ z = \text{bitwidth} - 1 \]

\[ qn-1 = \text{state of referenced output one setup time prior to active clock transition} \]

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD8CLED

Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Chapter 3: About Design Elements

Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>Q0</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
</tr>
<tr>
<td>CE</td>
<td>D0</td>
</tr>
<tr>
<td>LEFT</td>
<td>No Change</td>
</tr>
<tr>
<td>SLI</td>
<td>X</td>
</tr>
<tr>
<td>SRI</td>
<td>X</td>
</tr>
<tr>
<td>D7:D0</td>
<td>X</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLR</th>
<th>L</th>
<th>CE</th>
<th>LEFT</th>
<th>SLI</th>
<th>SRI</th>
<th>D7:D0</th>
<th>C</th>
<th>Q0</th>
<th>Q7</th>
<th>Q6:Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>D7:D0</td>
<td>↑</td>
<td>D0</td>
<td>D7</td>
<td>Dn</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>D7:D0</td>
<td>↓</td>
<td>D0</td>
<td>D7</td>
<td>Dn</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
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<td>No Change</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>SLI</td>
<td>X</td>
<td>X</td>
<td>↑</td>
<td>SLI</td>
<td>q6</td>
<td>qn-1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>SLI</td>
<td>X</td>
<td>X</td>
<td>↓</td>
<td>SLI</td>
<td>q6</td>
<td>qn-1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>SRI</td>
<td>X</td>
<td>↑</td>
<td>q1</td>
<td>SRI</td>
<td>qn+1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>SRI</td>
<td>X</td>
<td>↓</td>
<td>q1</td>
<td>SRI</td>
<td>qn+1</td>
</tr>
</tbody>
</table>

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
**SRD8RE**

Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

![SRD8RE Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

CoolRunner™-II

**Introduction**

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

**Logic Table**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition
Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

z = bitwidth -1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
SRD8RLED

Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Supported Architectures

This design element is supported in the following architectures:

CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, etc.) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.
### Logic Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R )</td>
<td>( L )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\( qn-1 \) or \( qn+1 \) = state of referenced output one setup time prior to active clock transition

### Design Entry Method

This design element is only for use in schematics.

### For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
VCC

Primitive: VCC-Connection Signal Tag

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element serves as a signal tag, or parameter, that forces a net or input function to a logic High level. A net tied to this element cannot have any other source.

When the placement and routing software encounters a net or input function tied to this element, it removes any logic that is disabled by the Vcc signal, which is only implemented when the disabled logic cannot be removed.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR2

Primitive: 2-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>I0 ... I2</td>
<td>O</td>
</tr>
<tr>
<td>Odd number of 1</td>
<td>0</td>
</tr>
<tr>
<td>Even number of 1</td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR3

Primitive: 3-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>I0 ... Iz</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>Odd number of 1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>Even number of 1</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR4

Primitive: 4-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR5

Primitive: 5-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR6

Macro: 6-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR7

Macro: 7-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR8

Macro: 8-Input XNOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XNOR9

Macro: 9-Input XNOR Gate with Non-Inverted Inputs

![XNOR9 Diagram]

**Supported Architectures**

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

**Introduction**

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

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</table>

**Design Entry Method**

This design element is only for use in schematics.

**For More Information**

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

XOR2

Primitive: 2-Input XOR Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XOR3

Primitive: 3-Input XOR Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
Chapter 3: About Design Elements

XOR4

Primitive: 4-Input XOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XOR5

Primitive: 5-Input XOR Gate with Non-Inverted Inputs

 Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XOR6

Macro: 6-Input XOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XOR7

Macro: 7-Input XOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XOR8

Macro: 8-Input XOR Gate with Non-Inverted Inputs

Supported Architectures
This design element is supported in the following architectures:
- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction
XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method
This design element is only for use in schematics.

For More Information
- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.
XOR9

Macro: 9-Input XOR Gate with Non-Inverted Inputs

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.