RTL Design and IP Generation Tutorial

PlanAhead Design Tool

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XILINX®

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RTL Design and IP Generation Tutorial

This tutorial provides an overview of the Register Transfer Level (RTL) development and analysis environment, in which you will:

- Import RTL sources and review them using the Text Editor
- Run Behavioral Simulation on the bft module
- Run elaboration to compile the RTL
- Use a variety of RTL analysis features to explore your compiled RTL design. These include:
- Analyze the RTL logic hierarchy using the RTL schematic
- Estimate RTL resources
- Run RTL Design Rules Checks (DRCs)
- Browse the Xilinx® IP Catalog, and customize and implement an Intellectual Property (IP) core in the design

Many of the PlanAhead™ software analysis features are covered in more detail in other tutorials. Not every command or command option is covered.

The objective of this tutorial is to familiarize you with the RTL development and analysis process using the PlanAhead tool.

Software Requirements

The PlanAhead tool is installed with ISE® Design Suite software. Before starting the tutorial, be sure that the PlanAhead tool is operational, and that the tutorial design data is installed.

For installation instructions and information, see the ISE Design Suite: *Installation and Licensing Guide (UG798)* at http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_4/iil.pdf.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller xc6vlx75t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Tutorial Design Description

The small sample design used in this tutorial has a set of RTL design sources consisting of Verilog and VHDL. The VHDL sources are from multiple VHDL libraries. The design used throughout this tutorial targets an xc6vlx75t device and contains:

- A RISC processor
- A pseudo FFT
- Gigabit transceivers
- Two USB port modules

Locating Tutorial Design Files

Download the `PlanAhead_Tutorial.zip` file from the Xilinx website:

http://www.xilinx.com/support/documentation/dt_planahead_planahead13-4_tutorials.htm

Extract the zip file contents into any write-accessible location.

The unzipped `PlanAhead_Tutorial` data directory is referred to in this tutorial as `<Extract_Dir>`.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data is required each time you run the tutorial.

Step 1: Creating a New RTL Project

The PlanAhead tool enables you to create several project types depending on where in the design flow the tool is being used. RTL sources can be used to create a project for development and analysis, synthesis, implementation, and bit file creation.

Opening the PlanAhead Tool

Open the PlanAhead tool:

- On Windows, select the **Xilinx PlanAhead 13.4** desktop icon or **Start > Programs > Xilinx ISE Design Suite 13.2 > PlanAhead > PlanAhead**.
- On Linux, change the directory to `<Extract_Dir>/PlanAhead_Tutorial/Tutorial_Created_Data`, and type **planAhead**.

The PlanAhead Getting Started Help page opens.

Figure 1: Getting Started Page

The PlanAhead Getting Started page contains links to open or create projects, and view the documentation.

Creating a New RTL Project

1. Create a new project called project_rtl, using the RTL source files in:

   `<Extract_Dir>\PlanAhead_Tutorial\Sources\hdl` directory.

2. On the Getting Started page, select the **Create New Project** link.
3. In the **Create a New PlanAhead Project** confirmation dialog box, click **Next.**

   The Project Name page of the New Project wizard opens:

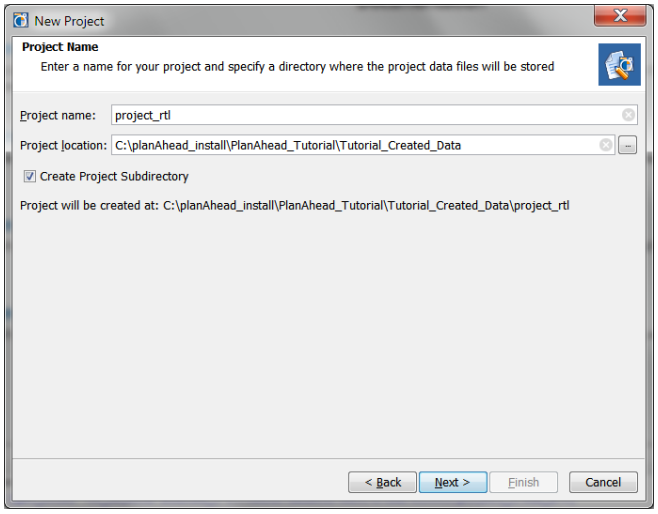

Figure 2: Entering the New Project Name

4. Browse to, and select `<Extract_Dir>\PlanAhead_Tutorial\Tutorial_Created_Data`.
5. Enter the Project name: **project_rtl**, and click **Next**.

   The Design Source page opens.

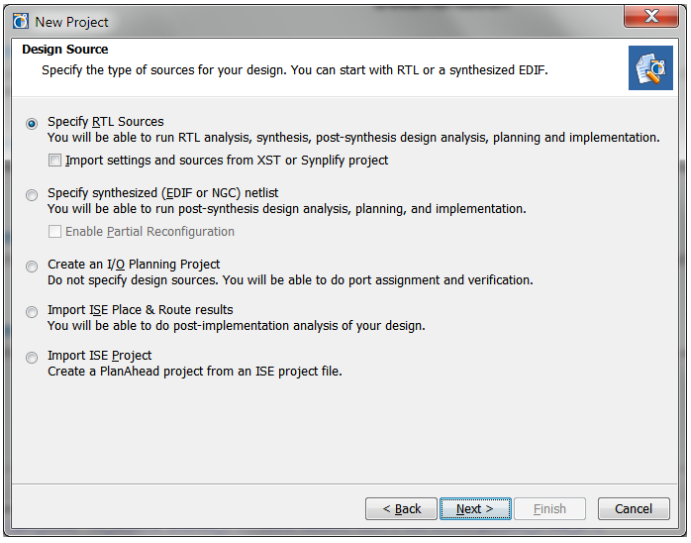

Figure 3: New Project: Design Source Dialog Box

6. Select Specify RTL Sources, and click **Next**.

   The Add Sources page opens:

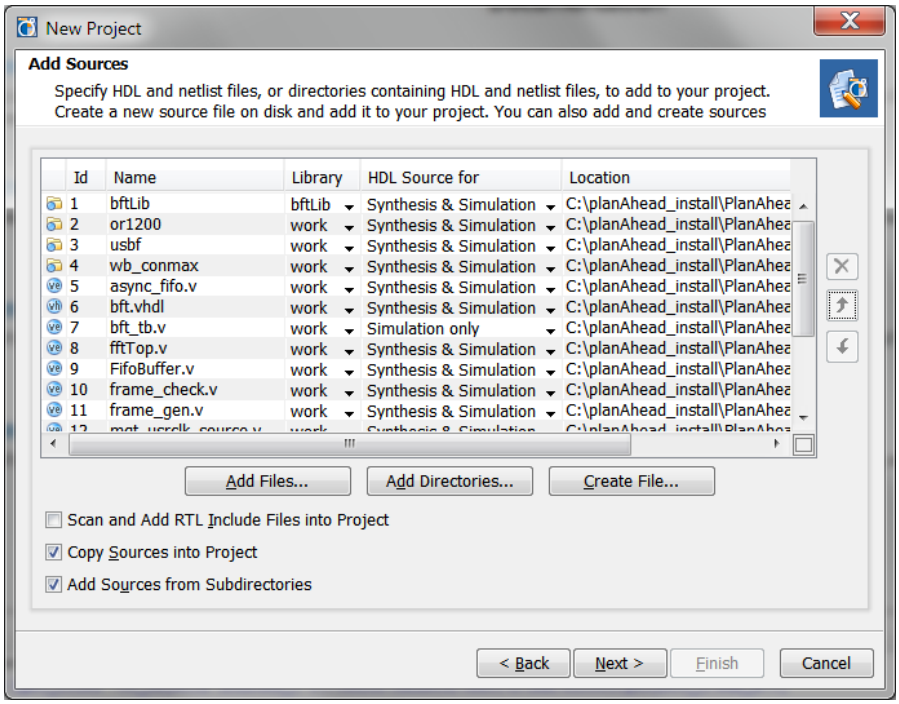

Figure 4: New Project: Add Sources Dialog Box

Adding Directories and Files

1. Click **Add Directories ,** browse to, : `<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl`, and select the bftLib, or1200, usbf, and wb_conmax directories.

2. Click Add Files, browse to `<Extract_Dir>/PlanAhead_Tutorial/Sources/hdl`, and add all of the source files listed (select a file and use Ctrl+A to select all of the source files).

3. Verify that the following checkboxes are selected:

3. Copy Sources into Project.

4. Add Sources from Subdirectories.

5. Modify the Library for the bftLib folder by select the work Library and typing bftLib

6. Update **HDL Source for** of bft_tb.v to **Simulation only** by selecting it from the drop down menu.

7. Be sure the page is identical to the previous figure (*New Project: Add Sources Dialog Box*) , and click **Next**.

   The Add Existing IP page opens.

8. Click **Next**.

   The Add Constraints Files page opens:

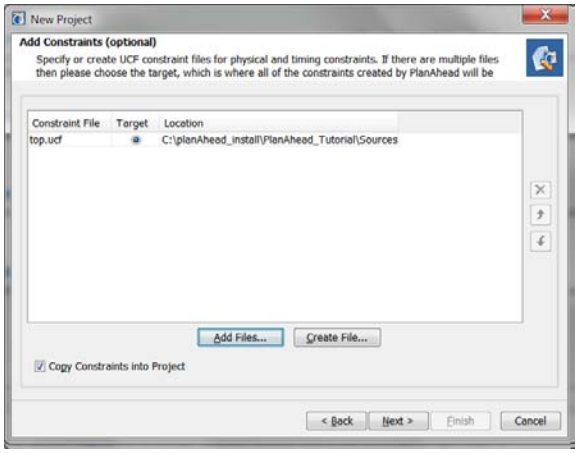

Figure 5: Selecting Constraint Files to Add to the Project

Adding a Constraints File

1. Click **Add Files** and browse to select the following file:

   `<Extract_Dir>/PlanAhead_Tutorial/Sources/top.ucf`

2. Click **OK**.
3. Ensure the **Copy Constraints into Project** option is set to on, and click **Next**.

   The Default Part page opens.

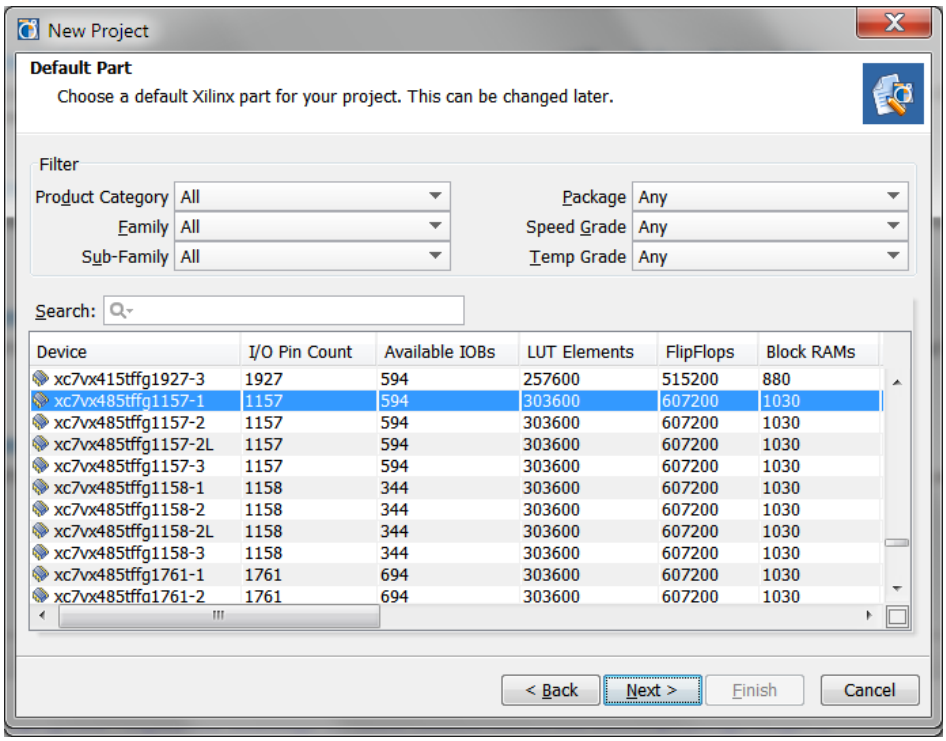

Figure 6: New Project: Default Part Dialog Window

Selecting a Default Part

1. In the Filter section, click the **Family** pull-down menu, and select **Virtex6.** The list is filtered to only show Virtex®-6 devices
2. Click the **Sub-Family** pull-down menu, and select **Virtex6 LXT**. The list is filtered to only show Virtex-6 LXT devices.
3. In the Search field type **75t**. The 75t devices are listed.

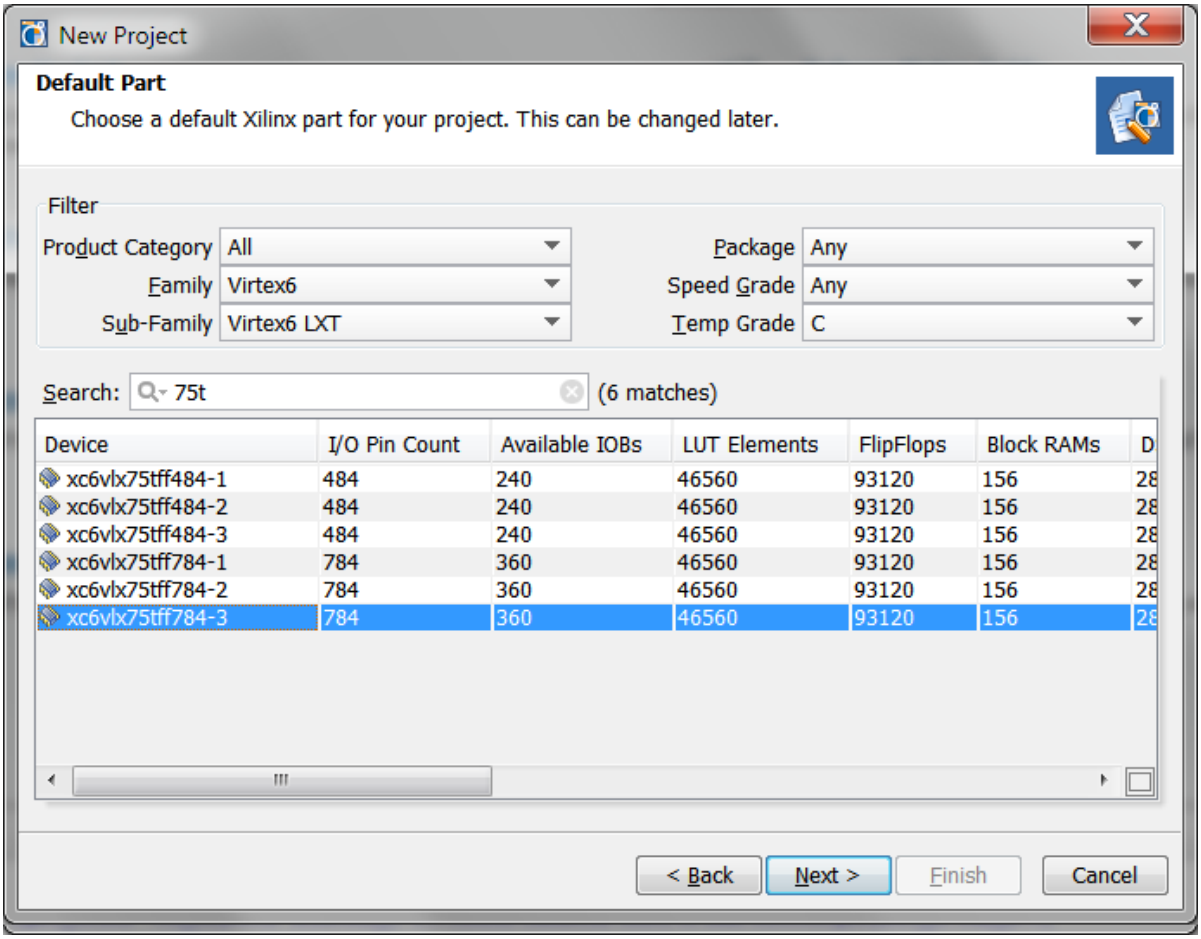

Figure 7: Selecting a Family and Default Part

4. Select **xc6vlx75tff784-3** and click **Next**.
5. Review the New Project Summary page, and click **Finish**.

   The PlanAhead environment opens.

Step 2: Using the Sources View and the Text Editor

The PlanAhead tool allows different file types to be added as design sources, including Verilog, VHDL, and NGC format cores. The files display by category in the Sources view. Use the supplied text editor to create or modify RTL sources.

Exploring the Sources View and Project Summary

1. Examine the information in the Project Summary. More information displays as the design progresses.

2. Examine the Sources view.

3. The source hierarchy is displayed by default, to explore the hierarchy, click the plus/minus signs (**+/-**) to expand and collapse it.

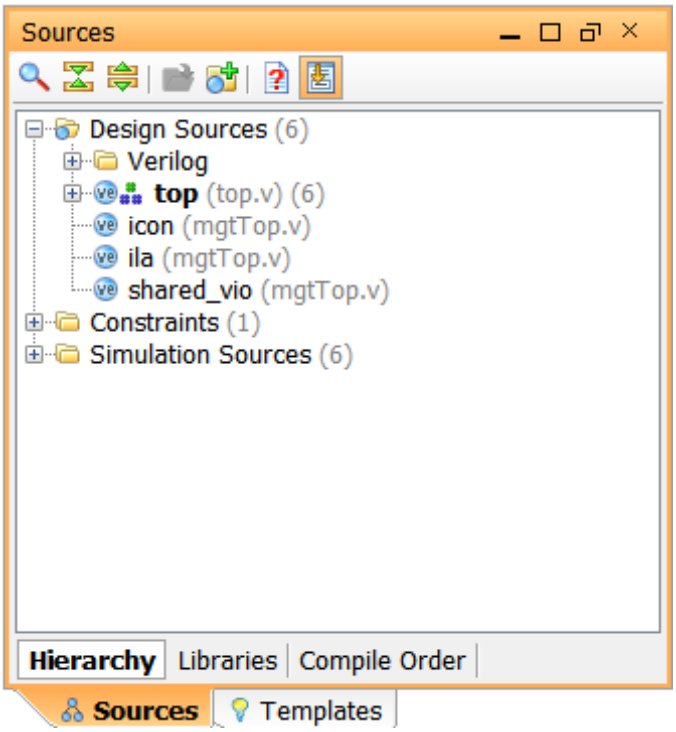

Figure 8: Viewing Sources Hierarchy

4. Click the **Libraries** tab and filter the Design Sources clicking the Search toolbar button and typing time. Select timescale.v, and view the information in the **Source File Properties** view. Change the Type to **Verilog Header** and click the Apply button. Click the Search toolbar button again to restore the full source view.

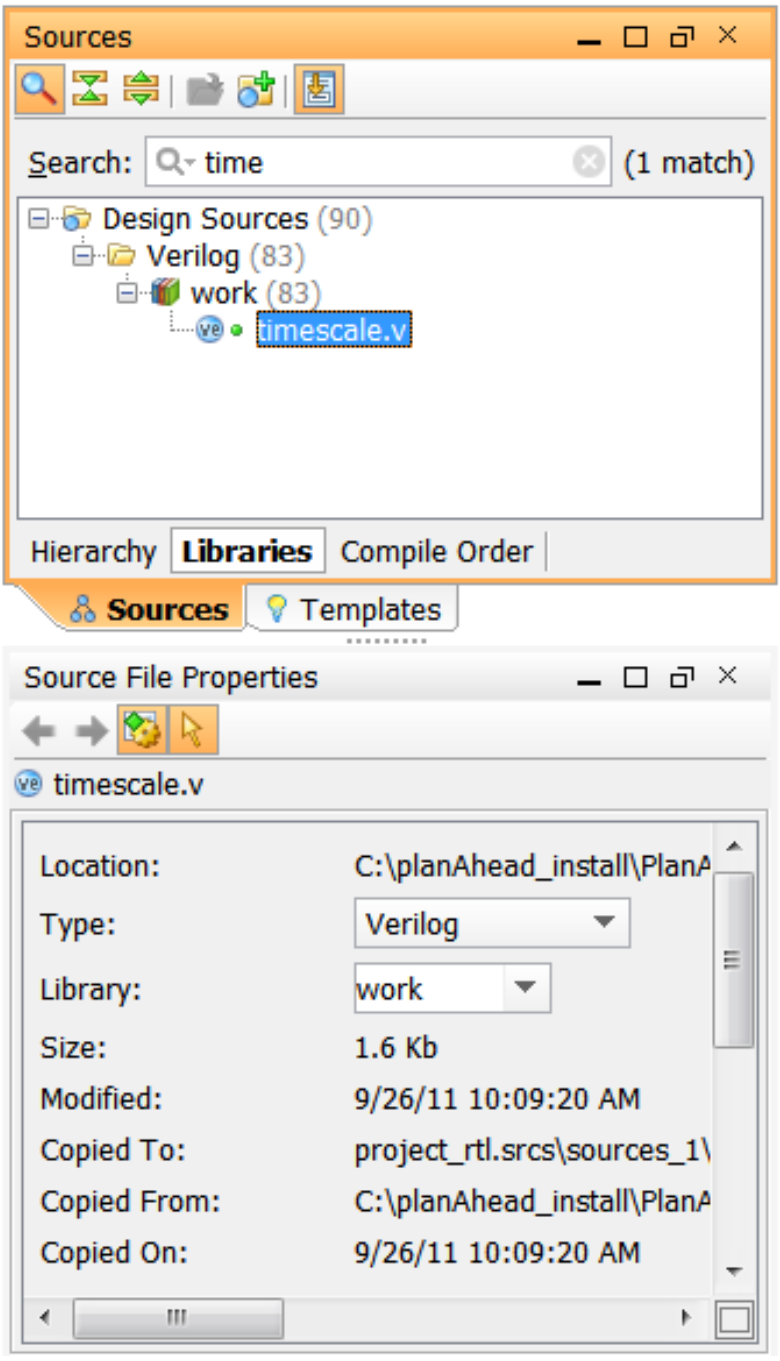

Figure 9: Viewing the Source File Properties

Verifying the bftLib VHDL Library

1. In the Sources view, click the sources tab and Libraries sub tab. Click the collapse all toolbar button to condense the source files displayed.
2. Click the Plus sign (expand) next to the VHDL folder to see its contents.
3. Expand the bftLib folder and verify following files are shown under it:

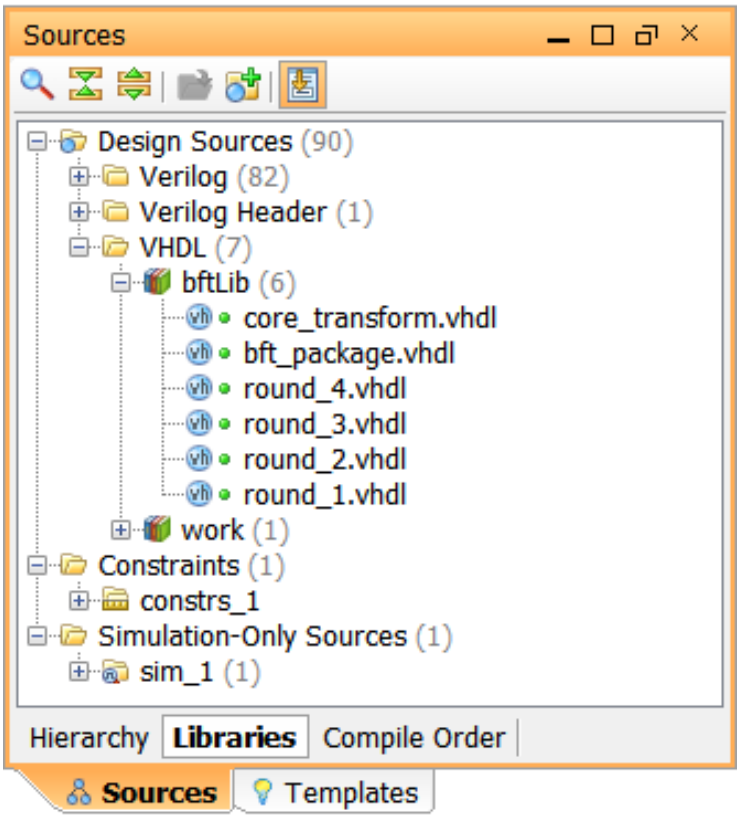

Figure 10: Verifying a VHDL Library

Identifying Simulation Source Files

1. In the Sources view, Libraries tab, expand the Verilog folder and the work subfolder under Simulation Only Sources.

2. Expand the Unreferenced folder and you should see the **bft_tb.v** source file that was set as Simulation Only during project creation and select **Move to Simulation Sources**) .

3. If bft_tb is not listed under simulation sources, use search to find it, select bft_tb.v, right-click on it and select **Move to Simulation Sources** from the context menu.

   The file is shown under the **Simulation-Only Sources** folder (it will become a reference file when it is set as the top file for simulation in a later step).

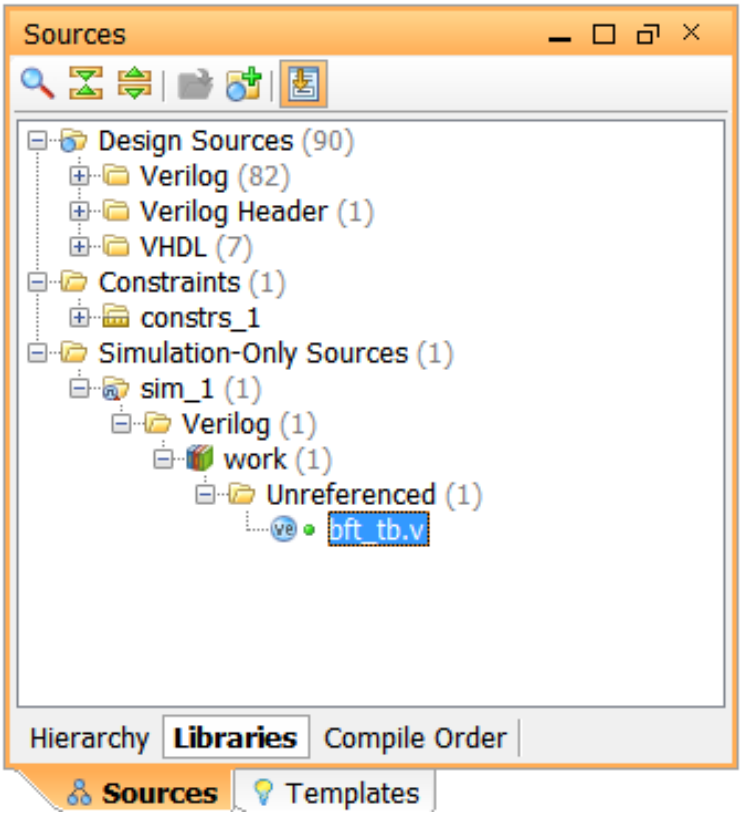

Figure 11: Viewing the Simulation-Only Sources

Exploring the Sources View Commands

1. Select one of the VHDL sources in the Sources view.
2. Right-click in the Sources view to review the available popup commands. To dismiss it, press the **Esc** key.

Using the Text Editor to View Source File Content

1. In the Sources view, double-click a VHDL source file to open it in the Text Editor.
2. Right-click in the Text Editor to view the available popup commands.
3. Select the **Find in Files** popup menu to open the **Find in Files** dialog box.

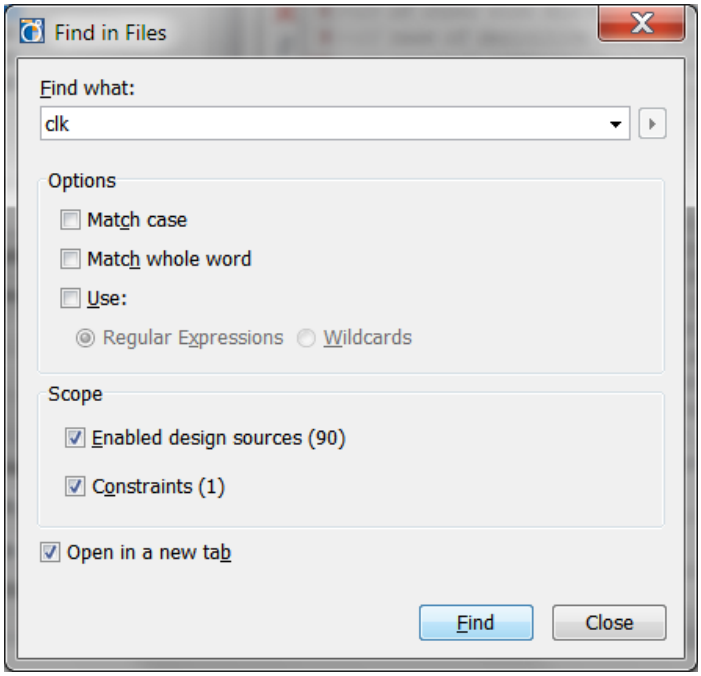

Figure 12: Using the Find in Files Command

4. Type **clk** and click **Find (**Click **Yes** when prompted to continue the search).

   The Find in Files view displays in the messaging area at the bottom of the PlanAhead environment.

5. In the **Find in Files** view, expand and select one of the occurrences of **clk**.

   The Text Editor now displays the file and occurrence.

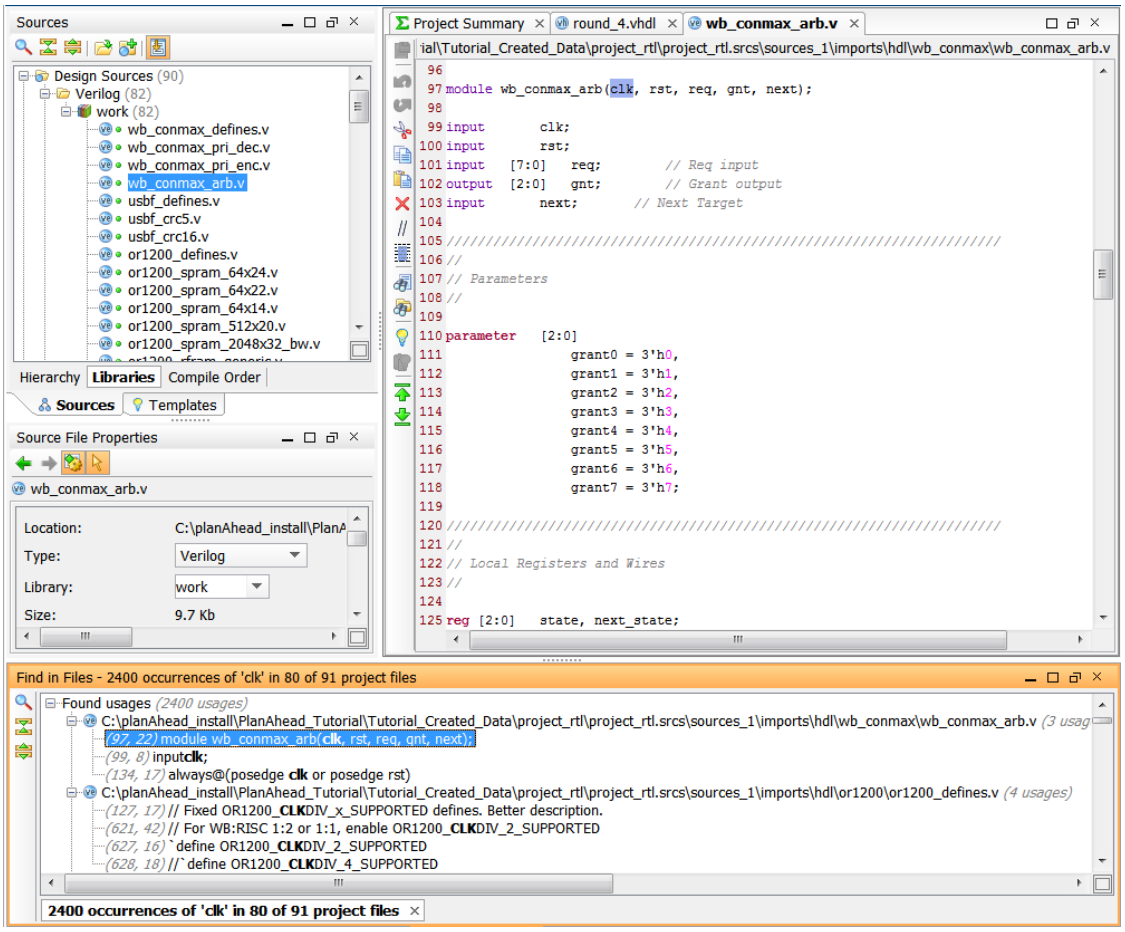

Figure 13: Viewing the Find in Files Results

6. Close the **Find in Files** view.
7. Close each of the open RTL file tabs in the Text Editor.

Creating a New RTL Source File and Importing a Template

The PlanAhead tool enables you to create new Verilog or VHDL source files. Standard Xilinx templates can be used as a starting point for a variety of logic and code constructs.

1. In the Flow Navigator under Project Manager, select **Add Sources**.
2. In the Add Sources dialog box, select **Add or Create Design Sources**, and click **Next**.
3. Click **Create File…** button in the Add or Create Design Sources dialog box.

   The Create Source File dialog box opens:

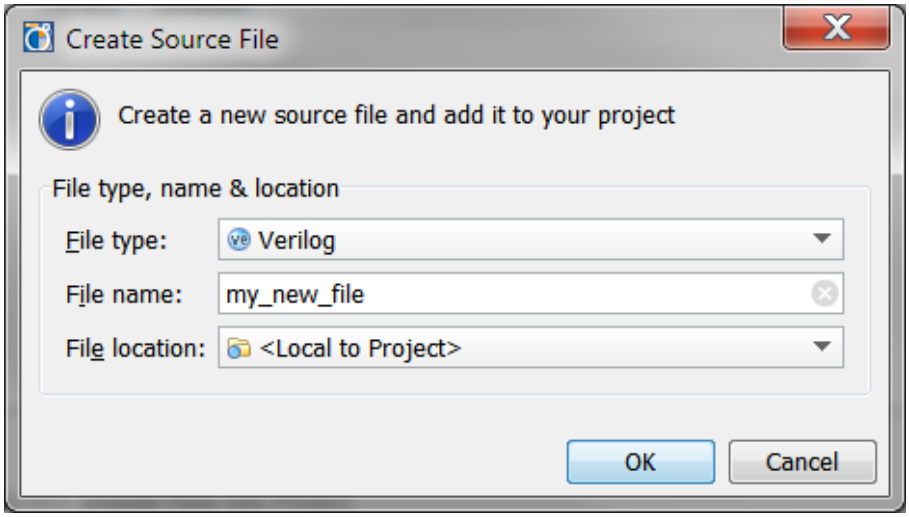

Figure 14: Create Source File Dialog Box

4. In the File name field, type **my_new_file**, and click **OK**.
5. In the **Add Sources** dialog box, click **Finish**.

   The Define Modules dialog appears. This can be used to define a module and its ports. Click the **Cancel** button. The new empty file is now listed in at the bottom of the Verilog folder list in the Sources view.

6. In the Sources view, double-click **my_new_file.v** to open it in the Text Editor (use the Search toolbar button to make finding this unreferenced source easier).
7. Click the Templates view tab next to the Sources view.
8. Expand the Verilog folder to examine the types of templates available and select one.

   The following figure shows the Verilog Templates folder.

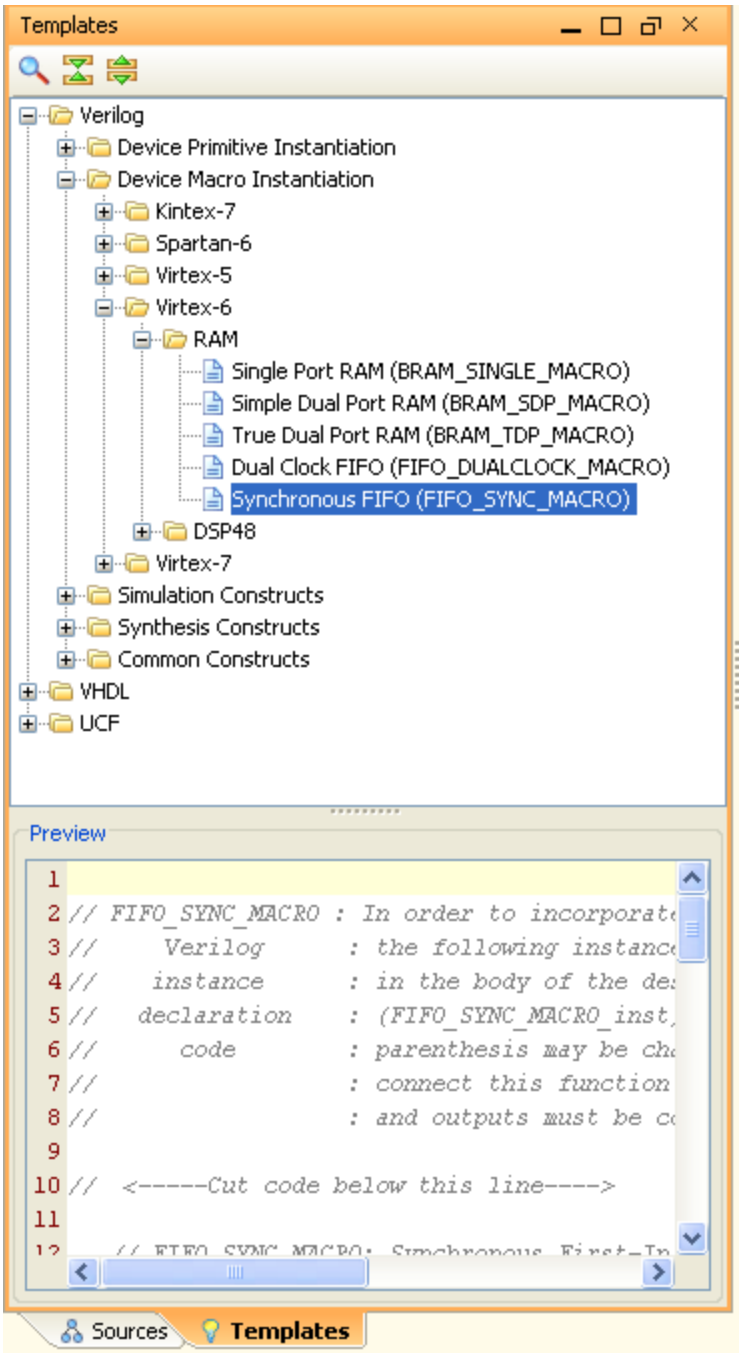

Figure 15: Examining the Templates in the Templates View

9. In the Text Editor, right-click and select **Insert Template**.

   The template text is now inserted in the new source file.

10. Click the **X** button in the my_new_file.v view tab.
11. In the **Save Text Editor Changes** dialog box, click **No**.
12. Select the Sources view tab.

Step 3: Running Behavioral Simulation

The Xilinx ISE Simulator (ISim) logic simulation environment is integrated with the PlanAhead tool. ISim can be used for behavioral or timing simulation. You can run behavioral logic simulation on the entire design, or an individual module.

Running Behavioral Simulation on the bft Module

1. In the Flow Navigator, select **Behavioral Simulation**.
2. Click the Simulation Top Module Name browser icon, and select **bft_tb**, and click **OK**.
3. Click **Launch**, and wait for ISim to open.

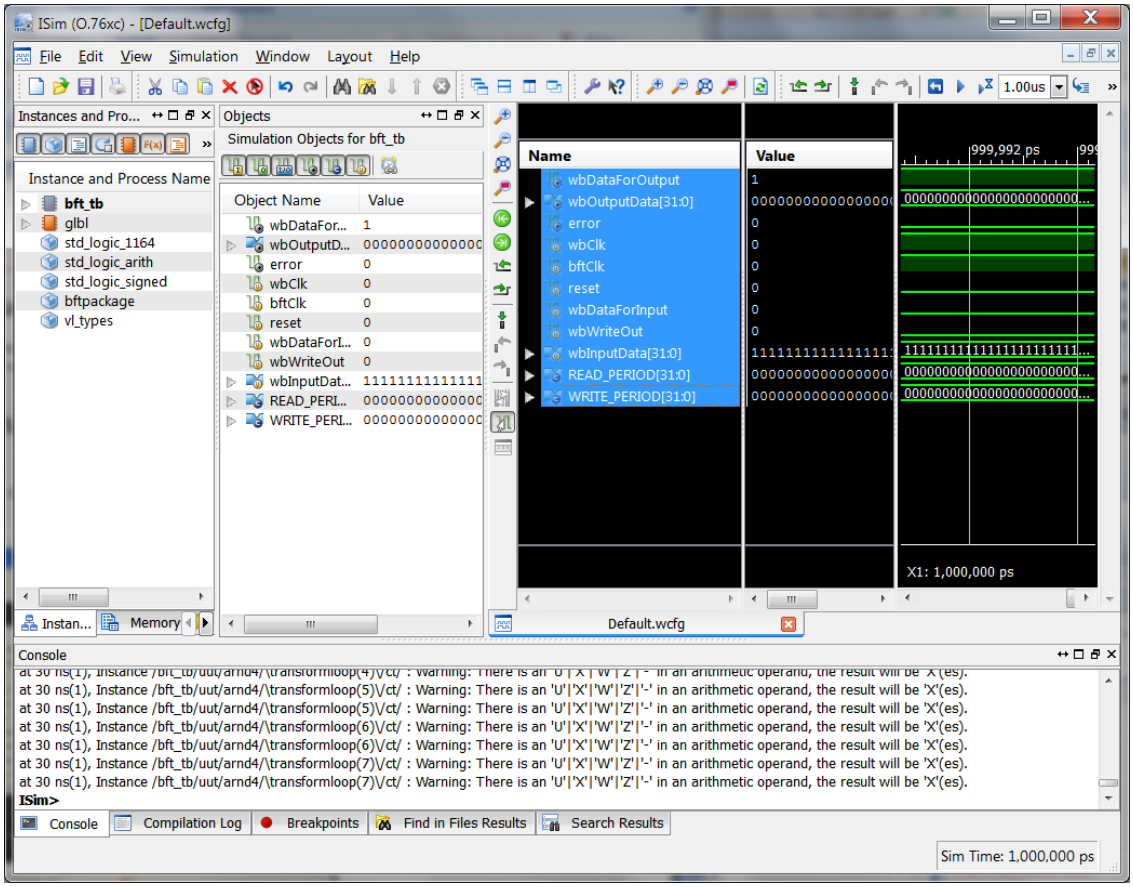

Figure 16: Launching ISim for Behavioral Simulation

4. Close the ISim window. Click **Yes** to confirm.

Setting Compilation Order and Disabling Unused Sources

The PlanAhead tool will automatically select a top module, order source files, and display source files based on compilation order. The top module can also be specified by the user. Files not needed in the design can be automatically or manually disabled.

1. In the Sources view, Hierarchy tab, expand **top** and select **mgtEngine**. Right-click, and select **Set as Top**.

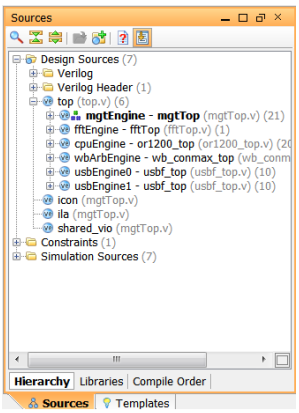

Figure 17: Specifying the Top Module in the Source Hierarchy View

2. Select the Compile Order tab in the Sources view and see that the required source files and compile order have been updated based on the new top module. To manually enable or disable a file, select the file, right-click, and select **Enable File** or **Disable File**.

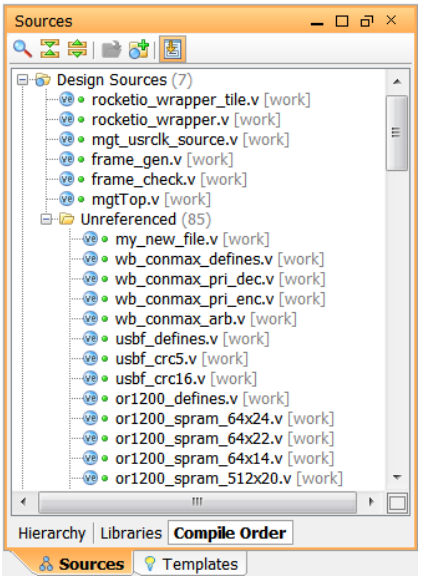

Figure 18: Viewing the Reordered Sources

3. Select the Hierarchy tab select **top**. Right-click, and select **Set as Top.**
4. The source file and compile order should be updated.

5. Right-click in the Sources view, select Hierarchy Update. See that three different options are available, ranging from fully automatic to completely manual file control.

6. Hit the **Esc** key to cancel the context menu.

Step 4: Elaborating and Analyzing the RTL Design

The PlanAhead tool provides RTL elaboration capabilities to compile RTL source files in the project. Displayed compilation errors and warnings are cross-selectable to the lines that are in error in the RTL code. Once elaborated, the RTL views enable cross-selection of logic objects. The RTL logic hierarchy is expanded and available for analysis. Opening the RTL Design from the Flow Navigator automatically elaborates the RTL design and displays the Design Analysis view layout.

- The RTL Netlist and Hierarchy views display the logic hierarchy of the design.
- The RTL Schematic enables interactive logic exploration.
- The Find command enables searching of RTL logic objects.
- The Instance Properties view displays information about the selected logic instantiation including resource estimation.
- The RTL DRCs highlight potential areas of the design to improve power or performance.

Elaborating and Opening the RTL Design

1. In the Flow Navigator, select **RTL Design**.
2. Click the Messages view tab to scroll through the Warnings and Info messages.

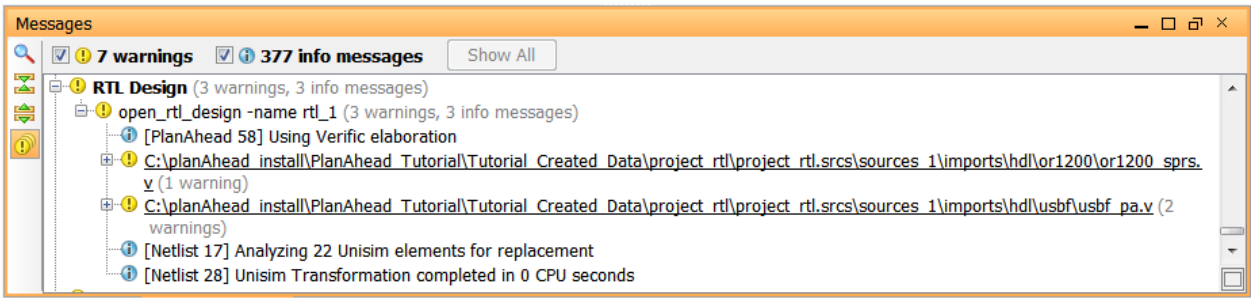

Figure 19: Viewing RTL Design Elaboration Messages

Reviewing RTL Design Messages

1. In the header of the Messages view, click to disable the Info Messages checkbox.
2. Review the Warning messages.

   There are no Errors in the design. If there were error messages, they would display in the Messages view.

3. Click to enable the Info Messages again, or click the **Show All** button, in the Messages view header.

Examining the RTL Logical Netlist and Hierarchy

1. In the RTL Netlist view, expand the usbEngine0 instance by clicking the plus sign (**+**).
2. Select the **usbEngine0/u0** instance.
3. Right-click and select the **Go to Definition** popup command.

   The RTL file `usbg_utmi_if.v` opens in the Text Editor. This is the RTL code that defines the UTMI Interface module. The file opens to the line containing the `usbg_utmi_if` module definition.

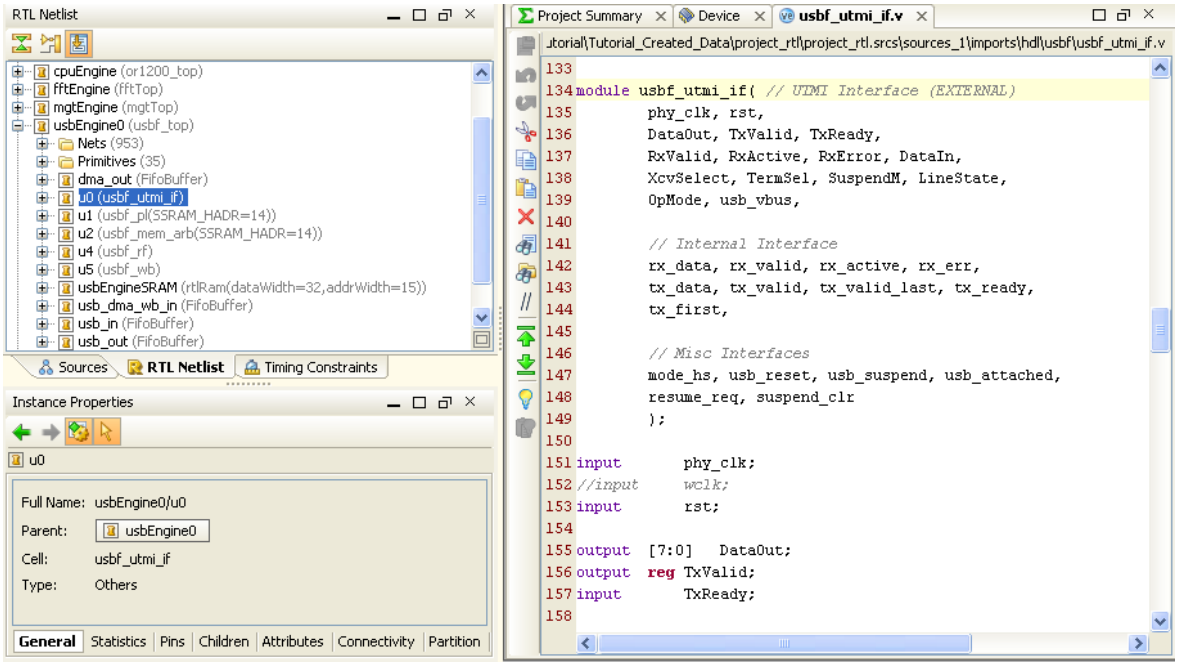

Figure 20: Viewing the Logical RTL Netlist

4. In the RTL Netlist view, right-click and select the **Go to Instantiation** popup command.

   The RTL file usbf_top.v opens in the Text Editor. This is the file in which the UTMI Interface module is instantiated into the design. The file opens to the line containing the usbg_utmi_if instance.
5. In the RTL Netlist view, right-click and select the **Show Hierarchy** popup command.

The RTL Hierarchy view opens with the selected module. The modules display with rectangles sized relative to the amount of logic contained in them, making it easy to locate large modules.

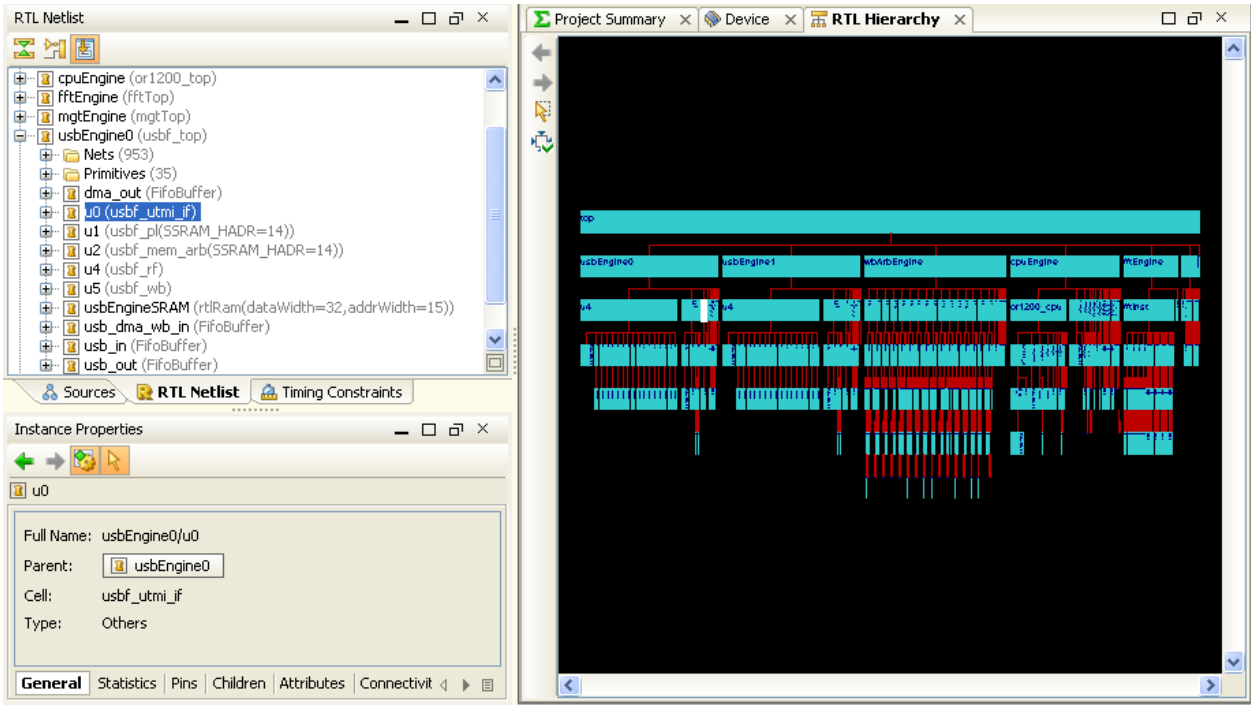

Figure 21: Displaying Modules in the RTL Hierarchy View

6. To close the RTL Hierarchy, click **X** on the view tab.
7. To close the Text Editor, click **X** on all open RTL files.

Examining the RTL Schematic

1. In the RTL Netlist view, expand and select the usbEngine0/u0/u0 instance (the level below the previous selection).

2. In the RTL Netlist view, click the **Schematic** button, or right-click and select the **Schematic** popup command.

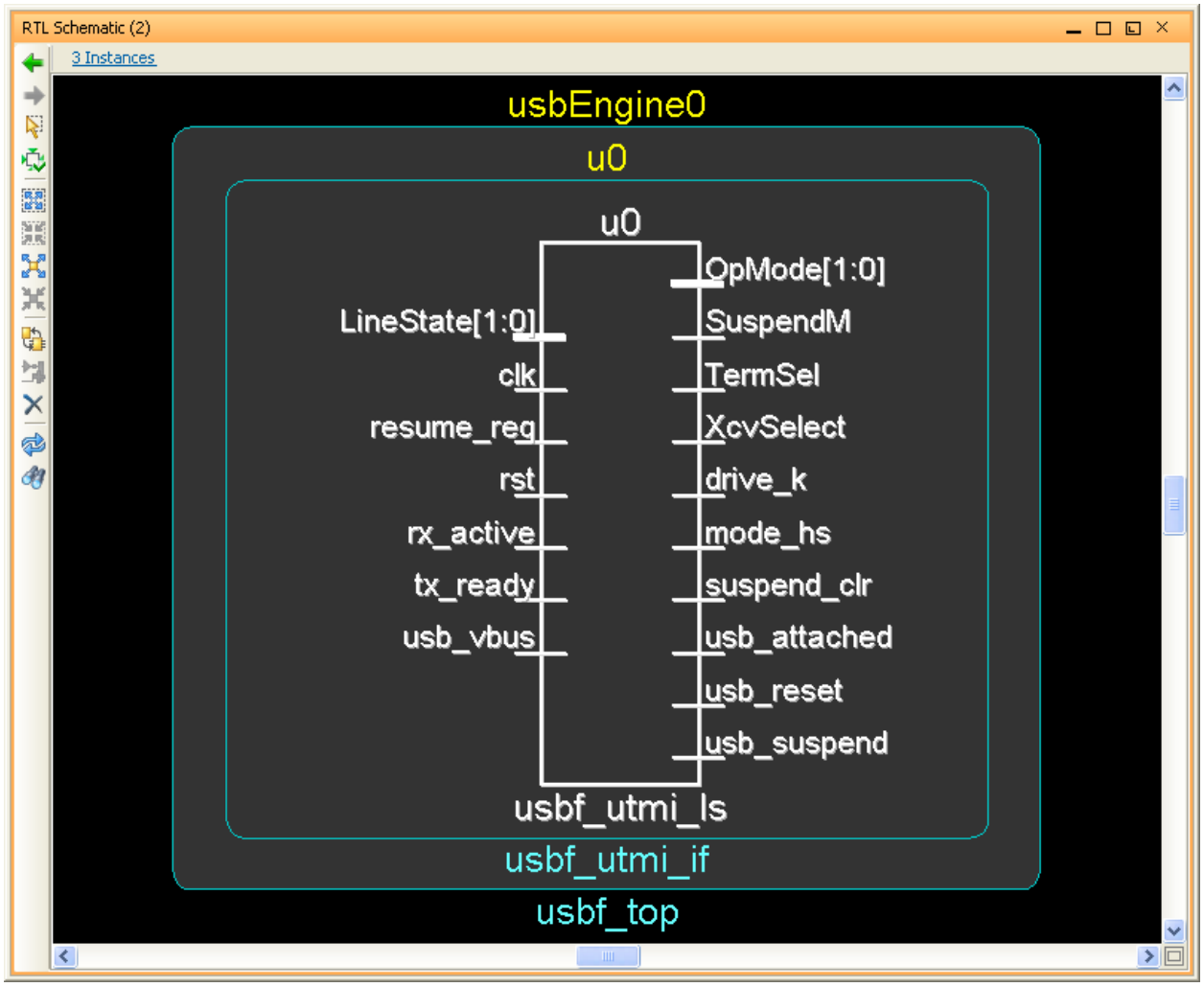

Figure 22: Viewing the RTL Schematic

3. Double-click the **LineState[1:0]** pin on the outside of the u0 module to expand the logic outward.

4. Zoom Fit the RTL Schematic view. The expanded logic is shown in the following figure.

Hint: Click and drag using the left mouse button in the RTL Schematic view from the lower right to the upper left to use the Zoom Fit command.

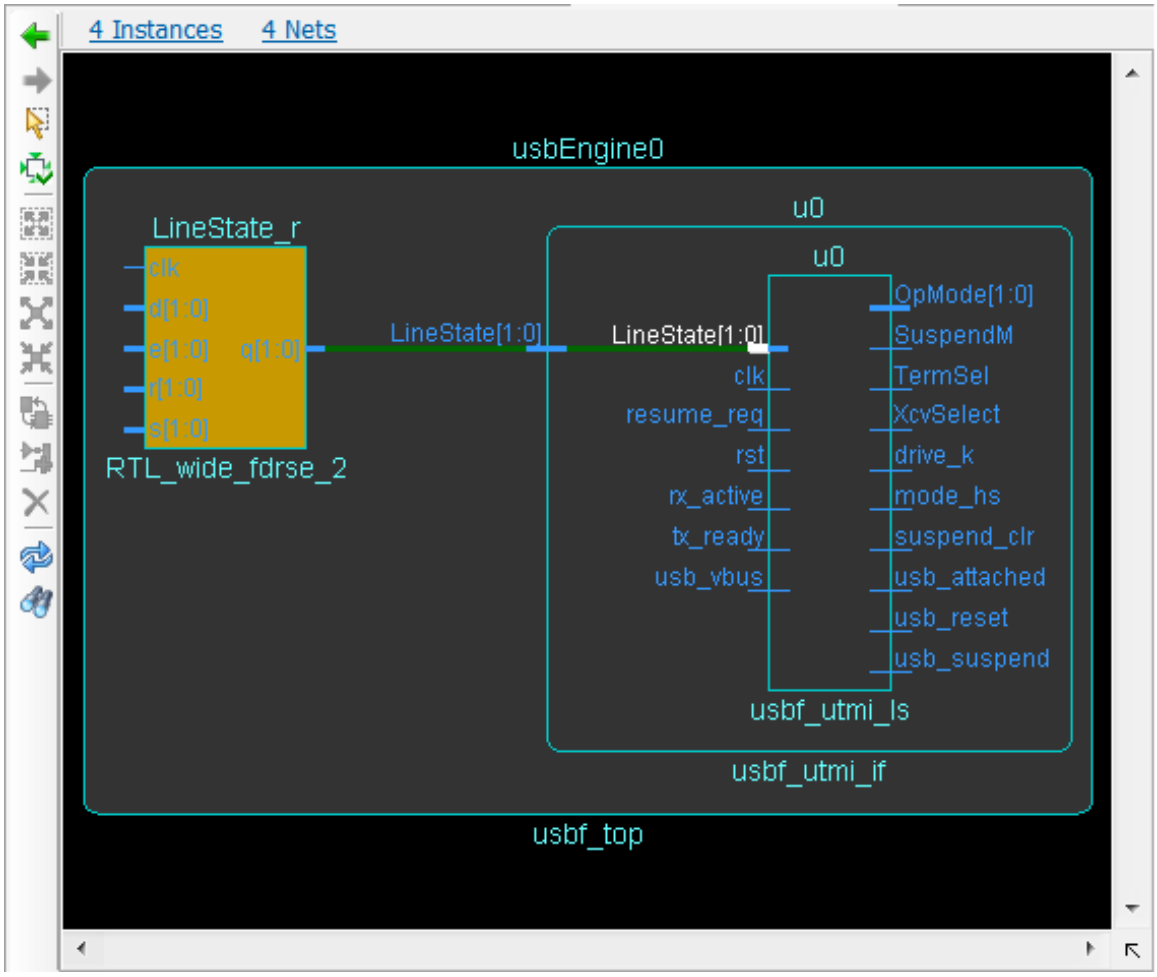

Figure 23: Expanding Logic in the RTL Schematic View

For additional schematic exploration capabilities, see the *Design Analysis and Floorplanning Tutorial (UG676)*.

5. On the left side of the RTL Schematic view, select the **RTL_wide_fdrse_2** instance.

6. In the RTL Schematic view, right-click and select the **Go to Instantiation** popup command to display the RTL file with the logic definition.

7. Close the Text Editor and the RTL Schematic.

8. In the RTL Netlist view, click the **Collapse All** button .

Using the Find Command to Locate RTL Block RAM Logic

1. Click the Find button in the main toolbar  , or select **Edit > Find** to open the **Find** dialog box.

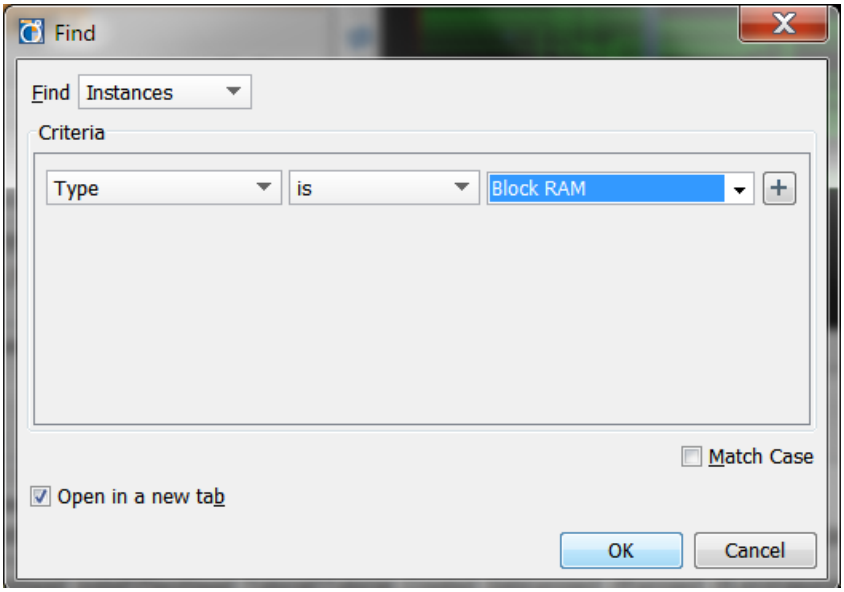

Figure 24: Searching for RTL Logic Using the Find Dialog Box

2. Examine the Find filter options.
3. Set the Criteria to **Type is Block RAM**, and click **OK**.

   The Find Results view opens.

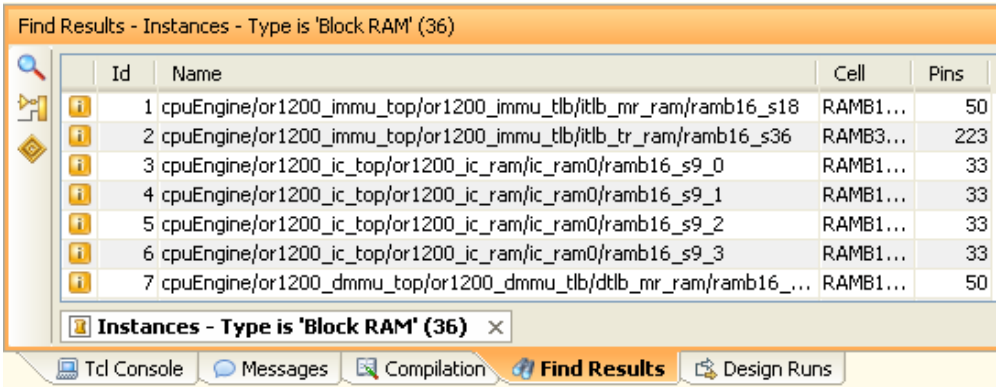

Figure 25: Find Results for RTL Block RAM Search

   The Find Results view displays the results of the search.

4. Select one of the Block RAMs in the list, right-click and select **Go to Instantiation**.

   The instance is selected in the RTL Netlist view and displayed in the Text Editor.

5. Close the Find Results view and the Text Editor.

Step 5: Estimating Resource Utilization

Examining the Resource Estimation Options

1. In the Flow Navigator, select the **Resource Estimation** command.

   The Resource Estimation view opens.

Figure 26: Viewing the RTL Resource Estimation

2. Expand the Block Memory Estimation tree to explore the hierarchical chart report.
3. To close the Resource Estimation view, click **X** on the Resource Estimation tab.

Examining Resource Estimates for RTL Instances

1. In the RTL Netlist view, select **top**. The RTL Macro Resources displays in the Netlist Properties view, as shown in the following figure.

   If the Netlist Properties view is not displayed, right-click, and select **Netlist Properties**.

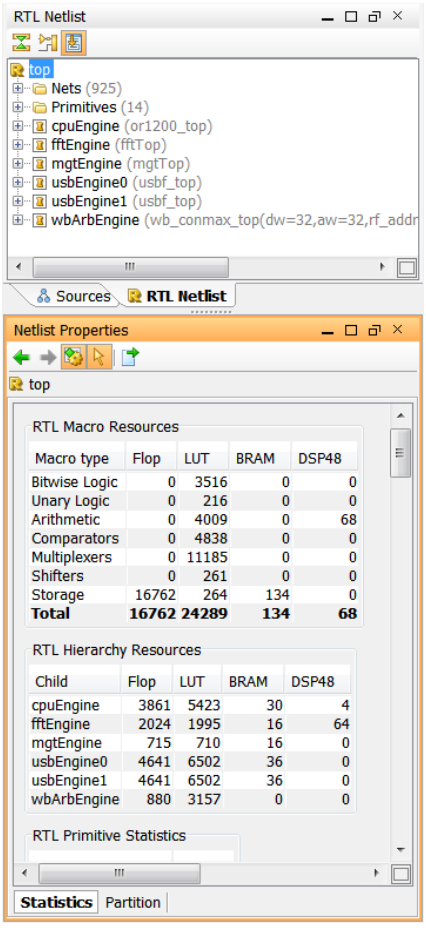

Figure 27: Viewing the RTL Resource Estimates

2. Scroll down the Netlist
3. Examine the properties, including:
   - RTL Macro Resources
   - RTL Hierarchy Resources
   - RTL Primitive Statistics
   - RTL Memory Resources
   - Net Boundary Statistics
   - Clock Report

In the RTL Netlist view, select other modules and examine the same estimates for the selected module. You might need to click the **Statistics** tab in the Instance Properties view.

Step 6: Running RTL Design Rule Checks

PlanAhead provides Design Rule Checks (DRC) that can be run on the RTL Design. These include LINT-style RTL checks for power or performance improvement suggestions. There are basic I/O bank and voltage rules for the RTL Design also. After the design is synthesized, a more comprehensive set of logic design, I/O, and clock DRCs is available for the Netlist Design.

Running DRCs

1. From the Flow Navigator or the **Tools** menu, select **Run DRC**.
2. In the **Run DRC** dialog box, expand and examine the RTL rules, and click **OK**.

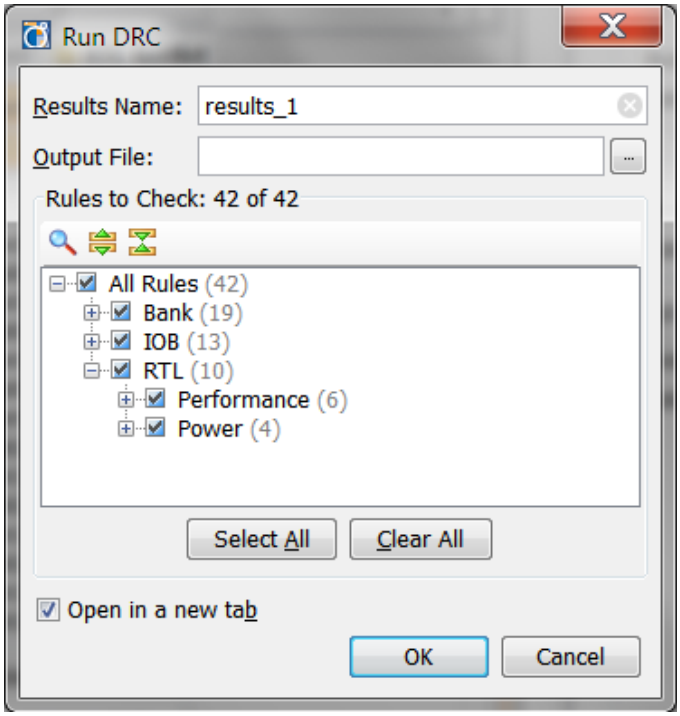

Figure 28: Running RTL DRCs

The DRC Results view opens.

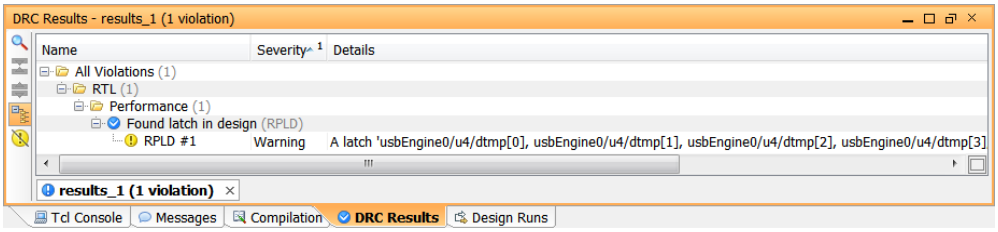

Figure 29: Viewing the RTL DRC Results

The RTL Results viewer color-codes messages as follows:

- Errors with a red icon
- Critical Warnings with an orange icon
- Warnings with a yellow icon
- Informational messages with a blue icon

4. Select the **RPLD #1** latch warning in the list.

   The Violation Properties view displays with information about the violation and links to select the offending logic objects.

5. In the Violation Properties view, click the **dtmp[0] link**, and see that the logic object is selected in the RTL Netlist view.
6. In the RTL Netlist view, select the **Go to Instantiation** popup menu command (or press **F7**) to open the Text Editor.
7. Close the DRC Results view and any open Text Editor views.
8. Close the RTL Design. Click **OK** in the confirmation dialog box if needed.

Step 7: Selecting IP from the Xilinx IP Catalog

The PlanAhead tool is integrated with the CORE Generator™ software to provide an IP Catalog with search and filtering capabilities. This allows you to easily find the desired IP. You can customize, instantiate and implement the core directly from the PlanAhead tool. You can access the IP Catalog from the Project Manager and RTL Design environments.

Opening the IP Catalog and Exploring the Search Options

1. Select **IP Catalog** from the Flow Navigator.
2. Expand some of the IP categories.
3. Select an IP and explore the available toolbar buttons and popup menu commands.

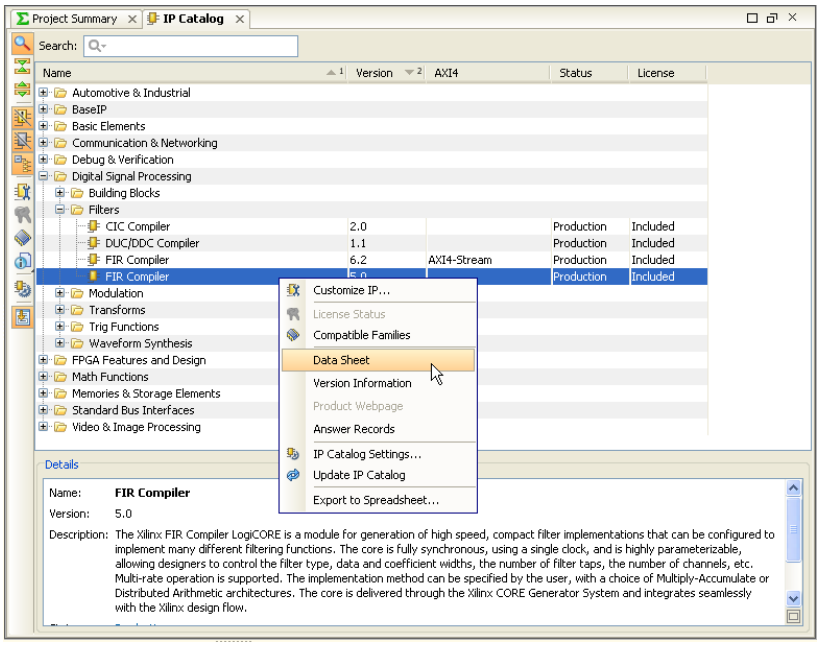

Figure 30: Browsing the IP Catalog

The Details for the selected IP display at the bottom of the view. By default, only the IP that is current and available for the selected device family is displayed.

4. To view all IP, toggle the Hide Superseded and Discontinued IPs button and the Hide incompatible IPs button .
5. To view a flattened list of IP, toggle the **Group by Category** toolbar button .
6. Type **fir** in the Search field at the top of the view.
7. Select a FIR Compiler IP, click the **Data Sheet** button , and select Data Sheet.
8. Examine the Data Sheet, then close the PDF viewer.
9. Clear the Search field to expand the Catalog list.

Step 8: Customizing and Instantiating IP

Customizing a Simple Adder IP

1. Click the **Group by Category** button .
2. Click the **Collapse All** button .
3. Expand the Math Functions > Adders & Subtracters folder.
4. Double-click Adder Subtracter to run the Customize IP command.

   This opens the CORE Generator™ tool and displays the customized interface for the selected IP. Different IP have different types of interfaces.

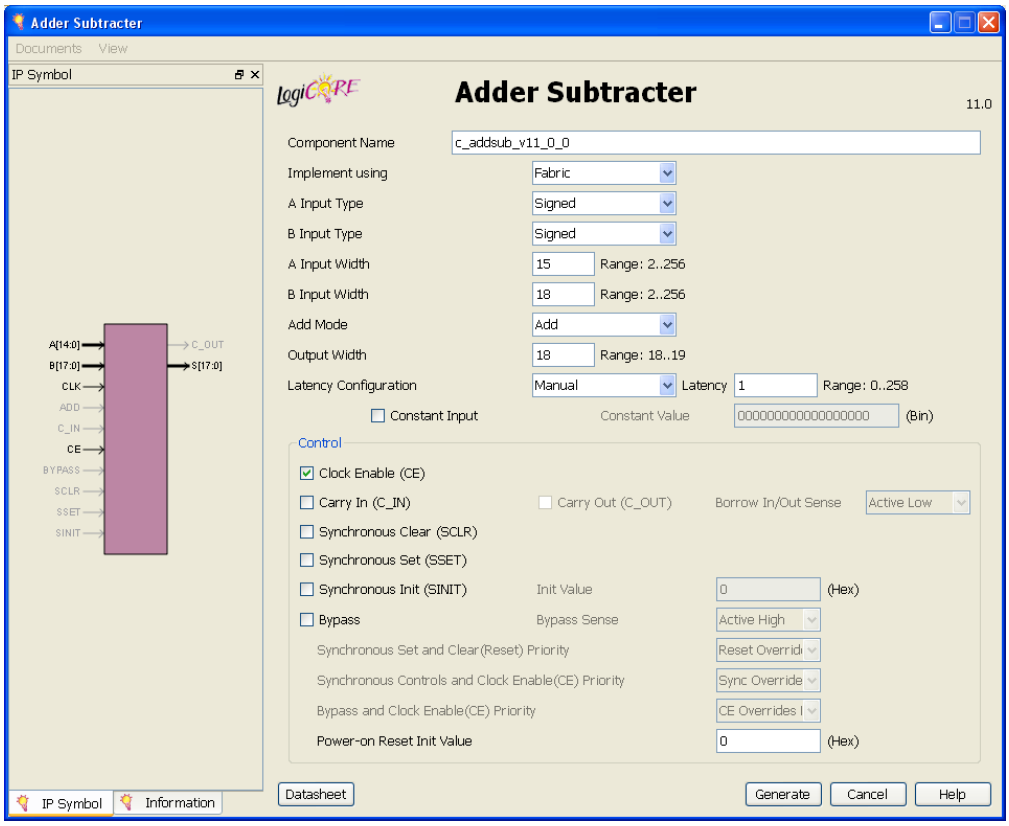

Figure 31: Customizing IP With the CORE Generator Software

5. In the B Input Width field, type **18**.
6. Click Generate.

   Clicking Generate has a different effect when launched from PlanAhead than when run from CORE Generator standalone.

   - In standalone mode, the CORE Generator™ software automatically launches XST to synthesize the IP core.
   - When launched from the PlanAhead tool, the synthesis step is not run automatically, which lets you instantiate and configure the core in your RTL before launching synthesis. You can

synthesize the IP at any time or launch synthesis on the entire design for which the IP is synthesized first.

Instantiating the Adder IP

1. In the Sources view, Libraries tab, click the **Collapse All** button .
2. Expand the IP folder and then expand the **c_addsub_v11_0_0** IP.
3. Double-click the **c_addsub_v11_0_0.veo** file to view the instantiation template in the Text Editor.

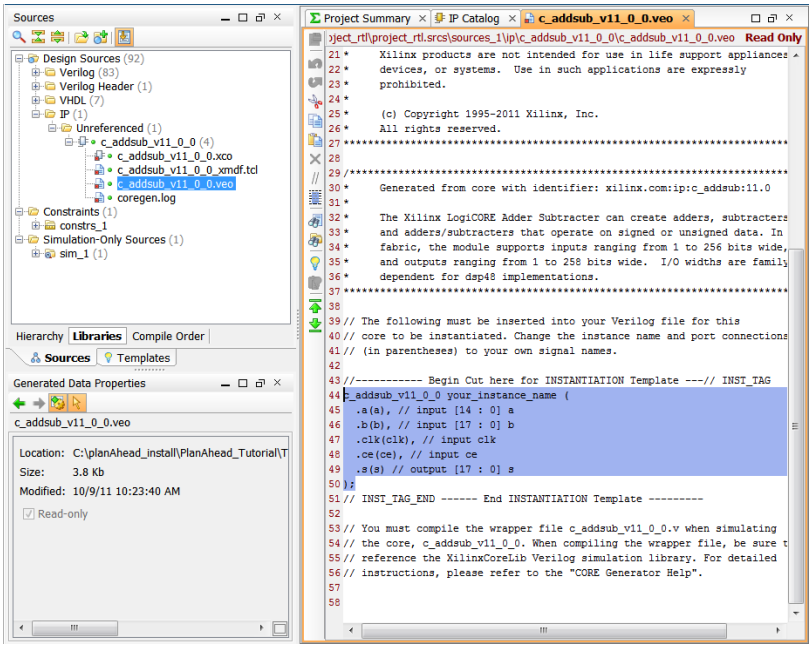

Figure 32: Viewing the Instantiated Template

4. Select the text in the Text Editor, as shown above, and click the **Copy** button .
5. In the Sources view, expand the Verilog and work folders.
6. Double-click the `top.v` file to open it in the Text Editor.
7. Scroll to the bottom of the file just before the endmodule text.
8. Select the line just above the endmodule statement and select the **Paste** button .
9. Change the **your_instance_name** text in the template to **my_addr** as shown in the following figure.

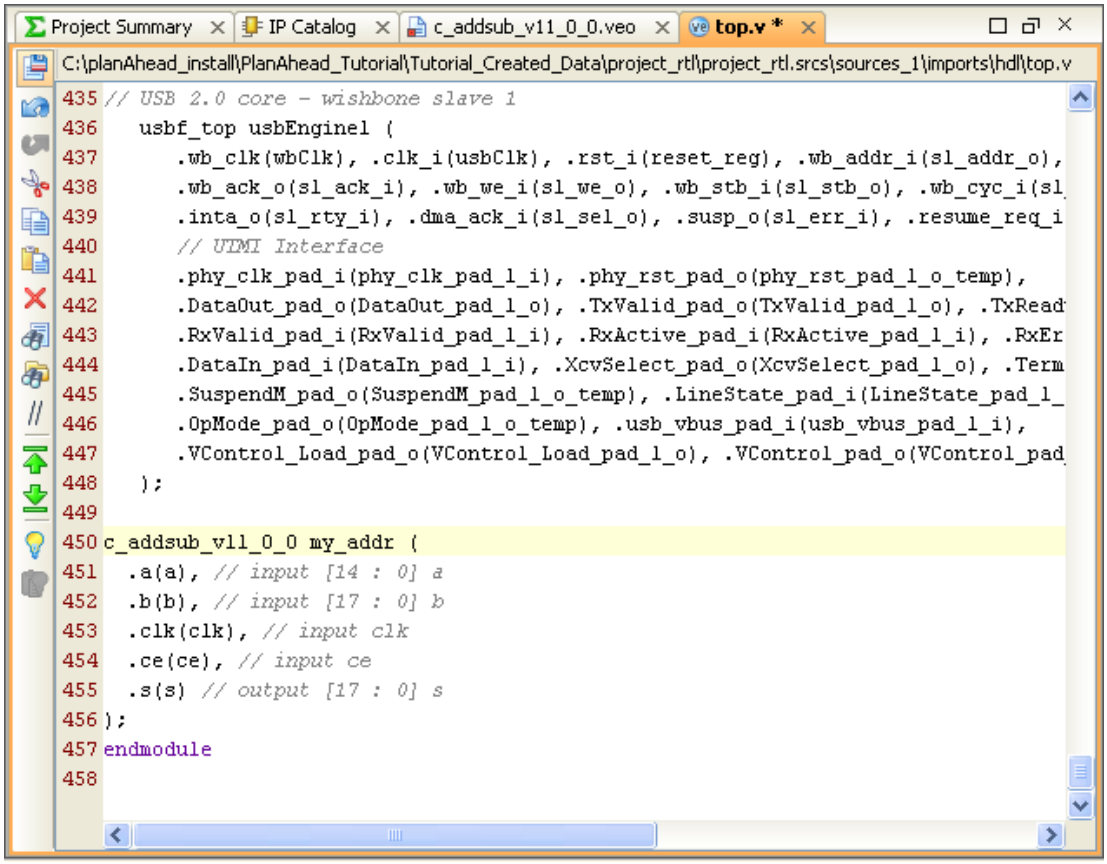

Figure 33:Instantiating IP in Your Design

10. Change the `.clk` port definition to use the existing **cpuClk** clock signal.

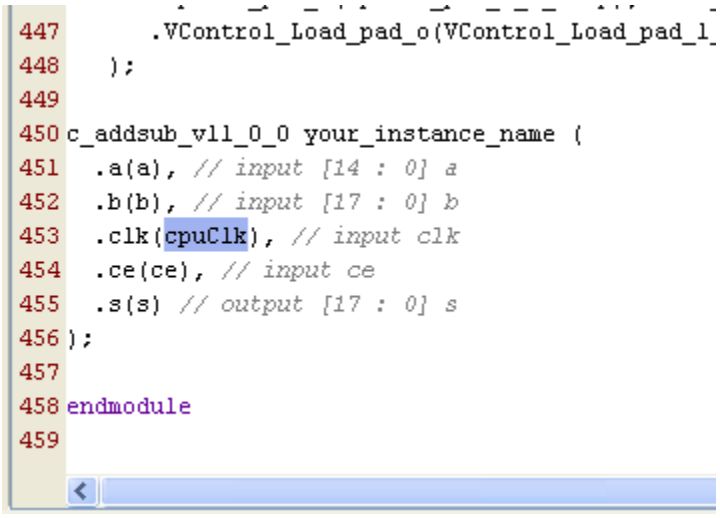

Figure 34: Modifying the clk Signal to Use the cpuClk Clock Signal

11. Scroll to the top of the `top.v` file and add the IP ports (a, b, ce, s) to the module port definition as shown in the following figure.

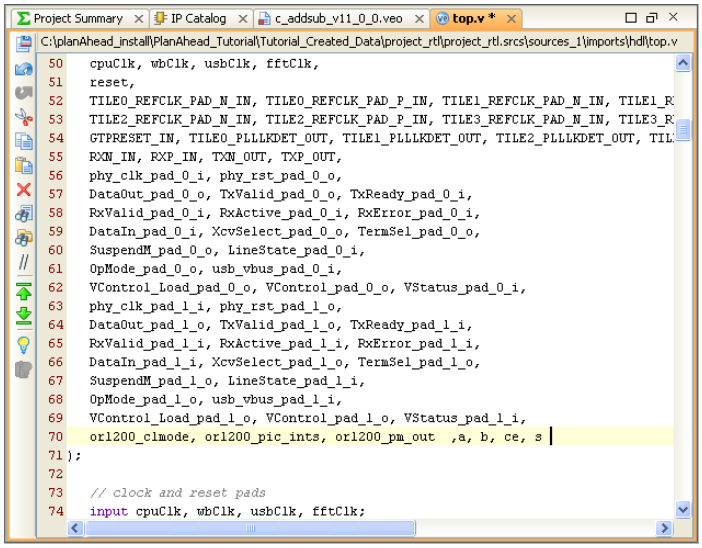

Figure 35: Adding IP Ports to the Top-Level Module Port List

12. Define the ports for the IP in the design by adding the following text to the top.v file.

```
//addr pads
input [14:0] a;
input [17:0] b;
input ce;
output [17:0] s;
```

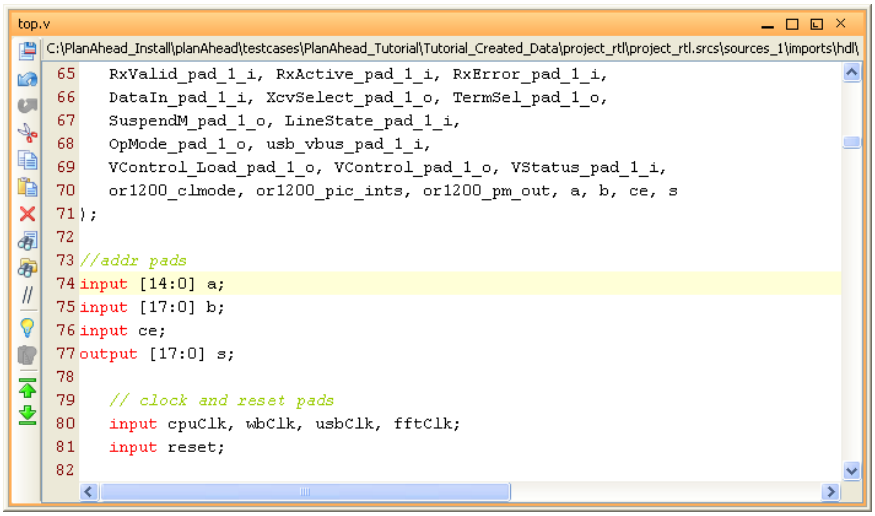

Figure 36: Defining IP Ports in top.v

13. To close the `top.v` file, click **X** on the tab, and select Yes to save changes.
14. To close the `.veo` template file, click **X** on the tab.
15. To close the IP Catalog, click **X** on the tab.

Step 9: Generating IP

Generating the IP and Exploring the Logic in the Schematic

1. In the Sources view, select the `c_addsub_Vxx_x` top-level file, right-click and select **Generate IP**. Wait for the IP to synthesize.

   After the IP generates, the Messages view displays information about the Generated IP. Scroll to explore the messages.

2. To open the RTL Design and view the logic, in the Flow Navigator, click **RTL Design**.

   In the RTL Netlist view, expand and select the **my_addr** module.

   Note: If a black box icon appears in the RTL Netlist, review the RTL Design and Generated IP messages and go back and check the top.v file for errors. Rerun the RTL Design command until the IP appears in the RTL Netlist.

3. From the toolbar, click the **Schematic** button .

4. In the Schematic view, double-click the instance to expand the inside logic.

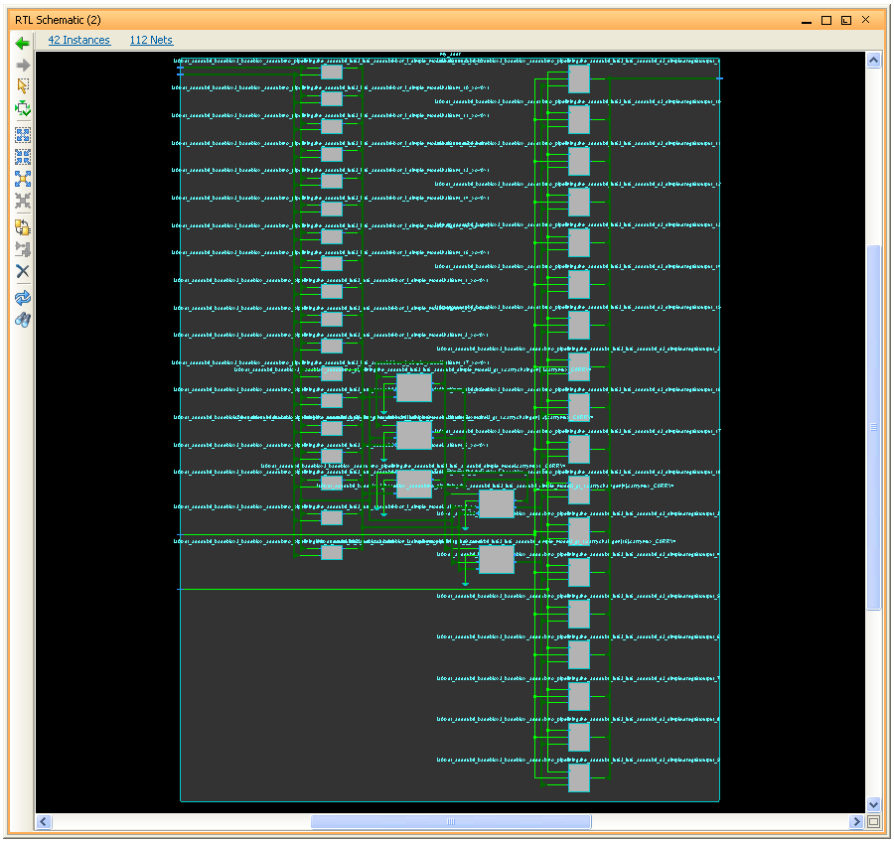

Figure 37: Analyzing the IP Logic in the Schematic

5. Close the Schematic view.

6. Select **File > Exit**. If prompted, click **No** to save and **OK** to close PlanAhead.

Conclusion

In this tutorial, you:

- Used a small RTL project to examine the PlanAhead RTL development and analysis environment.
- Started by creating an RTL project, explored RTL sources and the RTL editor.
- Ran behavioral simulation, elaborated the RTL design, and explored the analysis capabilities, which included examining the RTL logic hierarchy, RTL schematic exploration, searching for logic types, reviewing RTL resource and power estimates and running RTL DRCs.
- Examined the Xilinx IP Catalog, and customized, instantiated, and implemented a small adder IP core.