ChipScope Pro Tutorial

Using an IBERT Core with ChipScope Pro Analyzer

UG811 (v 14.3) October 16, 2012

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Revision
04/24/2012	Revalidated for the 14.1 release. Editorial updates only; no technical content updates.
07/25/2012	Revalidated for the 14.2 release. Editorial updates only; no technical content updates.
10/16/2012	Revalidated for the 14.3 release. Editorial updates only; no technical content updates.

Tutorial: Using an IBERT Core with ChipScope Pro Analyzer

Introduction

In the course of this tutorial you will:

- Create, customize, and generate an Integrated Bit Error Ratio Tester (IBERT) core design using the standalone CORE Generator™ tool.
- Interact with the design using ChipScope™ Pro Analyzer. This includes importing the bitstream file into ChipScope Pro Analyzer, configuring the device, and interacting with the IBERT/Transceiver IP cores.
- Perform a sweep test to optimize your transceiver channel and to plot data using the IBERT sweep plot GUI feature that was introduced in software version 13.1.

Prerequisites

A basic knowledge of Xilinx® ISE® tool flows.

Setting Up

Parts Required

Ensure that you have the following software and hardware:

- Xilinx ISE Design Suite 13.3 (Logic, DSP, Embedded, or System Edition)
- ML605 board
- JTAG USB cable delivered with the ML605 board
- Two SMA (SubMiniature version A) cables

Connecting the Board and Cables

1. Connect the USB cable from the USB JTAG connector on the board to your computer system.
2. Connect the two SMA cables:
   a. Connect one SMA cable from J28 to J26.
   b. Connect the other SMA cable from J29 to J27.

   The relative locations of connectors on the board are shown in Figure 1.

Figure 1: **SMA Cable Connections**

3. Turn the ML605 power switch on.

Design Description

You can customize the ChipScope Pro Analyzer IBERT core and use it to evaluate and monitor the functionality of transceivers for a variety of Xilinx devices. The focus for this tutorial is on Virtex®-6 GTX transceivers. The design includes pattern generators and checkers implemented in FPGA logic, as well as access to the ports and dynamic reconfiguration port (DRP) attributes of the GTX transceivers. Communication logic is included to allow the design to be runtime-accessible through JTAG. The IBERT core is a self-contained design. When generated, it runs through the entire implementation flow, including bitstream generation.

The IBERT design is auto-generated according to your specific customization in the Xilinx CORE Generator tool, so no additional example design is required for this tutorial.

Figure 2 shows a block diagram of the interface between the IBERT Virtex-6 GTX core interfaces with Virtex-6 transceivers.

- **DRP Interface and GTX Port Registers:** IBERT provides you with the flexibility to change GTX transceiver ports and attributes. Dynamic reconfiguration port (DRP) logic is included, which allows the runtime software to monitor and change any attribute in any of the GTX transceivers included in the IBERT core. When applicable, readable and writable registers are also included. These are connected to the ports of the GTX transceiver. All are accessible at runtime using the ChipScope Pro Analyzer tool.
- **Pattern Generator:** Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter.
- **Error Detector:** Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern.

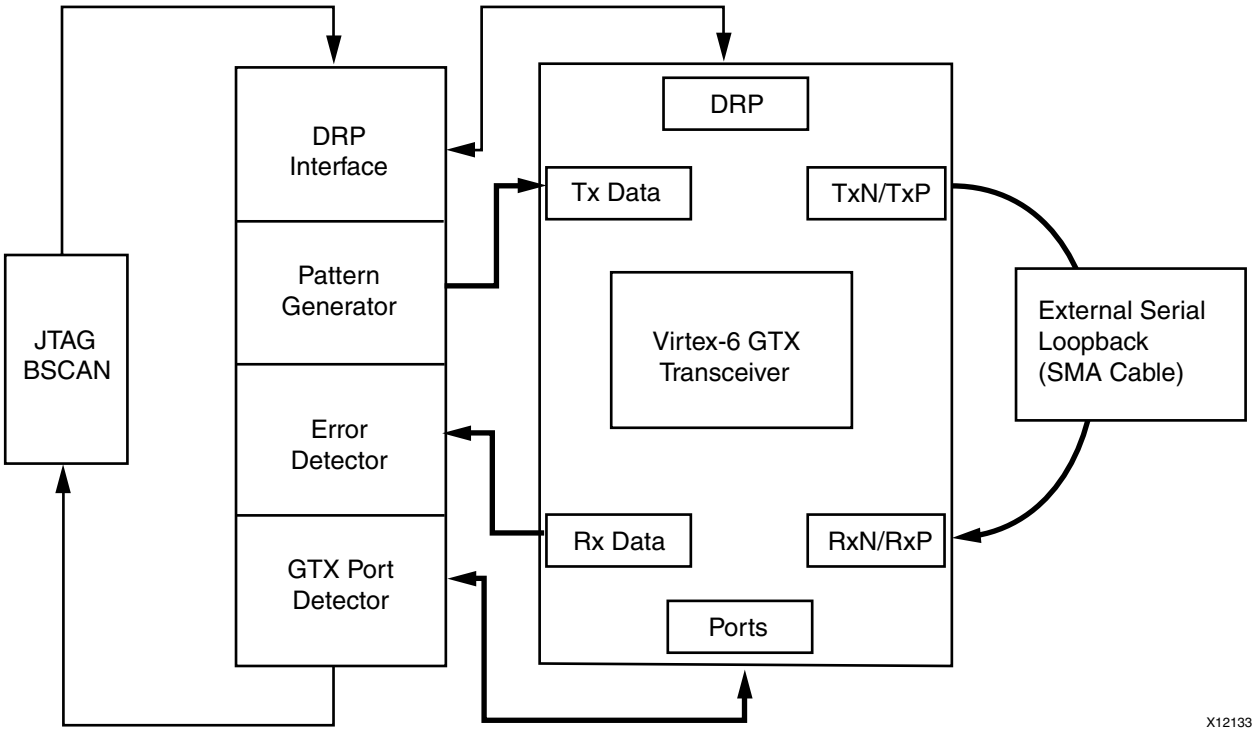

Figure 2: **IBERT Design Flow**

Step 1: Creating, Customizing, and Generating an IBERT Design

1. Open the Xilinx CORE Generator tool.
2. **Click File > New Project** and save the project as `IBERT_GTX_coregen`, as shown in Figure 3.

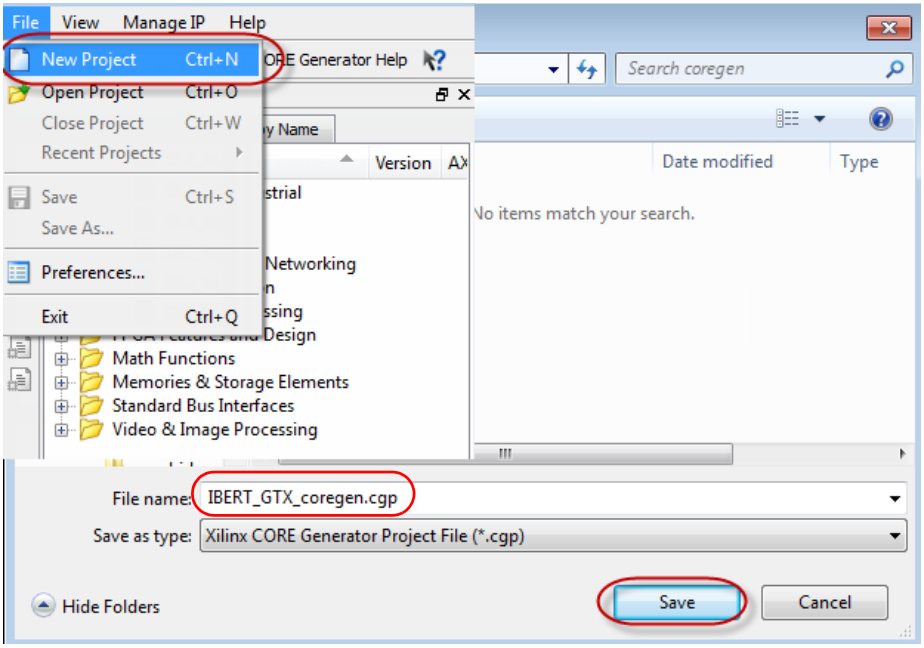

Figure 3: **Creating and Saving a Project in the CORE Generator Tool**

3. When you save the project, the **Project Options** dialog box appears.
   a. With the **Part** option selected:
      - Set **Family** to **Virtex 6**.
      - Set **Device** to **–xc6vlx240t** (the device on the ML605 board).
      - Set **Package** to **ff1156.**
      - Set **Speed Grade** to **-1**.
   b. Use the default settings for all other project options (Generation and Advanced).
   c. Click **Apply**, then **OK**.
4. Select the IBERT IP core to generate.

   In the **IP Catalog** pane, double click **Debug & Verification > ChipScope Pro > IBERT Virtex6 GTX (ChipScope Pro-IBERT)**.
5. In the board configuration settings dialog box for the core, shown in Figure 4, locate the **Board Configuration Settings** drop-down menu and select **ml605 bank116fmclpcsfpsmasgmii**.

   Note: If you don't see the drop-down items shown in Figure 4, you might have selected the wrong device in numbered step 2, above.

   Note: The **Board Configuration Settings** drop-down menu includes **User Defined**, along with four other pre-configured board settings that target an ML605 board, including the one you selected, above. Each of the pre-configured board selections provides all the pre-settings you need. This is useful when you want to evaluate your design environment quickly, or when you want to explore certain pre-configured board functions. In addition, you can use the pre-settings

as a template for your own **User Defined** settings. The **User Defined** option requires that you familiarize yourself with parameters such as clock, pin location, and protocol type. When you choose a pre-configured board selection, this is not necessary.

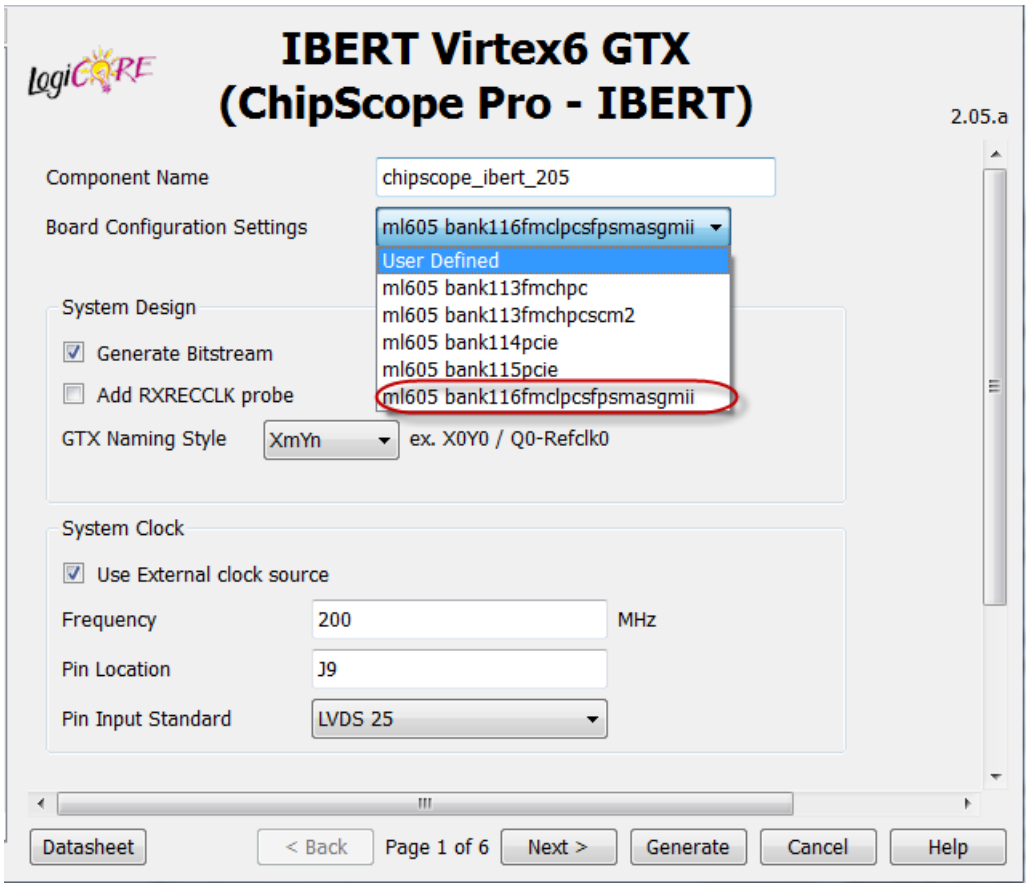

Figure 4: **Board Configuration Settings Dialog Box**

6. Click **Next** and review the pre-configured parameters.
7. When finished, click **Generate** to start generating the IBERT design. It might take a minute or so to generate the core.

You just finished creating a project file in the CORE Generator tool, and you customized and generated the IBERT design. Next, you will learn how to interact with this design using ChipScope Pro Analyzer.

Step 2: Interacting with the Design Using ChipScope Pro Analyzer

In this section of the tutorial, you will use ChipScope Pro Analyzer to interact with the IBERT design that you created in Step 1. You will perform some analysis using various input patterns and loopback modes, while observing the bit error count.

1. Start ChipScope Pro Analyzer.
2. In the menu bar, click **JTAG Chain > Xilinx Platform USB Cable.**
3. The **ChipScope Pro Analyzer [new project]** dialog box appears. Accept the default settings.
4. The **ChipScope Pro Analyzer** dialog box appears. Accept the default settings.

Configuring the Device

1. In the ChipScope Pro Analyzer main window, in the **New Project** pane, right click **DEV: 1 MyDevice1 (XC6VLX240T)** and select **Configure** from the resulting menu.
2. In the pop-up dialog box, click **Select New File**, browse to the `..\coregen\*.bit` file, and click **OK** to start downloading the bit file onto the ML605 board.
3. In the ChipScope Pro Analyzer main window, in the **New Project** pane, expand **DEV: 1 MyDevice1 (XC6VLX240T)** and double-click **IBERT Console**.

Note: The **ChipScope Pro Analyzer - IBERT V6TX Project Settings** prompt might appear at this point, asking if you want to set up the core with settings from the current project. If you see this prompt, click **Yes**.

4. With initial settings on the loopback modes, the interactive **IBERT Console** window appears, as shown in Figure 5.

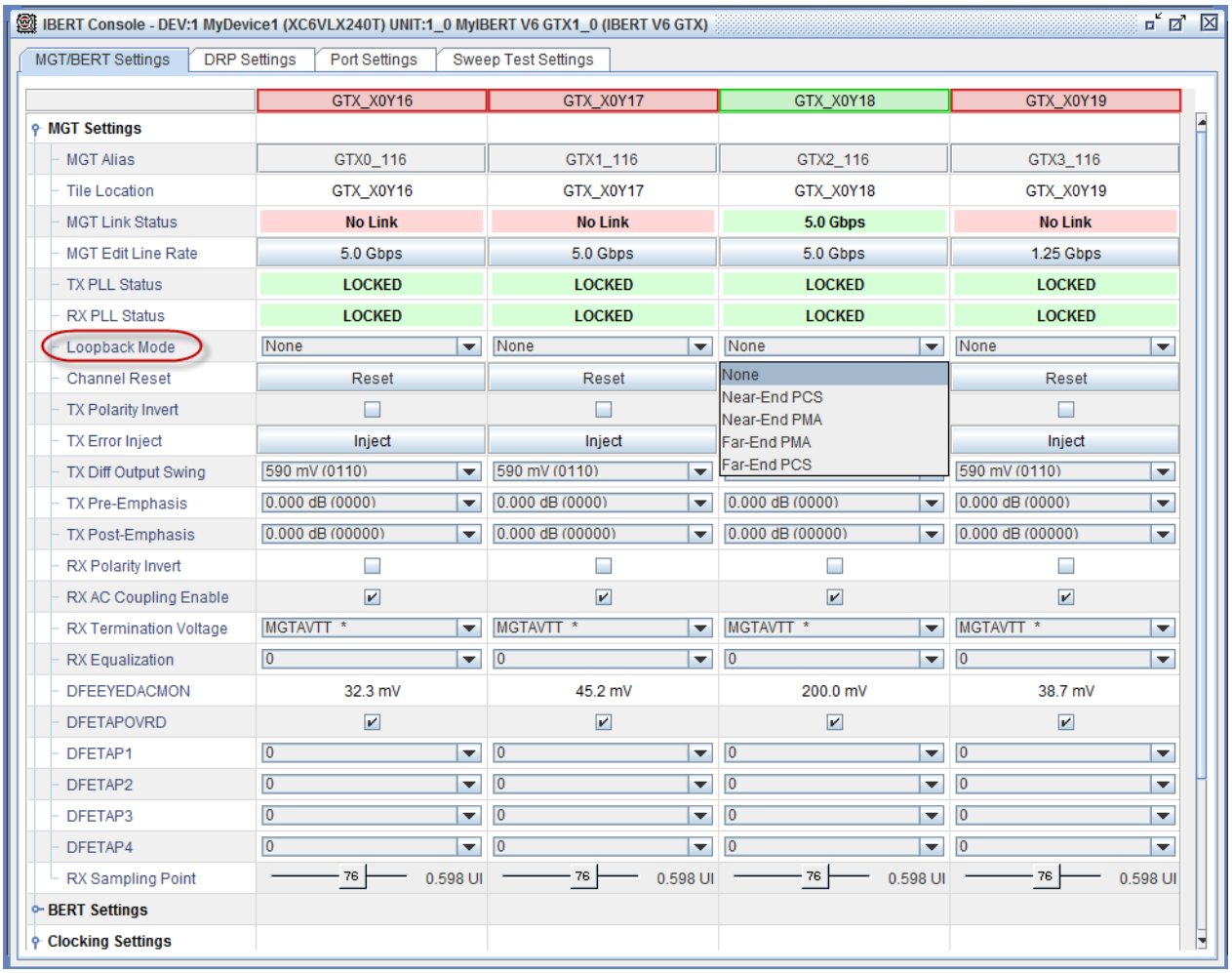

Figure 5: **IBERT Console Window for Virtex-6 FPGA GTX Transceivers**

IBERT Console Window Key Features

Note the four settings tabs at the top of the console window. Associated with each is a table in which the rows typically describe a function that can be dynamically controlled or that can serve as a status monitor.

For example, you can configure the Loopback Mode function by selecting one of the available settings from the pull-down menu.

Look at the Loopback Mode setting, which controls the loopback mode of a particular GTX transceiver channel. The following loopback modes are used in this tutorial.

- **None.** No internal loopback is used.
- **Near-End PCS.** The circuit is entirely contained within the near-end GTX transceiver. The loopback path starts from the TX fabric interface, passes through the PCS, and returns immediately to the RX fabric interface without passing through the PMA side of the GTX channel as shown Figure 6.

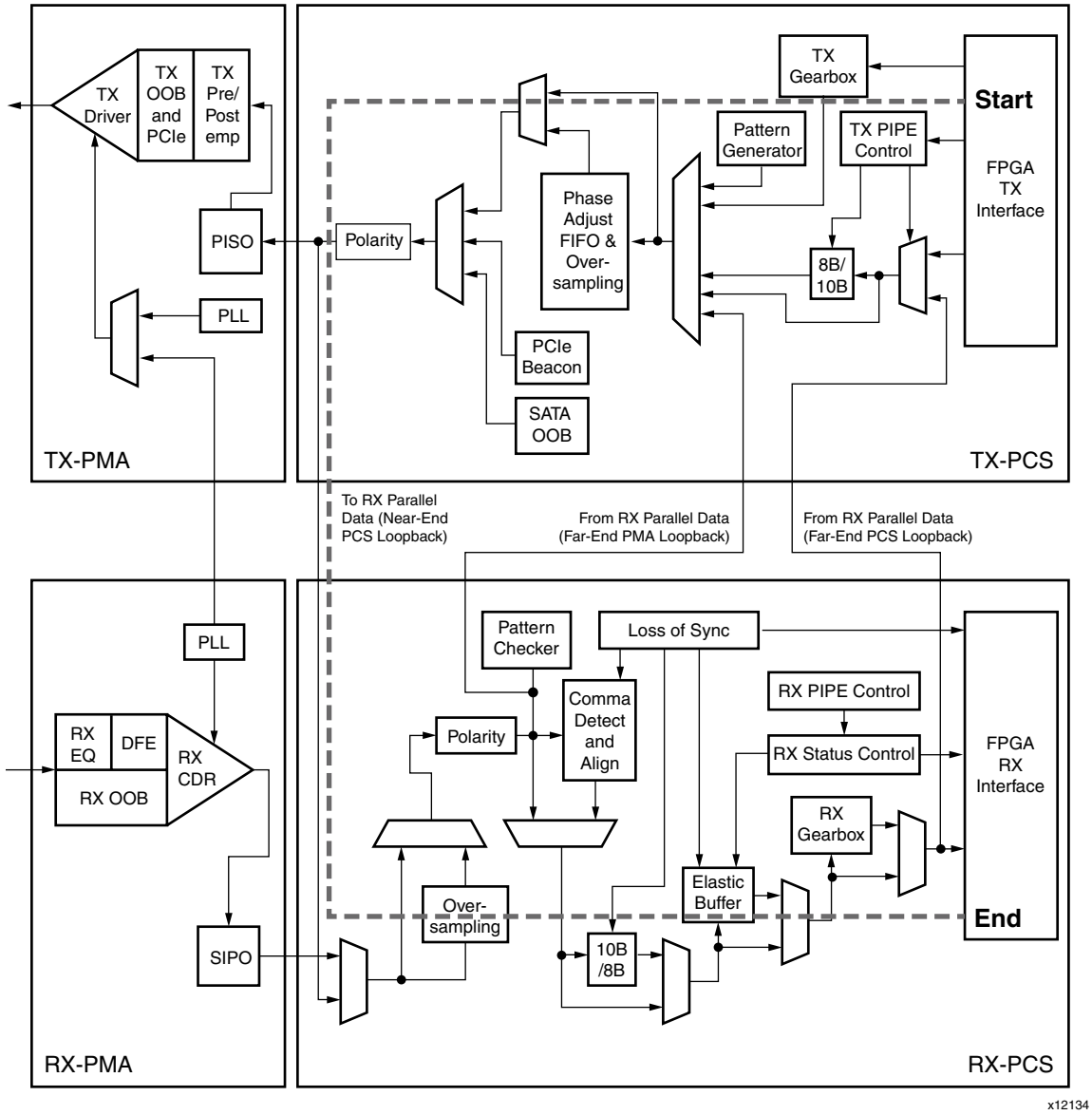

Figure 6: **GTX Loopback Path**

In the IBERT console, you can see that only the GTX_X0Y18 transceiver channel has established a 5 Gbps line rate link between the TX and RX channels. This is because it is the only channel being looped back between TX and RX. The other three channels display as **No Link**. The GTX_X0Y18 transceiver is the only channel in ML605 BANK 116 that can be looped back via SMA cables, as shown in the ML605 schematics below (Figure 7).

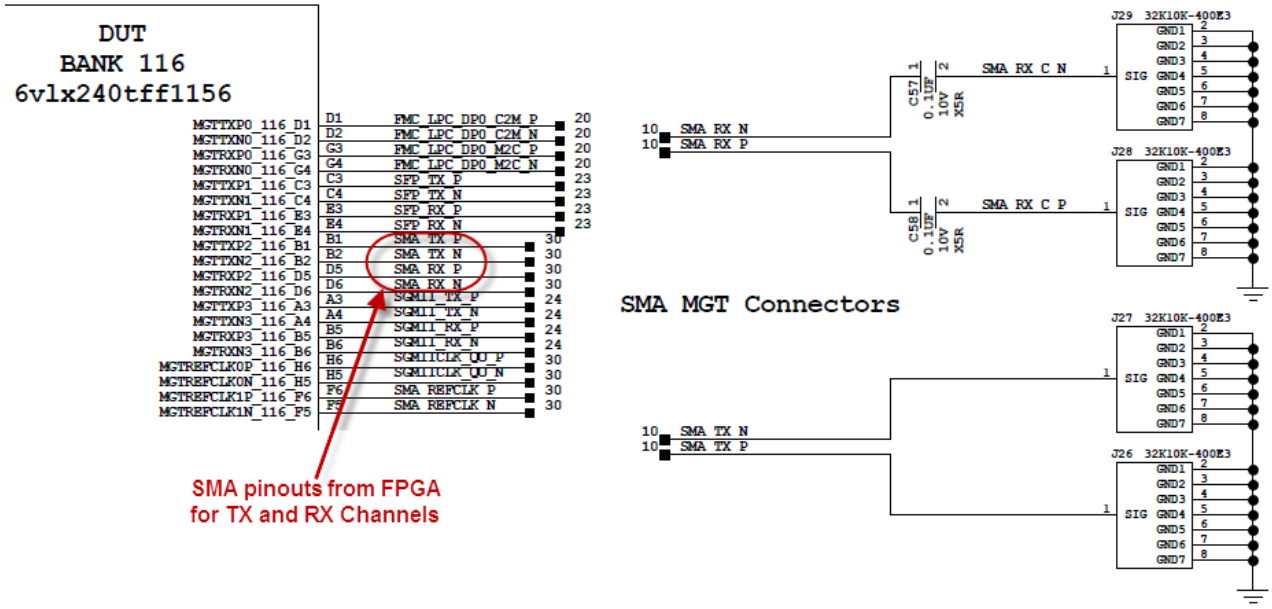

Figure 7: **ML605 Schematics for Loopback via SMA Cables**

For more details about the IBERT Console Window for Virtex-6 GTX Transceivers, refer to the *ChipScope Pro Software and Cores User Guide* at http://www.xilinx.com/tools/cspro.htm.

Step 3: Performing a Sweep Test

Overview

In this final step, you will perform a sweep test on a channel using various transceiver settings. You will:

- Open the Sweep Test Settings panel and review sweep test parameters.
- Set up to run the sweep test.
- Run the sweep test.
- Plot the data using the IBERT Sweep Plot GUI.

Opening the Sweep Test Panel and Reviewing Sweep Parameters

From the **IBERT Console**, click the **Sweep Test Settings** tab to open the panel in which you can set parameters for the sweep test.

Sweep Test Panel Parameters and Options

The **Sweep Test Settings** panel is shown in Figure 8. Some key options are circled in red.

In the **Sweep Test Settings** panel you can set up a channel test that sweeps through a variety of transceiver settings.

The TX and RX settings are for the same GTX transceiver. Sweeping through both TX and RX settings works only if the transceiver is set to one of the near-end or external loopback

modes. Sweeping through RX parameters can be accomplished only when the corresponding TX endpoint for the link resides in a different device or a different transceiver in the same device.

Note that the **Sweep Test Settings** panel is divided into four areas:

- Parameter Settings
- Sampling Point Region
- Test Controls
- Test Results

In this section of the tutorial, you will perform a sweep test of the GTX_X0Y18 transceiver channel.

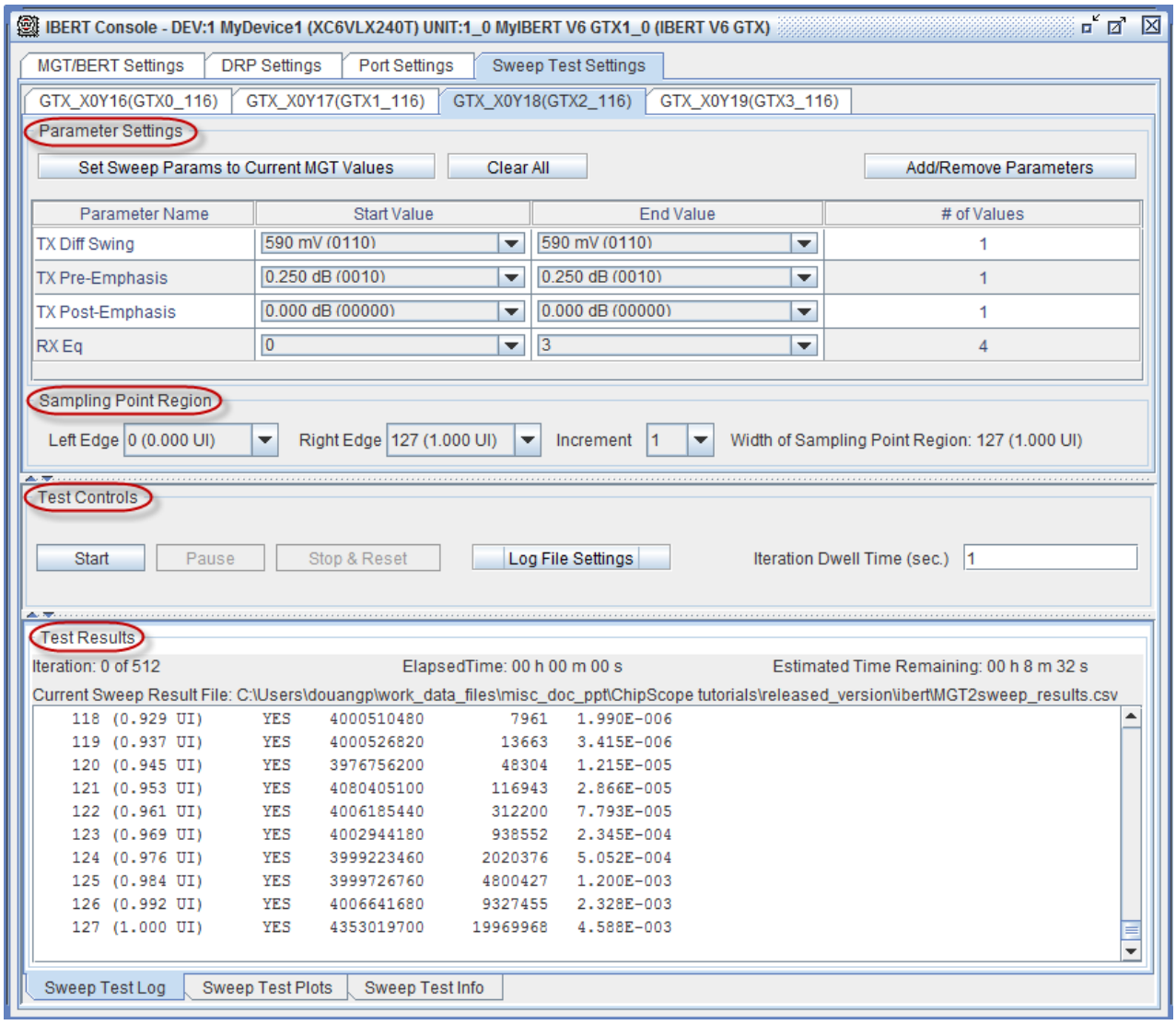

Figure 8: **Sweep Test Settings Panel**

Setting Up to Run the Sweep Test

1. From the IBERT Console, be sure the **Sweep Test Settings** tab is selected, as shown in Figure 8, above.
2. Select the **GTX_X0Y18 (GTX2_116)** transceiver.
3. Click **Add/Remove Parameters**. The **Add/Remove Ports/Attributes** dialog box appears.
4. In the **Add/Remove Ports/Attributes** dialog box, shown in Figure 9, select the parameters listed below and place them in the order shown.
   - **TX Diff Swing**
   - **TX Pre-Emphasis**
   - **TX Post-Emphasis**
   - **RX Eq**
5. Click **OK** to return to the **IBERT Console** window.

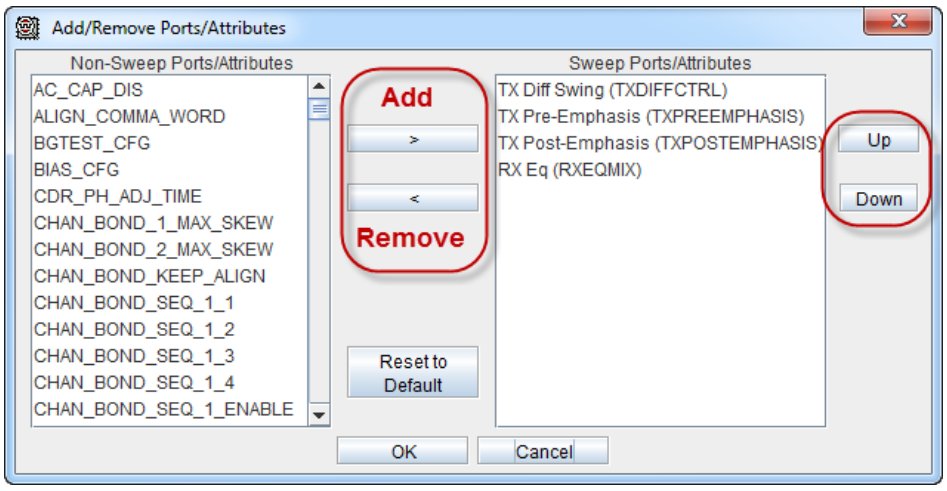

Figure 9: **Sweep Settings Options**

Note: The specified order of the parameters in the **Sweep Ports/Attributes** list dictates how the parameters are swept. The values of the parameters near the top of the list are swept less frequently than those near the bottom. In other words, the parameters near the top are in the outer loops of the sweep algorithm, while those near the bottom are in the inner loops of the sweep algorithm.

6. In the IBERT Console window, with the **Sweep Test Settings** tab selected, verify the Start and Stop values for each of the sweep parameters:

Parameter	Start Value	Stop Value
TX Diff Swing	590 mV	590 mV
TX Pre-Emphasis	0.25 dB (0.010)	0.25 dB (0.010)
TX Post-Emphasis	0.000 dB (0.000)	0.000 dB (0.000)
RX Eq	0	3

Note: In this tutorial, the only parameter to be swept is RX Eq (Receiver Equalizer). Others are set to constant values.

7. Verify that the **Sampling Point Region** is set from **0 (0.000 UI)** to **127 (1.00 UI)** with an increment of 1 second dwell time per iteration.

   Note: The Sampling Point Region represents the horizontal point within the eye to sample.

8. In the **Test Controls** area of the **Sweep Test Settings** panel, verify that **Iteration Dwell Time** is set to an increment of 1 second per iteration.

Running the Sweep Test and Viewing the Results

Click **Start** to begin sweeping test data. You can view test results in real time or in a log file.

- To view the test results in real time:

  Select the **Sweep Test Log** tab at the bottom of the IBERT Console to examine and observe sweep test results. For these sweep parameter settings, there are total of 512 iterations (Total Sample Points * Total Number of Sweep Values = 128 * 1 *1 *1 * 4 = 512).

- To view the test results log file:

  The test results are also written to a sweep test results file, which enables you to perform analysis later, offline. Click the **Log File Settings** button under the **Test Controls** panel to open a dialog box in which you can set both the location and name of the file.

Plotting the Data with the IBERT Sweep Plot GUI

Next, you will create a bathtub plot with multiple curves and visually compare the transceiver margin with different settings of the RX Eq parameter. If you were using software version 12.3 or earlier, you would use a separate spreadsheet software program to chart the graph, using the sweep data results obtained from previous steps. Starting in version 13.1, however, ChipScope Pro Analyzer includes an IBERT sweep plot GUI feature in the IBERT Console window.

About the IBERT Sweep Plot GUI

The IBERT Sweep Plot GUI:

- Allows you to plot a bathtub curve directly inside the console window once the sweep data is available.
- Helps you analyze the sweep data from the transceiver more efficiently, without having to use external spreadsheet software.
- Serves as a standalone mode, launching and reading in single or multiple sweep data files (comma separated values). Performs data analysis in a manner similar to the integrated mode. The standalone mode is helpful when you do not have access to a board and would like to analyze sweep data offline. The integrated mode requires that you connect to a live board locally or remotely.

Plotting the Bathtub Curve

1. Click the **Sweep Test Plot** tab at the bottom of the **Sweep Test Settings Panel** to plot a bathtub curve.

   Four bathtub plots display as shown in Figure 10. Some of the display options you can take advantage of include:

   - Plot single or multiple plots.
   - Move Left, Right, or BER Markers to examine a margin of each plot.
   - Display or hide plots (right click the plot number to the right of the plot graph).
   - Assign or change the line color.

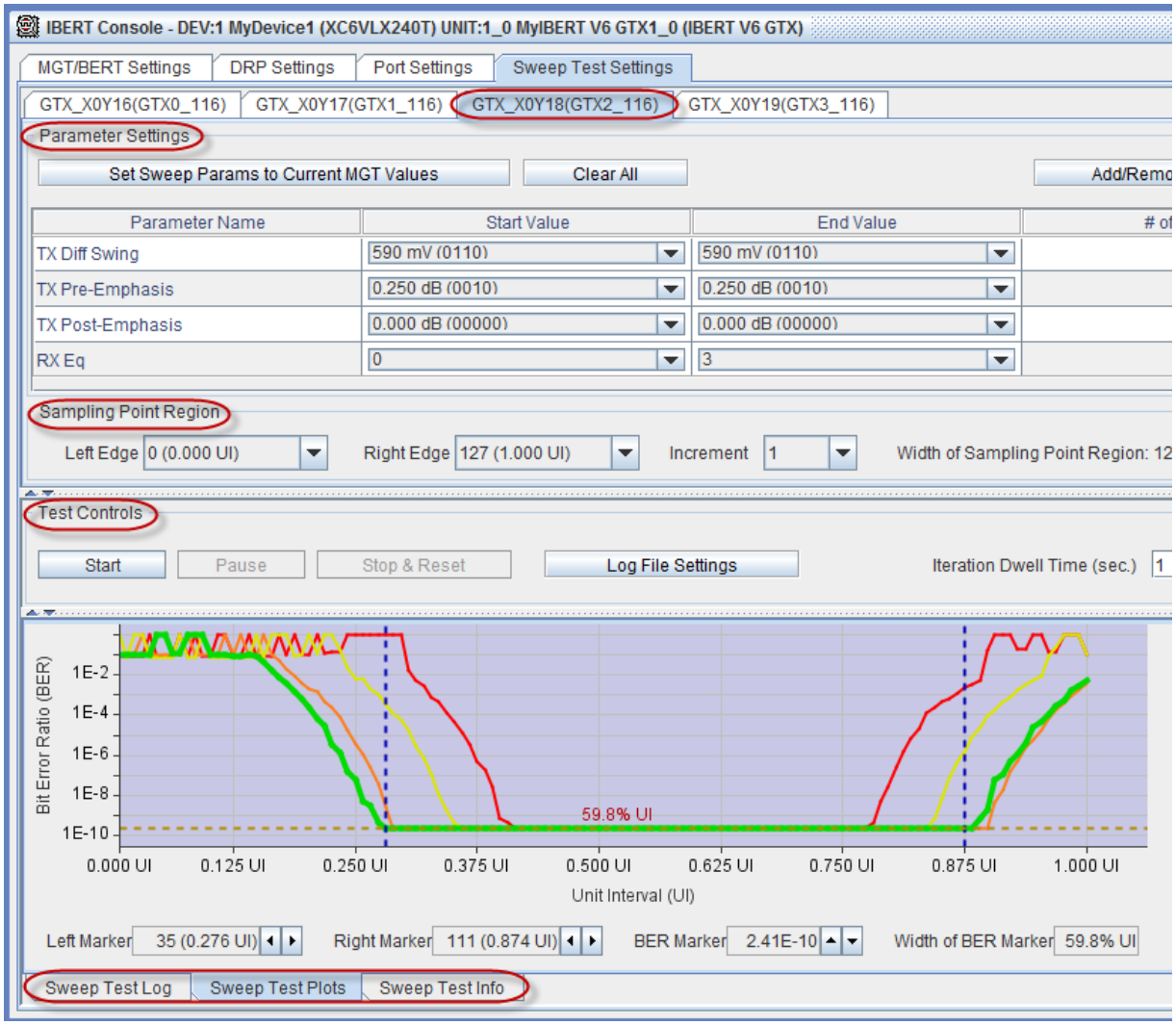

Figure 10: **Sweep Test Plots Display**

2. Click the **Sweep Test Info** tab, shown in Figure 11, and find the widest eye opening and/or highest margin.

You can sort the **Opening at Lowest BER Level** column. In this tutorial, plot 3 appears to have the biggest opening and the highest margin when the RX Eq parameter is set to 3.

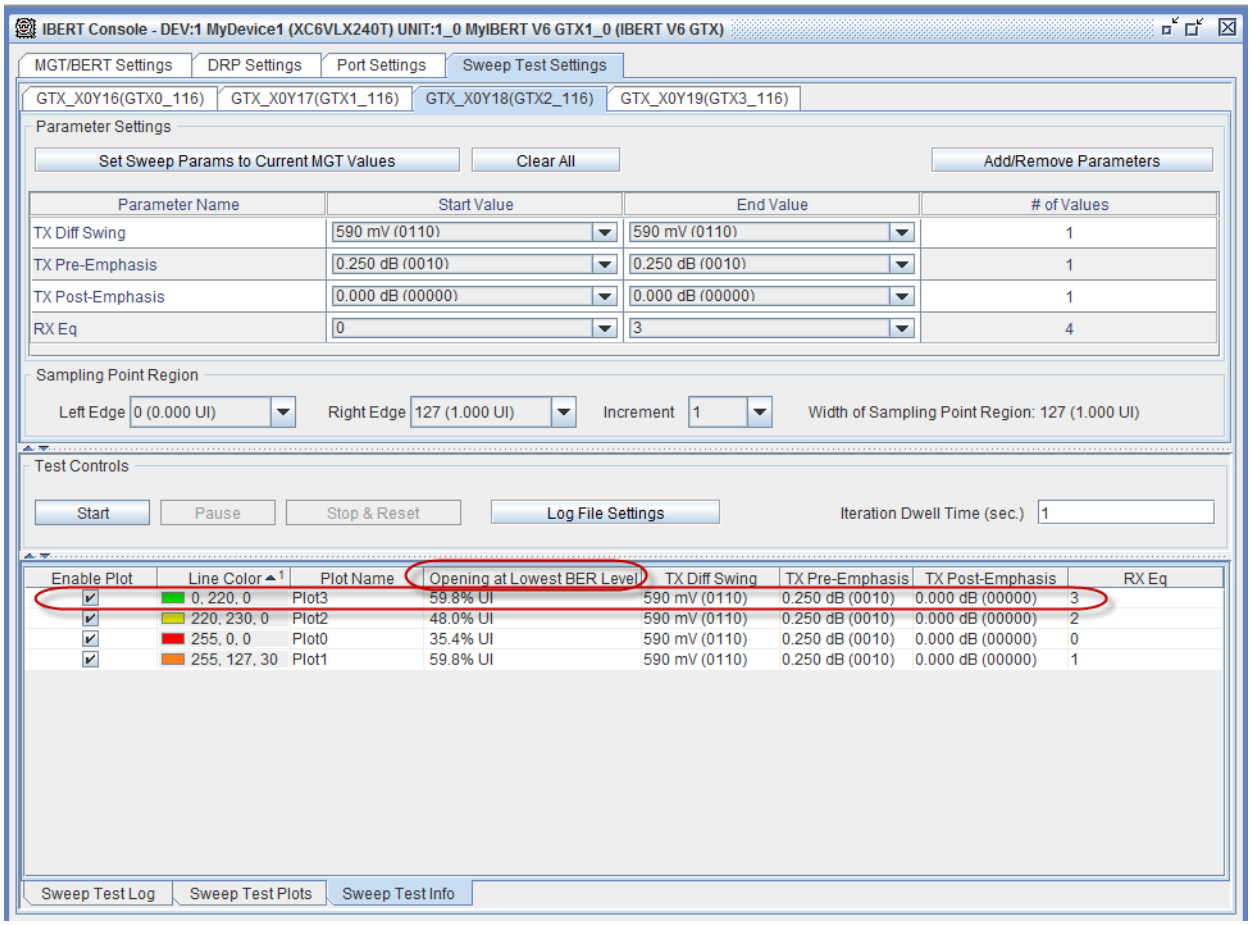

Figure 11: **Sweep Test Info Tab Display**

For additional information on running sweep tests, refer to the *ChipScope Pro Software and Cores User Guide* at http://www.xilinx.com/tools/cspro.htm.

XILINX®

Appendix

Additional Resources

Xilinx Resources

- **Xilinx® Documentation**: http://www.xilinx.com/support/documentation
- **Xilinx Glossary**: http://www.xilinx.com/support/documentation/sw_manuals/glossary
- **Xilinx Support**: http://www.xilinx.com/support

ChipScope Documentation

- ***ChipScope™ Pro Software and Cores User Guide*** *(UG029)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_3/chipscope_pro_sw_cores_ug029.pdf
- ***Using Xilinx ChipScope Pro ILA Core with Project Navigator to Debug FPGA Applications*** *(UG750)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_3/ug750.pdf

Board Documentation

- Virtex®-6 FPGA ML605 Evaluation Kit Information: http://www.xilinx.com/products/boards-and-kits/EK-V6-ML605-G.htm