## FPGA Design Flow Workshop

**Atlys Board**

The purpose of this workshop is to introduce you to the FPGA design flow using the ISE Foundation software, and is intended for University faculty who are new to Programmable Logic. During the course of the workshop, you will step through the complete Xilinx design flow from design entry to download. The workshop includes slides and labs to help guide you through the flow. The design used in the lab examples throughout the workshop makes use of the 8-bit PicoBlaze controller, which is used to illustrate how to take advantage of various board components.

1. **Install the Software**
* v12.3i ISE Software (submit online donation request form at XUP web)
* Install v12.3 Chipscope-Pro (submit online donation request form at XUP web)
1. Download and install software drivers, for serial communication using mini-USB2 cable, available at <http://www.exar.com/Common/Content/ProductDetails.aspx?ID=XR21V1410>
* Download and install Adept driver and software available at <http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,66,828&Prod=ADEPT2>
* Download and install the latest “Digilent Plugin for Xilinx Tools” available at <http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,66,768&Prod=DIGILENT-PLUGIN>
1. **Setup Hardware**
* Atlys board and power supply (see XUP donation request form)
* Mini USB cable for serial communication
1. **Install distribution**

The labsource.zip file contains KCPSM3.zip and labs.zip files. Unzip this on your local PC.

### Unzip the KCPSM3.zip file in c:\xup\fpgaflow directory. The KCPSM3.zip file includes the source code, assembler, and reference designs for PicBlaze controller. PicoBlaze is also available as free download from the Xilinx web.

* KCPSM3/Assembler **(**directory containing PicoBlaze assembler and template files)
* KCPSM3/Docs(directory containing user guides and user manuals for PicoBlaze)
* KCPSM3/JTAG\_loader(utility for downloading assembled program to FPGA memory – not used for workshop)
* KCPSM3/Verilog(directory containing Verilog source code for PicoBlaze and reference designs)
* KCPSM3/VHDL(directory containing VHDL source code for PicoBlaze and reference designs)

The labs.zip file consists of source files needed to conduct labs. Unzip the labs.zip file in c:\xup\fpgaflow\ directory.

The docs\_pdf.zip file contains lab documents and presentations in PDF format. Unzip this file in c:\xup\fpgaflow or any other directory of your choice.

1. **For Professors only**

Download the labsolution.zip and docs\_source.zip files using your membership account. Do not distribute them to students or post them on a web site. The docs\_source.zip file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get started**

Review the presentation slides and step through the lab instructions (see workshop flow below) to
gain hands-on experience with the Xilinx ISE Foundation tools. The lab exercises in this design make use of the PicoBlaze 8-bit micro-controller reference design provided with the PicoBlaze distribution.

1. **Contact XUP**

Please email xup@xilinx.com with questions or comments

**Outline**

Workshop flow (Day 1)

|  |  |  |
| --- | --- | --- |
| Presentations (.pptx) | Lab Exercises (.docx) | Lab Files (VHDL and Verilog) |
| 00\_course\_agenda |  |  |
| 11\_basic\_fpga\_arch |  |  |
| 12\_xilinx\_tool\_flow |  |  |
| 12a\_lab1\_intro | 01\_tool\_flow\_demo | Lab1 |
| 13\_ arwz\_and\_pins\_assgnmt |  |  |
| 13a\_lab2\_intro | 02\_arwz\_pins\_assgnmt\_demo | Lab2 |
| 14\_reading\_reports |  |  |
| 15\_global\_time\_const |  |  |
| 15a\_lab3\_intro | 03\_global\_time\_const | Lab3 |

Workshop flow (Day 2)

|  |  |  |
| --- | --- | --- |
| Presentations (.pptx) | Lab Exercises (.docx) | Lab Files (VHDL and Verilog) |
| 21\_ fpgaDsgnTech |  |  |
| 22\_synch\_des\_tech |  |  |
| 23\_synthesis |  |  |
| 23a\_lab4\_intro | 04\_Synthesis\_lab\_XST | Lab4 |
| 24\_impl\_options |  |  |
| 25\_coregen |  |  |
| 25a\_lab5\_intro | 05\_coregen\_lab | Lab5 |
| 26\_chipscope\_pro |  |  |
| 26a\_lab6\_intro | 06\_chipscope\_lab | Lab6 |