**Embedded System Design on Zynq using Vivado Workshop**

**ZedBoard**

**COURSE DESCRIPTION**

This workshop brings experienced FPGA designers up to speed on the capabilities and characteristics of the Xilinx Zynq All Programmable SoC family and Vivado design environment. Developing embedded systems using ARM Cortex-A9 processor and a set of soft peripherals is also included in the lectures and labs.

# Install Xilinx software

Professors may submit the online donation request form at <http://www.xilinx.com/member/xup/donation/request.htm> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* Vivado 2013.3 System Edition
* Download and install software driver, for serial communication using micro-USB cable, available at <http://www.zedboard.org>

1. **Setup hardware**

Connect ZedBoard

* 1. Connect programming cable between configuration port of ZedBoard and PC
  2. Connect another micro USB cable between ZedBoard’s UART port and PC USB port
  3. Connect the power supply and power on the board

1. **Install distribution**

Extract the labsource.zip file in c:\xup\embedded directory. This will generate **sources** and **labs** folder The docs\_pdf.zip file consists of lab documents and presentations in PDF format. Extract this zip file in c:\xup\embedded\ directory or any directory of your choice.

1. **For Professors only**

Download the labsolution.zip and docs\_source.zip files using your membership account. Do not distribute them to students or post them on a web site. The docs\_source.zip file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

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| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| Vivado Overview | 11\_Vivado\_overview.ppt x |
| Lab 1: Basic Hardware Design | 11a\_lab1\_intro.pptx  Lab1.docx |
| Zynq Architecture | 12\_zynq\_architecture.pptx |
| Extending Embedded System into PL | 13\_Extending\_Embedded\_System\_into\_PL.pptx |
| Lab 2: Adding IPs in PL | 13a\_lab2\_intro.pptx  Lab2.docx |
| Creating and Adding Custom IP | 14\_Creating\_and\_Adding\_Custom\_IP.pptx |
| Lab 3: Adding Custom IP in PL | 14a\_lab3\_intro.pptx  Lab3.docx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Software Development Environment | 21\_ Software\_Development\_Environment.pptx |
| Lab 4: Writing Basic Software Application | 21a\_lab4\_intro.pptx  Lab4.docx |
| Software Development and Debug using SDK | 22\_Software\_Development\_and\_Debug.pptx |
| Lab 5: Software Writing for Timer and Debugging | 23a\_lab5\_into.pptx  Lab5.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Basic Hardware Design: Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.

Lab 2 - Adding Peripherals in Programmable Logic: Extend the hardware system by adding AXI peripherals from the IP catalog.

Lab 3 - Creating and Adding Your Own Custom Peripheral: Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral.

Lab 4 - Writing Basic Software Application: Write a basic C application to access the peripherals.

Lab 5 - Software Writing for Timer and Debugging Using Software Development Kit (SDK): Use API to drive CPU's timer. Perform software debugging using SDK.

1. **Contact XUP**

Send an email to [xup@xilinx.com](mailto:xup@xilinx.com) for questions or comments