



WP286 (v1.1) October 13, 2011

Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits

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In the September 2005 issue of IEEE Transactions on Device and Materials Reliability, the article entitled *The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs* [Ref 1] described real-time experiments that evaluated large Xilinx FPGAs fabricated in two CMOS technologies (150 nm through 40 nm) for their sensitivity to radiation-induced, single-event upsets and detailed the results from simulation, beam testing, and atmospheric testing.

This white paper clarifies some open issues from the 2005 Xilinx Rosetta experiments and presents additional results for various technology nodes down to 40 nm.

Introduction

The *Stone of Rosette* by Ulrich Schabe and Richard Wäsch [Ref 2] defines Rosetta as follows:

“Rosetta refers to the crucial breakthrough in the research regarding Egyptian hieroglyphs. It especially represents the “translation” of “silent” symbols into a living language, which is necessary in order to make the whole content of information of these symbols accessible.”

Just as the Rosetta Stone enabled researchers to decode the unsolvable and mysterious Egyptian hieroglyphs by comparing them to the same text written in a known language, the Xilinx Rosetta experiments link two prior known and well-documented techniques of estimating atmospheric neutron single event upsets (SEUs) with the real effects of atmospheric neutrons on integrated circuits. The known techniques are accelerated testing in a neutron or proton beam and software simulation of the circuit to determine the critical charge a particular node or latch can handle before it changes state. These Xilinx experiments determine the actual upset rate of Virtex™ and Spartan™ FPGAs due to an atmospheric neutron cascade, which resulted from a cosmic ray. With a good understanding of the real effect(s) that these atmospheric neutrons have on today’s integrated circuits, Xilinx can validate the design and technology choices being used to mitigate these effects.

Predicting atmospheric neutron flux is not an exact science. In the JEDEC89A standard, there is a methodology that uses models and magnetic latitude data to predict the flux at any given location on the earth. The 2005 Rosetta results clearly did not agree with the original JEDEC89 standard, and the committee worked in collaboration with Xilinx to resolve this issue. Three corrections were made to the JEDEC89A standard:

1. Realization that the proton flux is not insubstantial (it is approximately an additional 7% in San Jose and as much as an additional 32% at Mauna Kea).
2. The attenuation by the building must be more accurately calculated (28% of the flux is lost to the ground floor of a typical Silicon Valley, two-story, tilt-up, concrete structure).
3. A more automated model can be developed to aid investigators (a new prototype web-based tool): <http://www.seutest.com/cgi-bin/FluxCalculator.cgi>.

The JEDEC89A revision also proposes a new atmospheric spectral model, based on work done by Goldhagen, et al [Ref 3].

Experiments

Each Rosetta experiment consisted of multiple sets of 100 of the largest Xilinx FPGAs using differing technologies, located at 10 different altitudes. All tested components were fabricated by UMC or Toshiba in their 300 mm submicron fabrication lines using standard logic CMOS processes and the new Triple Gate Oxide CMOS process.

[Table 1](#) lists the locations of the experiments, and [Table 2](#) lists the device type, technology, and quantity.

Table 1: Locations of Xilinx Rosetta Experiments

Location	Adjusted Altitude Factor ⁽¹⁾	Altitude (Feet)
San Jose, CA	0.75	257
Marseilles, France	1.08	359
Longmont, CO	4.11	4958
Albuquerque, NM	3.34	5145
Pic du Bure, France	6.00	8196
Pic du Midi, France	8.62	9298
Aiguille du Midi, France	12.45	11289
White Mountain, CA	19.48	12442
Mauna Kea, HI	11.35	13000
Rustrel, France	0.00	-1600

Notes:

- Adjustments have been made for the influence of minimum solar sunspots on cosmic ray flux.

Table 2: Devices Currently Under Test

Device Family	Device Number	Technology	Quantity
Virtex-II FPGAs	XC2V6000	150 nm	300
Virtex-II Pro FPGAs	XC2VP50	130 nm	600
Spartan-3 FPGAs	XC3S1500	90 nm	200
Spartan-6 FPGAs	XC6SLX150	45 nm	200
Virtex-4 FPGAs	XC4VLX25	90 nm	400
Virtex-4 FPGAs	XC4VLX60	90 nm	300
Virtex-5 FPGAs	XC5VLX110	65 nm	300
Virtex-6 FPGAs	XC6VLX240T	40 nm	300

Test times at Rustrel, France (which is 550 meters directly below the summit of a hill, and hence completely shielded from cosmic rays) have reached 2.35E6 device hours, and the alpha upset rate is 35 FIT/Mb⁽¹⁾. There has been one upset to date. Because these devices used ultra low alpha lead, the configuration cell upset rate due to alphas in the packaging was expected to be much less than 100 FIT/Mb. The manufacturing flow seems to have met this objective.

1. FIT/Mb = failures per billion hours per Megabit.

Recently, due to the latest technology and understanding of packaging material purity, an alpha-upset estimation was added for Virtex-6 and Spartan-6 FPGAs. See [UG116, Device Reliability Report](#), which is published quarterly, for the latest atmospheric and alpha data.

In the IC design of the Xilinx FPGAs, the individual memory cells (implemented as static latches) used for configuration, look-up tables, and block RAM were all simulated for their sensitivity to single event upsets.

To detect alpha contamination in packaging and assembly, the experimental groups were rotated through the three altitudes in addition to using the underground facility. Any evidence of a constant upset rate due to alpha particles would be observed as a non-altitude, non-latitude dependent factor in the resulting upsets, or measured directly at Rustrel.

Atmospheric Test Results

All atmospheric and alpha information is present in [UG116, Device Reliability Report](#), which is updated every quarter. The report summarizes the atmospheric and beam test results for all Xilinx FPGA device technologies. The error rate is stated either in failures in time (FIT) per billion hours or in mean time between events in hours, days, or years. A functional failure of the user data due to the single event upset rate then becomes mean time between functional failure in hours, days, or years. *Estimation of Single Event Upset Probability Impact of FPGA Designs* [Ref 4] discusses the relationship between the mean time between failure (MTBF) configuration bit and mean time between functional failure, which is exactly SEUPI⁽¹⁾. More commonly, the SEUPI factor is known as the derating factor (not every flip causes a failure).

Since on average, it takes from 10 to 100 upsets to actually cause a functional failure, determining the field failure rate of any design needs to be appropriately derated. The recommended worst-case estimate is to use a factor of ten (10) as the derating factor. An *essential bits* feature of the BitGen software tool provides a design-specific estimate of the de-rating for any design. In addition to the *Device Reliability Report*, Xilinx also provides a failures-in-time (FIT) rate calculator tool that helps customers to predict the FIT rate for their targeted device.

1. SEUPI = single event upset probability impact.

Q_{CRIT} Simulation

The Xilinx IC design group uses models and methods from Xilinx fabrication partners to estimate the potential sensitivity of the memory cells to upsets. These models and methods have been used in their production of standard products and ASICs. Their prediction of Q_{CRIT} to atmospheric upsets is used to compare with Xilinx observations in the Rosetta experiment.

Accelerator Test Facilities

In the past, the best resource available to simulate atmospheric neutrons had been the high-energy Neutron Testing Facility at the Los Alamos Neutron Science Center (LANSCE). At LANSCE, high-energy neutrons are produced by spallation. A linear accelerator produces an 800 MeV pulsed proton beam that strikes a water-cooled tungsten target. The impact produces a spectrum of neutrons whose energy distribution and intensity is precisely measured. This spectrum is very similar in shape to the atmospheric spectrum. The flight path consists of a small building for the irradiation that also encloses the testing equipment, isolated from the beam by a substantial concrete barrier. The devices to be tested are placed in the neutron beam line (in air) in the irradiation building. The experimenters control the neutron beam by opening and closing a shutter external to the irradiation building, and the number of neutrons on the sample is continuously monitored and recorded. Corrections to flux for the $1/R^2$ distance from the source must be included.

Additional tests were performed at TSL in Stockholm (pseudo-white neutron spectrum at different peak energies) and at the ISIS facility in the United Kingdom. In multiple visits to these locations, the data is self-consistent, but yields a different numerical result for a cross section of identical parts, tested under identical conditions. Six of the 150 nm technology devices (XC2V6000) have visited these locations, where the cross sections for configuration bits are:

LANSCE	$2.56E-14 \pm 10\%$
TSL	$3.38E-14, 2.41E-14$ to $4.35E-14$
ISIS	$4.35E-14 \pm 5\%$
Anita	$5.25E-14 \pm 7.5\%$

Accuracies are calculated either by variations in the results over many visits (more than 13 for LANSCE), from spectrum folding calculations (TSL) or from particle counter stated accuracy (ISIS), and represent the 95% confidence intervals. All tests had more than 5,000 actual upsets each, so that the inaccuracies due to counting of the number of events are less than $\pm 1\%$ for 95% confidence interval.

In the future, companies might have to use more than one beam facility due to beam availability issues. Xilinx has been using the 150 nm technology results as a *golden standard* for use in calibrating the results. This method is reliable because other technologies are measured at the same time in the same beam.

LANSCE Results

Testing is performed at LANSCE on a regular basis. See [UG116](#), *Device Reliability Report*, which is updated every quarter.

Conclusion

As the hardness to atmospheric neutrons improves, fewer upsets in the beam testing also occur, which affects the accuracy of the results, requiring longer beam exposures or resulting in higher statistical uncertainty.

It is not possible to make a statement about foundry, process, voltage, or temperature effects without side-by-side experiments in the same beam, at the same time, with a few thousand upsets on each. All data in [UG116](#), *Device Reliability Report*, meets these criteria.

The LANSCE facility now operates at one-third reduced beam power, so that one gets only a fraction of the number of upsets in the time allotted. It might not be possible to gather enough data depending on the upset rate and the beam time allotted.

Xilinx has 63MeV proton testing data on all products, including the 40 nm Virtex-6 devices. Proton testing is very inexpensive and correlates well with atmospheric neutrons. The proton data is available upon request from Xilinx.

For more information, go to:

<http://www.xilinx.com/products/quality/single-event-upsets.htm>

Acknowledgments

Xilinx extends appreciation to these facilities for their assistance with this document:

- The Los Alamos Neutron Science Center at the Los Alamos National Laboratory. This facility is funded by the U.S. Department of Energy under Contract W-7405-ENG-36.
- The California Institute of Technology Submillimeter Observatory at Mauna Kea, Hawaii.
- The White Mountain Research Station at White Mountain, California operated by the University of California Office of Research in San Diego, California.

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Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/10/08	1.0	Initial Xilinx release.
05/22/09	1.0.1	Changed footnote 1 on page 3. Was: FIT/Mb = failures per million hours per Megabit. Is: FIT/Mb = failures per billion hours per Megabit.
10/13/11	1.1	Updated document to reflect 40 nm technology node and added Virtex-6 and Spartan-6 FPGA data. Updated "Introduction," Table 2, Experiments, Atmospheric Test Results, Q_{CRIT} Simulation, Accelerator Test Facilities, Conclusion, Acknowledgments, and References sections.

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