

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

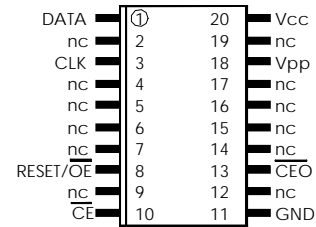
XC1701, XC1701L, XC1702L, XC1704L, & XC17512L Family

Description

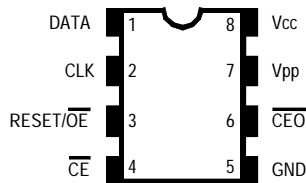
The XC1701, XC1701L, XC1702L, XC1704L, and XC17512L Serial Configuration PROMs provide easy-to-use, cost-effective configuration memory for Xilinx Field Programmable Gate Arrays.

These devices use a simple serial-access procedure to configure one or more LCA devices. The user can select the polarity of the reset function by programming a special bit. These devices are fully compatible and can be cascaded with other members of the XC1700 family of devices.

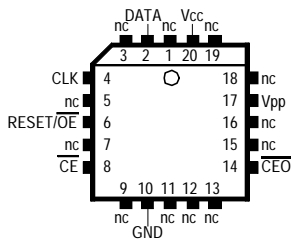
20-Pin SOIC Pin Assignments



8-Pin DIP Pin Assignments

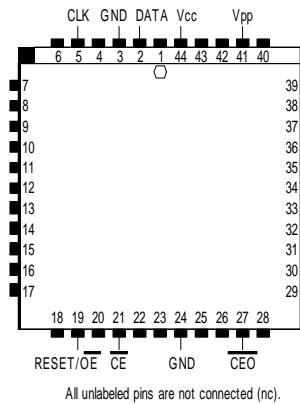


20-Pin PLCC Pin Assignments



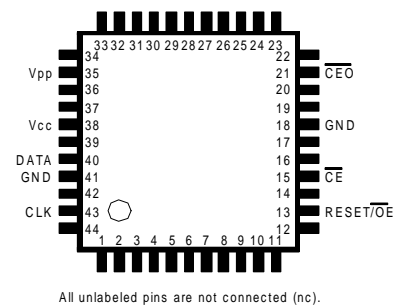
44-Pin CLCC Pin Assignments

XQ1701L Military Package Only



44-Pin VQFP Pin Assignments

XC1702L and XC1704L Only



XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC1701, XC1701L, XC1702L, XC1704L, & XC17512L Family

Programming Overview

The XC1701, XC1701L, XC1702L, XC1704L, and XC17512L devices are one-time programmable (OTP), devices organized as follows:

XC1701/L	1,048,576	x	1 bit
XC1702L	2,097,152	x	1 bit
XC1704L	4,194,304	x	1 bit
XC17512L	524,288	x	1 bit

All the XC1701, XC1701L, XC1702L, XC1704L, and XC17512L SPROMs are internally organized in rows, each row contains multiple 64-bit words. Additional non-data rows are used to read the Manufacturer's/Device ID and set the Reset Polarity and cannot be used to store configuration data. The device programmer should prompt the user for the desired Reset Polarity.

Figure 1 shows the flow of how the SPROMs are programmed. See Figure 2 for the programming cycle overview and Figure 4 for the details of the programming cycle.

Enter Programming Mode

The programming mode is entered by holding \overline{CE} and \overline{OE} High with V_{PP} at V_{PP1} for two rising clock edges, then lowering V_{PP} to V_{PPNOM} for one more rising clock edge (See Figure 3). Once in the programming mode, the following functions are available.

Read Manufacturer's/Device ID

All of the SPROMs contain a Manufacturer's and Device identification code. Prior to attempting to program or verify the device, the device programmer should read this code and verify that it is the correct code for the device selected by the user. If not, display message

“Manufacturer or Device ID Error.”

To read the Manufacturer's/Device identification code, first enter the programming mode. While holding \overline{CE} High and \overline{OE} Low, apply clock signals to the clock pin to access the ID row.

- For XC1701, XC1701L, XC17512L
19,791 clock signals
- For XC1702L, and XC1704L
65,632 clock signals

Then bring \overline{OE} High and \overline{CE} Low* . The first bit of the identification word is present when \overline{CE} goes Low and does not require a clock. Apply 15 additional clock signals to the CLK pin to read the complete device ID.

The Manufacturer's/Device ID

Consisting of 2 bytes of data. The first byte contains the JEDEC assigned Manufacturer's ID code for Xilinx (C9). The first four bits of the second byte define the density of the PROM, while the last four bits of the second byte contain specific programming algorithm information, currently:

- A for XC1701
- B for XC1701L, 02L, 04L, and 512L

The data is read out MSB first.

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The density codes are defined as follows:

XC1701 and XC1701L	D (1101)
XC1702L	3 (0011)
XC1704L	B (1011)
XC17512L	9 (1001)

Loading and Programming a Data Word

The data word is shifted into the SPROM, one bit at a time, on the rising edge of the clock, while \overline{CE} and \overline{OE} are High. The data word counter is temporarily held in internal latches until the address is advanced to the next address, and is programmed into the memory as an entire word upon strobing the device with V_{PP} at V_{PP1} for T_{PGM} .

The contents of the data word must now be verified at V_{PP2} . The data word is read while lowering \overline{CE} and capturing the data while clocking the device 63 times. The first bit of the word (LSB) is present when \overline{CE} goes low. After all 64 bits were read, bring \overline{CE} high and compare the data to the original file data. If the data does not compare, stroke V_{PP} at V_{PP1} for T_{PGM1} . (Note, the original data is still contained in internal latches and does not have to be loaded into the device again.) Read the data word again (as described above) and compare it to the original data. If it still does not compare, pulse V_{PP} at V_{PP1} for T_{PGM1} . Now read the data word again. If it still does not compare, power the device down and issue message: "Device Failed to Program". See Figure 4. If the word compares, increment the word counter as described below.

Increment the Address (Word) Counter

After successfully programming a data word, the address counter must be incremented. This is done on the rising edge of the clock while \overline{CE} is High and \overline{OE} is Low.*

* Be careful not to have \overline{CE} and \overline{OE} Low at the same time, as this causes the device to exit programming mode.

Set RESET Polarity

The polarity of the Reset/ \overline{OE} pin may be made active Low by writing zeros into a dedicated row. (See Figure 5).

Reset/ \overline{OE} is located outside of the user data array. Enter the programming mode, then lower Reset/ \overline{OE} , hold the Data pin Low, strobe the clock.

- 16,384 times for XC1701, XC1701L, and XC17512L.
- 65,536 times for XC1702L and XC1704L .

Raise the Reset/ \overline{OE} pin, load the data latches with all zeros (see Load a Data Word above), and strobe V_{PP} at V_{PP1} for T_{PRST} .

The reset polarity has to be verified (sensed) at V_{PP2} while in programming mode. To sense the polarity bit, after strobing V_{PP} for T_{PRST} , set \overline{CE} low and sense the $\overline{CE0}$ pin. If $\overline{CE0}$ is high, reset is active low (successfully programmed). If $\overline{CE0}$ is low, reset is active high (failed to program).

Writing ones or not writing anything maintains RESET active High.

Note:

The Reset Polarity is actually only the MSB of the data word.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC1701, XC1701L, XC1702L, XC1704L, & XC17512L Family

Sensing RESET Polarity

To sense or read the polarity of the Reset/ \overline{OE} pin, enter the programming mode, then lower Reset/ \overline{OE} , hold the Data pin High, then strobe the clock.

- 16,384 times for XC1701, XC1701L, and XC17512L.
- 65,536 times for XC1702L and XC1704L.

Set Reset/ \overline{OE} High, set \overline{CE} Low and sense the \overline{CE} pin. If \overline{CE} is High, Reset is active Low. If \overline{CE} is Low, Reset is active High. The reset polarity bit is active high by default (unprogrammed). When the reset bit is programmed, the “reset” polarity is active low.

Exit Programming Mode

To exit the programming mode, remove power from the device, per Figure 6.

Stand Alone Verify Of Data Bits

(Normal Mode)

The verify operation should be performed after programming. Power up the device and read the data bits out serially in normal readout mode (see Figure 7). A margin voltage (difference between V_{PP} and V_{CC}) is applied to the device to ensure charge retention on each programmed bit. Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY} . When in normal mode, the Reset/ \overline{OE} signal should be driven active high if the reset polarity bit was unprogrammed (logic “1”). It should be driven active low if the reset polarity bit was programmed (logic “0”).

At the end of the verify operation the programmer must confirm that the \overline{CE} pin has gone Low one clock after the last bit is read out.

If the data fails to verify, display message “**Failed Margin Verify**”. If the data verifies, display message “**Device Passed**”.

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Programming Mode Pin Assignments

Dip Pins	PLCC Pins	SOIC Pins	CLCC Pins	VQFP Pins	Name	I/O	Description
1	2	1	2	40	Data	I/O	The rising edge of the clock shifts a data word in or out of the SPROM one bit at a time.
2	4	3	5	43	CLK	I	Clock input. Used to increment the internal address/word counter for reading and programming.
3	6	8	19	13	Reset/ \overline{OE}	I	The rising edge of CLK shifts a data word into the PROM when \overline{CE} and \overline{OE} are High; it shifts a data word out of the PROM when \overline{CE} is Low and \overline{OE} is High. The address/word counter is incremented on the rising edge of CLK while \overline{CE} is held High and \overline{OE} is held Low. Note: Any modified polarity of the RESET/ \overline{OE} pin is ignored in the programming mode.
4	8	10	21	15	\overline{CE}	I	The rising edge of CLK shifts a data word into the PROM when \overline{CE} and \overline{OE} are High; it shifts a data word out of the PROM when \overline{CE} is Low and \overline{OE} is High. The address/word counter is incremented on the rising edge of CLK while \overline{CE} is held High and \overline{OE} is held Low.
5	10	11	3 / 24	18 / 41	GND		Ground pin
6	14	13	27	21	\overline{CEO}	O	The polarity of the RESET/ \overline{OE} pin can be read by sensing the \overline{CEO} pin. Note: The polarity of the RESET/ \overline{OE} pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
7	17	18	41	35	V_{PP}		Programming Voltage Supply. Programming mode is entered by holding \overline{CE} and \overline{OE} High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PPNOM} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration T_{PGM} or T_{PGM1} . V_{PP} must be held at V_{CC} for normal operation.
8	20	20	44	38	V_{CC}		V_{CC} power supply input.

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AC Programming Specifications

Symbol		Description	Min	Rec	Max	Units
1	T_{RPP}	10% to 90% rise time of V_{PP}		5		μs
2	T_{FPP}	90% to 10% fall time V_{PP}		5		μs
3	T_{PGM}	First V_{PP} programming pulse width	90	100		μs
4	T_{SVC}	V_{PP} setup to CLK for entering programming	100			Ns
5	T_{HVC}	V_{PP} hold from CLK for entering programming	300			Ns
6	T_{SDP}	Data setup to CLK for programming	50			Ns
7	T_{HDP}	Data hold from CLK for programming	0			Ns
8	T_{SCC}	\overline{CE} setup from programming/verifying	100			Ns
9	T_{ON}	Reset Pulse Width		5		Ms
10	T_{SCV}	\overline{CE} hold from CLK for programming/verifying	100			Ns
11	T_{HCV}	\overline{CE} hold from V_{PP} for programming	50			Ns
12	T_{SIC}	\overline{OE} setup to CLK for incrementing address	100			Ns
13	T_{HIC}	\overline{OE} hold from CLK for incrementing address	0			Ns
14	T_{CAC}	CLK to data valid			400	Ns
15	T_{OH}	Data hold from CLK	0			Ns
16	T_{CE}	\overline{CE} low to data valid			250	Ns
17	T_{PGM1}	Second V_{PP} programming pulse width XC1701/01L & XC17512L	480	500		μs
		XC1702L & XC1704L	180	200		μs
18	T_{PRST}	Reset Polarity programming pulse width XC1701/01L & XC17512L		5		ms
		XC1702L & XC1704L		400		μs

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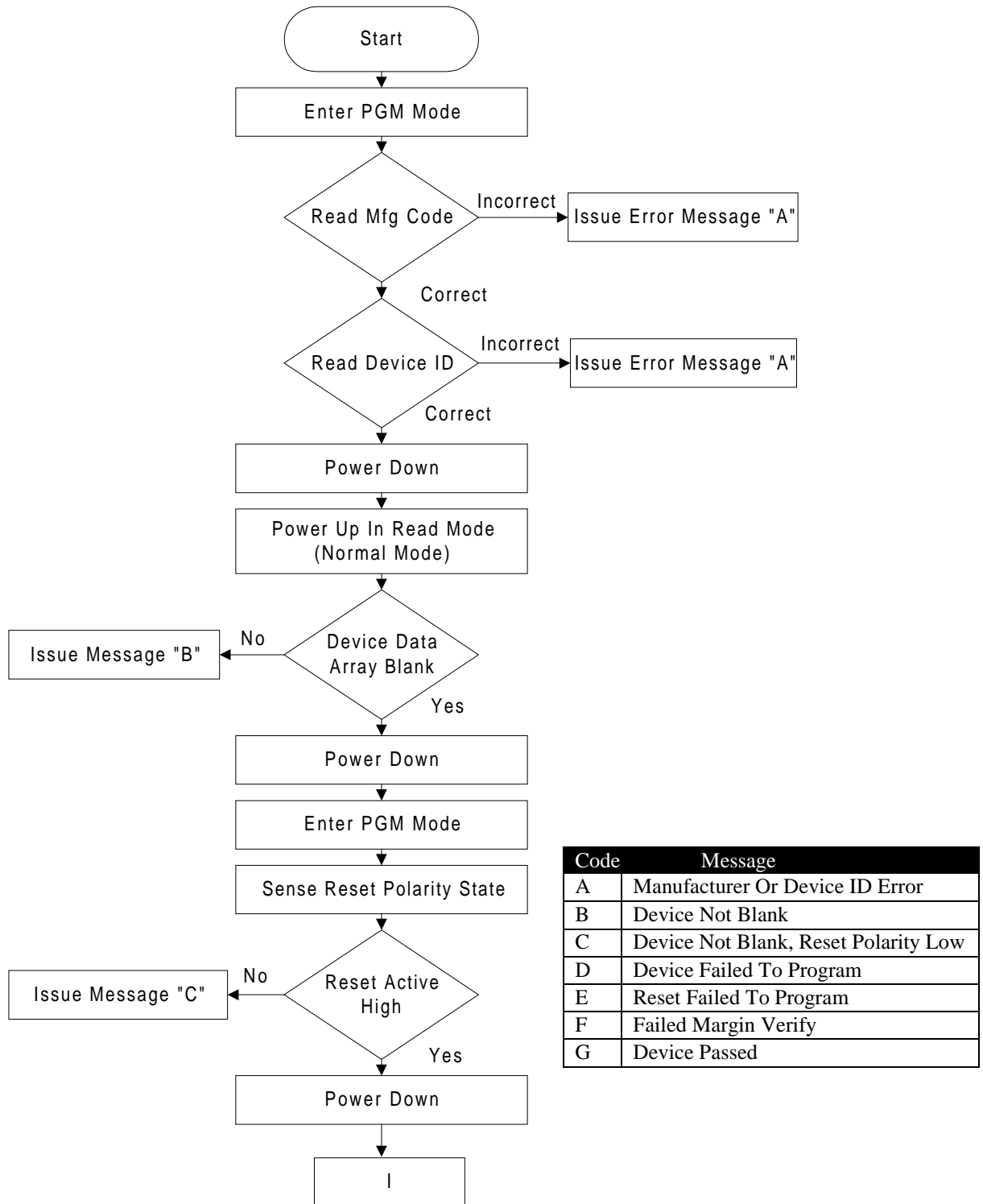


Figure 1. Programming Flow

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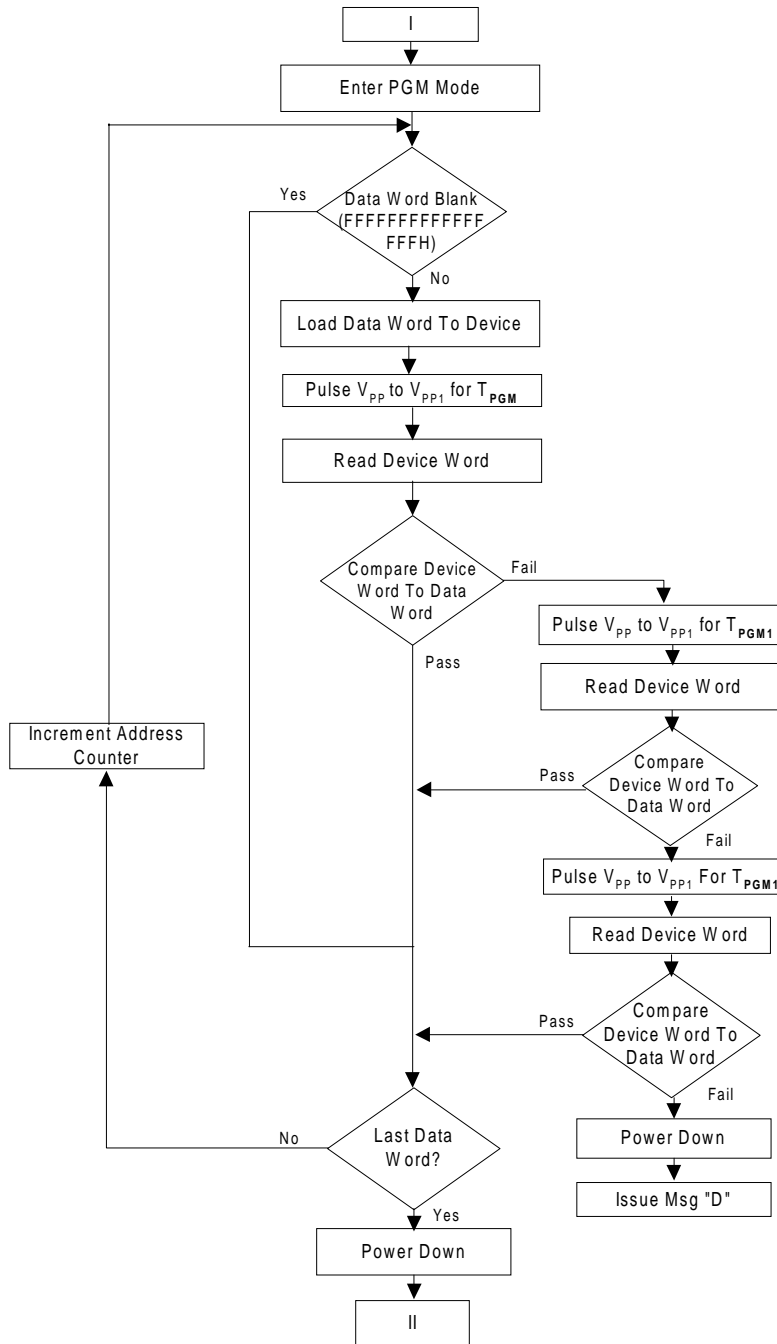


Figure 1. Programming Flow (Continued)

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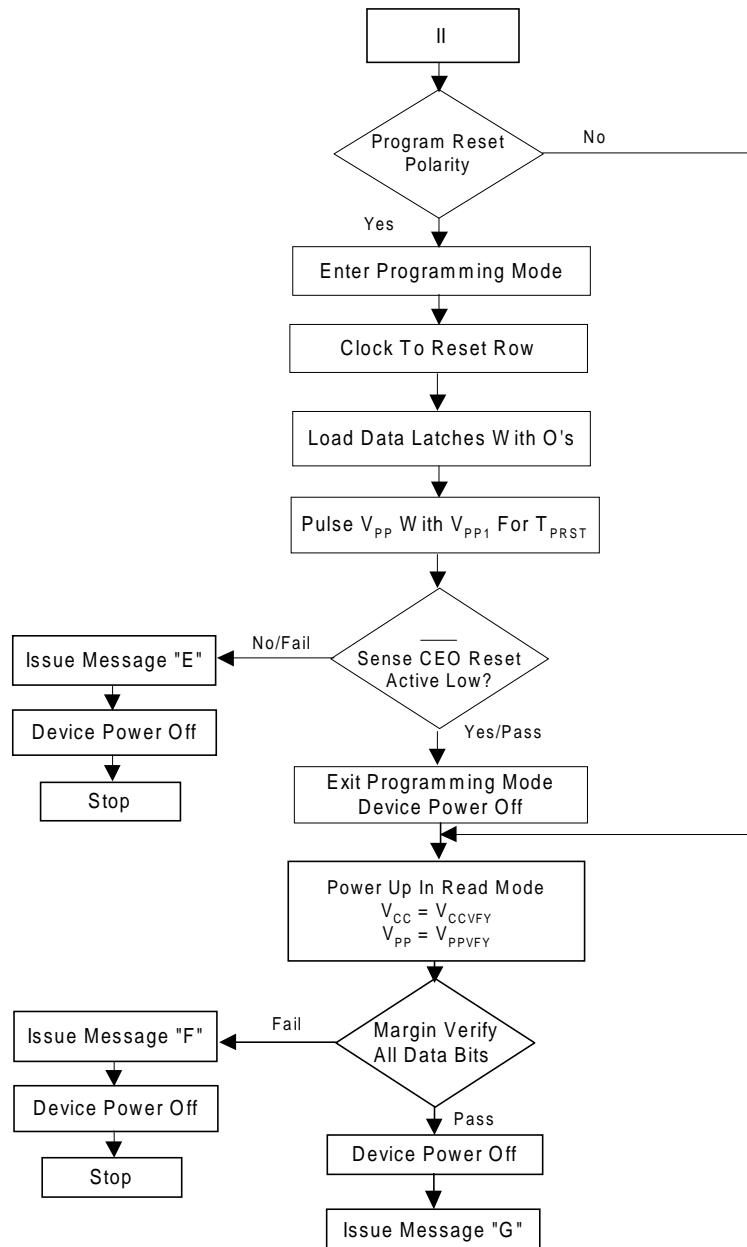


Figure 1. Programming Flow (Continued)

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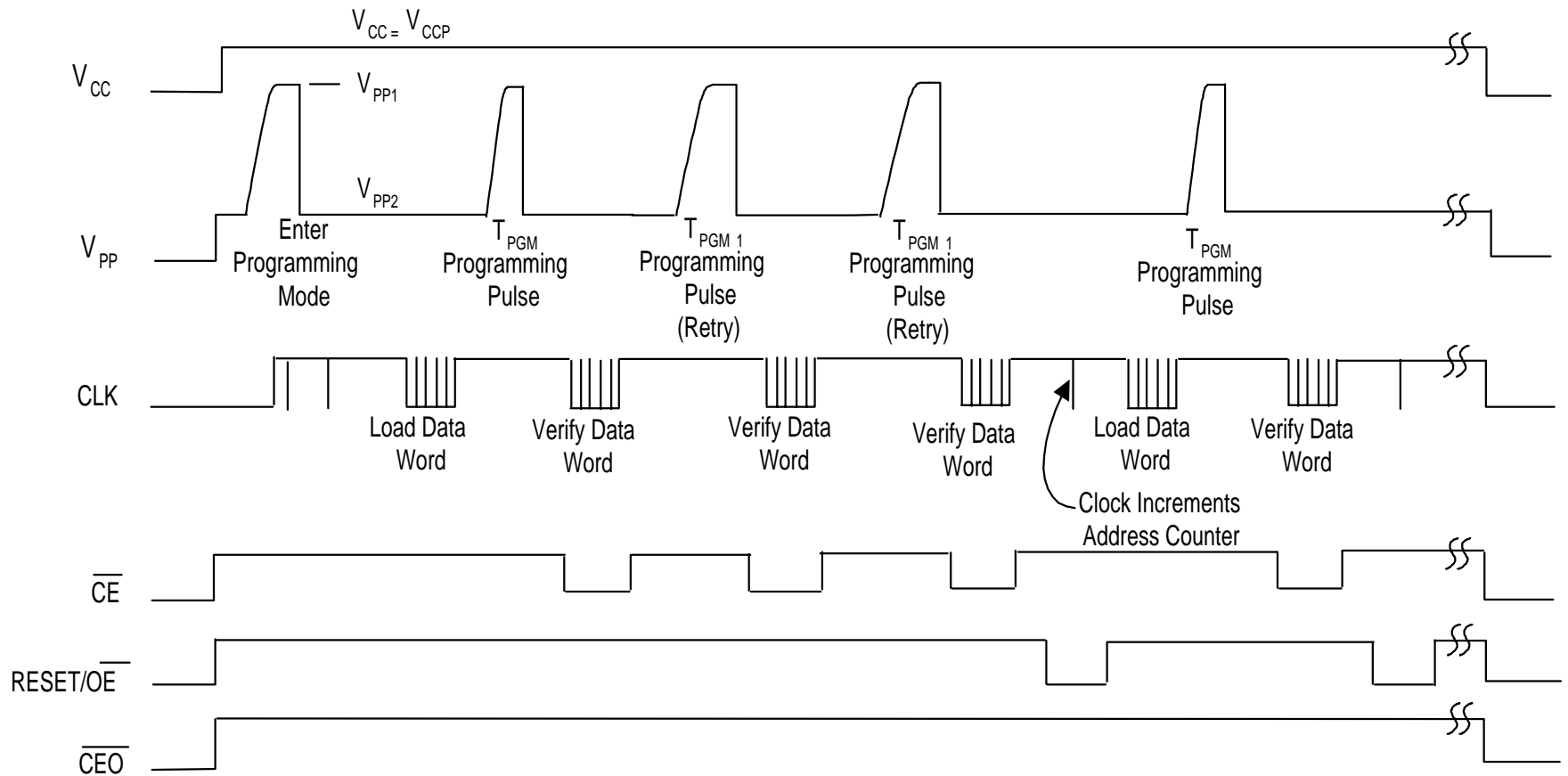


Figure 2. Programming Cycle Overview

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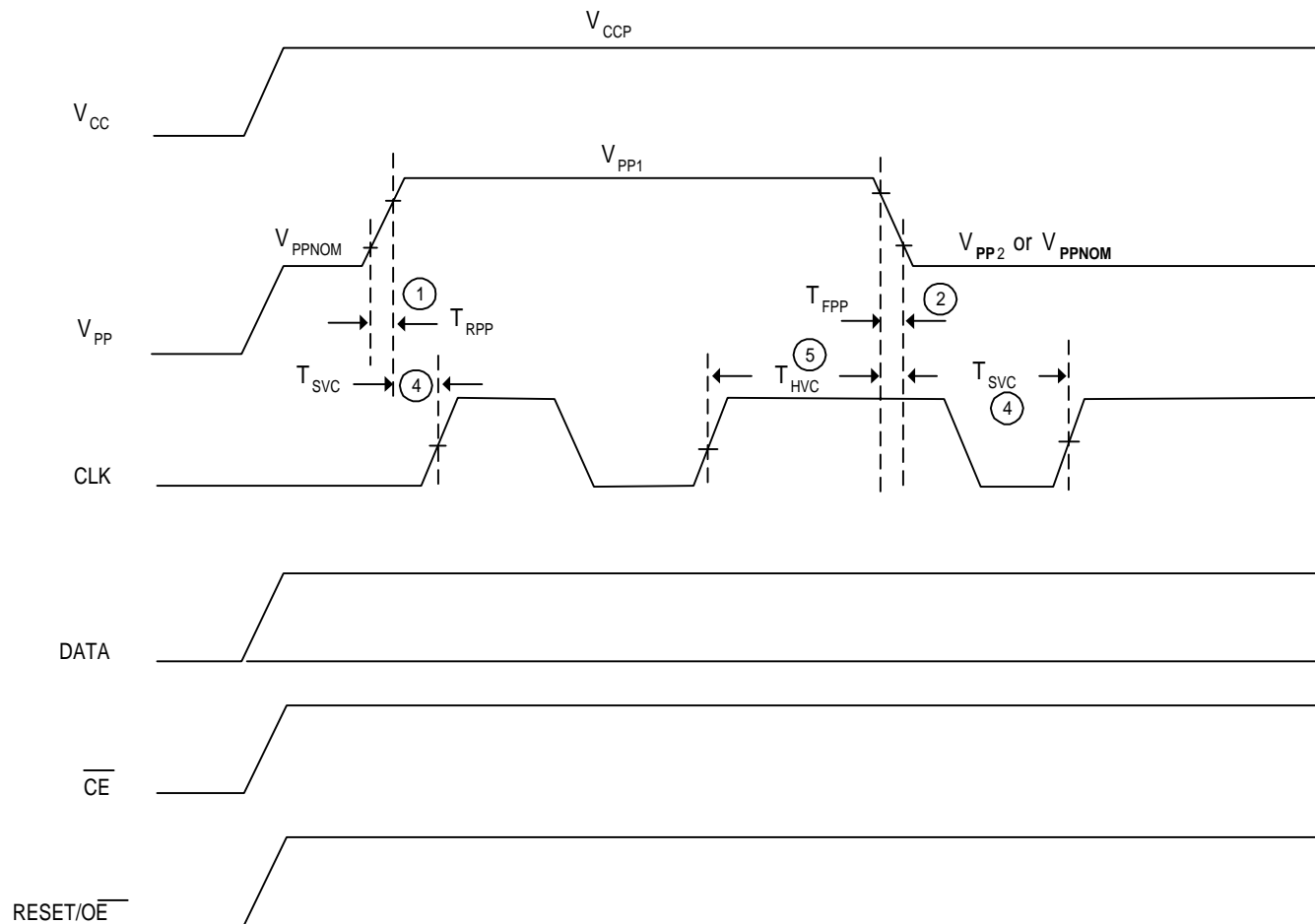


Figure 3. Enter Programming Mode

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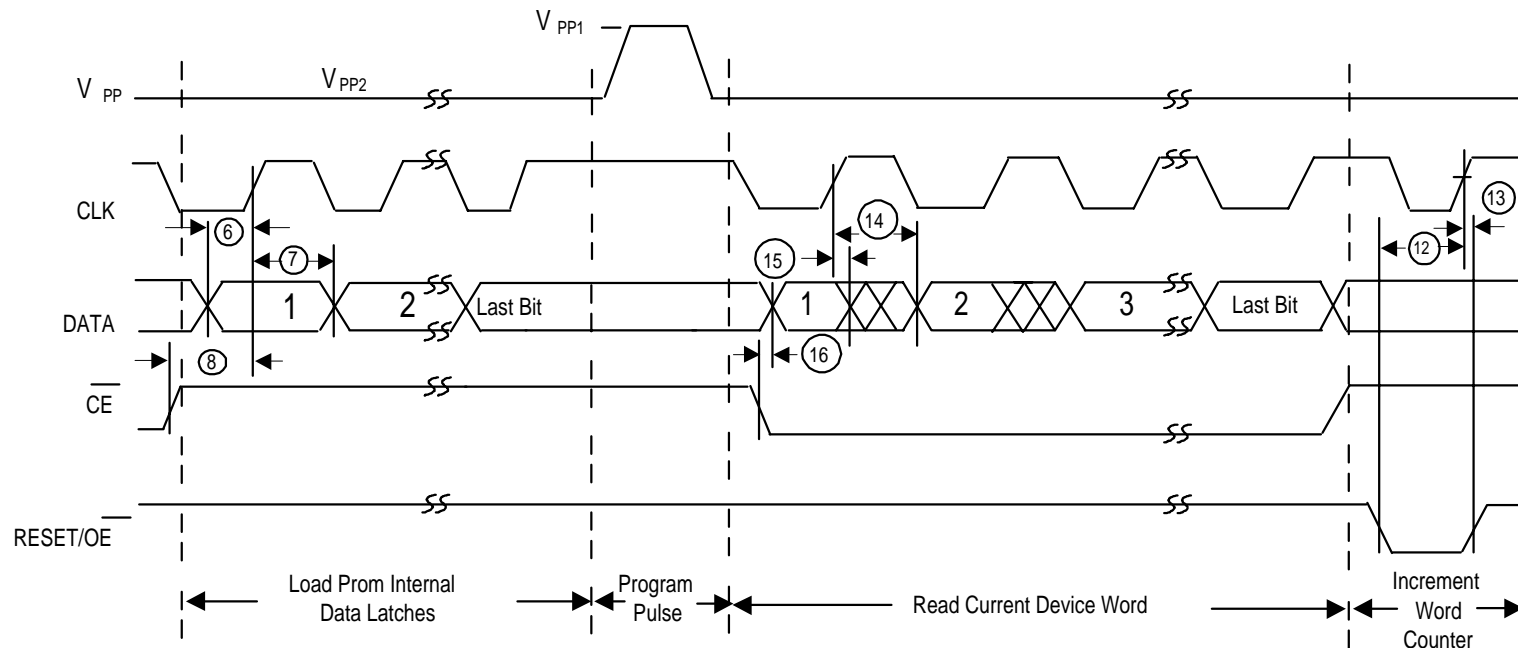


Figure 4. Details Of The Programming Cycle

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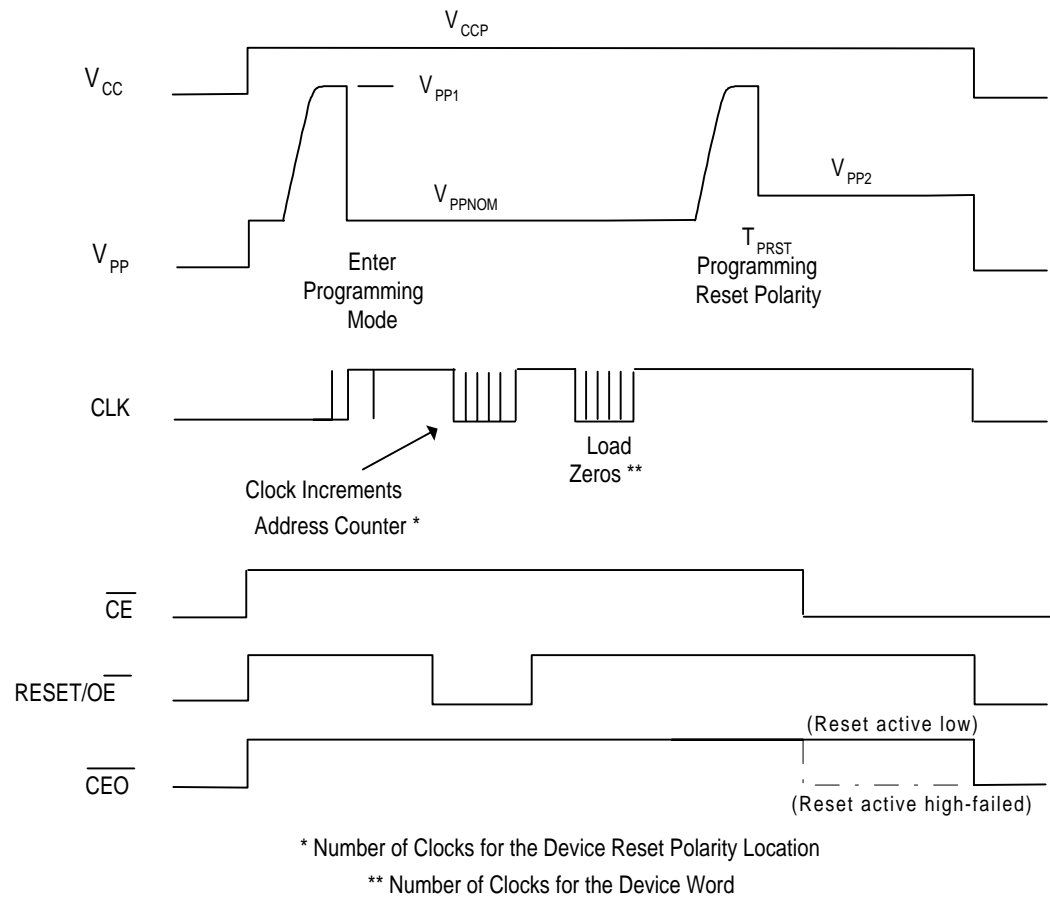
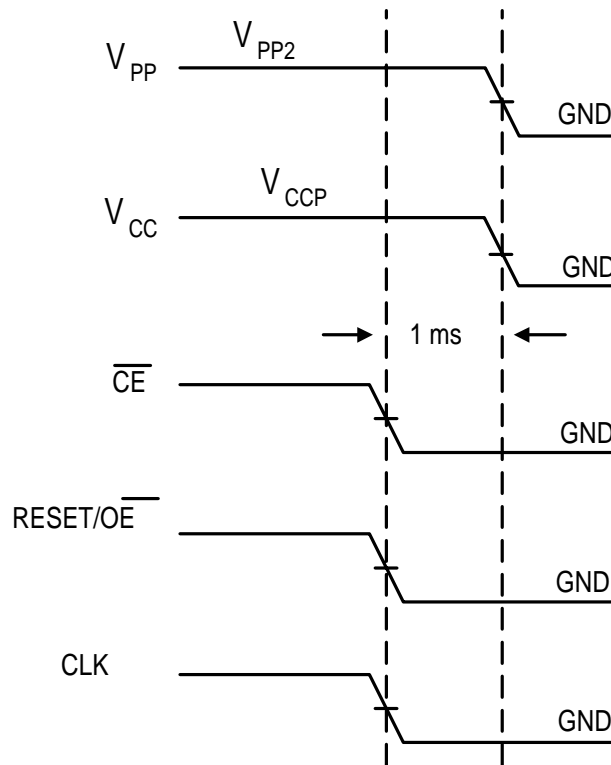


Figure 5. Programming Reset Polarity

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If your programming hardware does not allow V_{PP} and V_{CC} to power up and down simultaneously, make sure to first power up V_{PP} during power up and power down V_{PP} after V_{CC} during power down.

Figure 6. Exit Programming Mode

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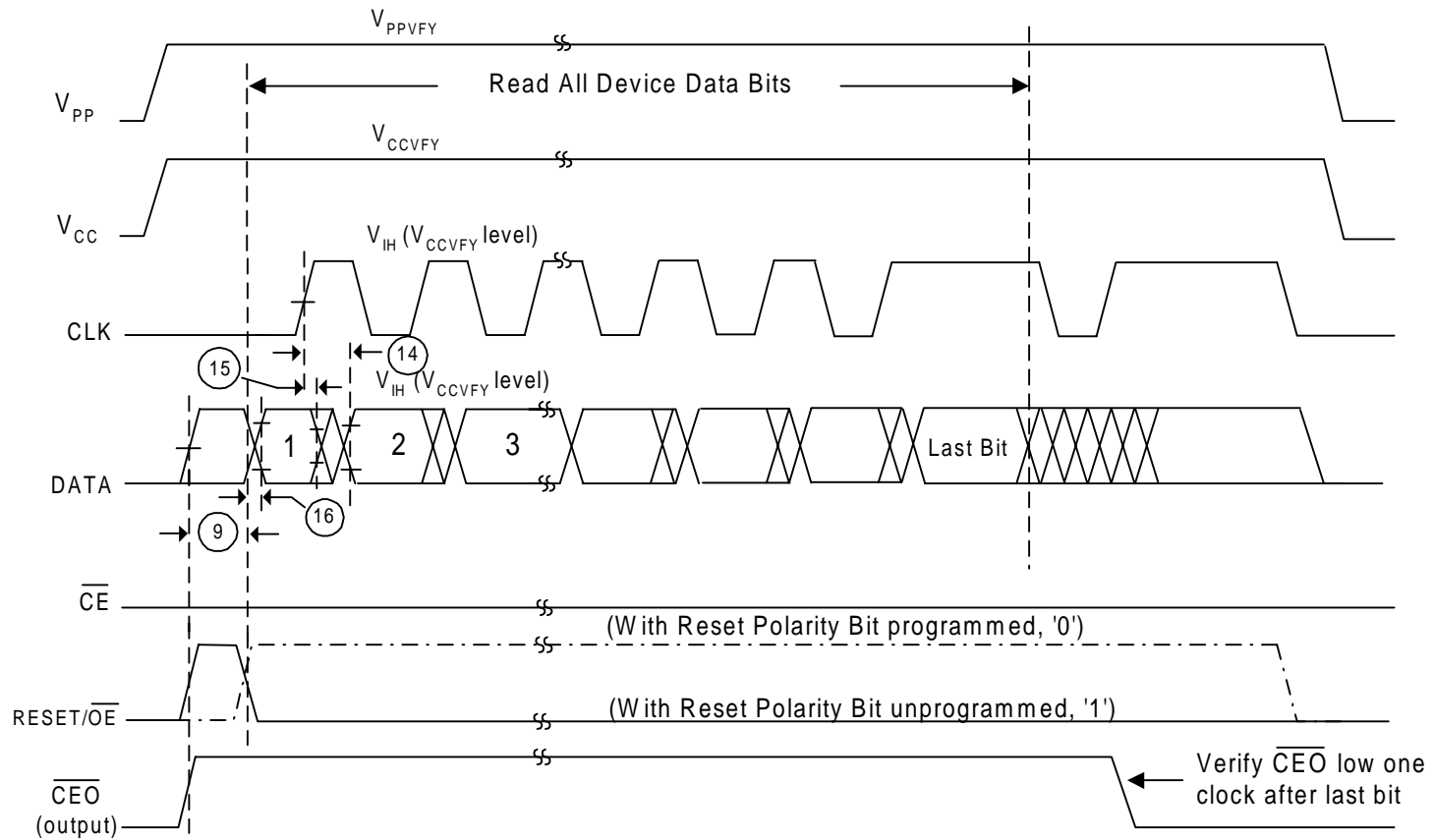


Figure 7. Details Of Verify Cycle