
XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC17V08, XC17V16 Family

Description

The XC17V08 and XC17V16 Configuration PROMs provide easy-to-use, cost-effective configuration memory for Xilinx Field Programmable Gate Arrays.

These devices use a simple serial-access or by eight access procedure to configure one or more LCA devices. The user can select the polarity of the reset function by programming a special bit. In addition, the internal pull-down resistor on the BUSY pin may be enabled and the express mode enabling eight outputs can be activated using other programmable user bits. These devices are fully compatible and can be cascaded with other members of the XC17V00 and XC17S00A family.

Pin Assignments:

Function	Pin-out for VQ44	Pin-out for PC44/CC44
Vpp	35	41
Vcc	8,16,17,26,36,38	14,22,23,32,42,44
Gnd	6,18,28,37,41	3,12,24,34,43
CLK	43	5
\overline{CE}	15	21
Reset/ \overline{OE}	13	19
BUSY *	24	30
$\overline{CE0}$	21	27
D0	40	2
D1	29	35
D2	42	4
D3	27	33
D4	9	15
D5	25	31
D6	14	20
D7	19	25

NOTE: Unlike other members of the XC17V00 family of PROM devices, the BUSY line should be pulled down or grounded on the XC17V08 and XC17V16 adapter for the programmer.

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Programming Overview

The XC17V08 and XC17V16 devices are one-time programmable (OTP), devices organized as follows:

XC17V16

16,777,216 X 1 bit

2,097,152 X 8 bit (in express mode)

XC17V08

8,388,608 X 1 bit

1,048,576 X 8 bit (in express mode)

The XC17V08 and XC17V16 PROMs are internally organized in rows, each row containing multiple 128 bit words. Additional non-data rows are used to read the Manufacturer's/Device ID and set the Reset Polarity and cannot be used to store configuration data. The device programmer should prompt the user for the desired Reset Polarity, output mode and busy mode. Figure 1 shows the flow of how the PROMs are programmed. See Figure 2 for the programming cycle overview and Figure 4 for the details of the programming cycle.

Perform Blank Check

Power up the device and read the data bits out bit-by-bit in normal serial readout mode (see Figure 7) Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY} . When in normal mode, the Reset/ \overline{OE} signal should be driven active high if the reset polarity bit was unprogrammed (logic "1"). It should be driven active low if the reset polarity bit was programmed (logic "0").

At the end of the read operation the programmer must confirm that the \overline{CEO} pin has gone low one clock after the last bit is read out.

If the data fails to read logic "1", display the message "Failed Blank Check". If the data verifies, display the message "Device Passed".

Enter Programming Mode

The programming mode is entered by holding \overline{CE} and \overline{OE} High with V_{PP} at V_{PP1} for two rising clock edges, then lowering V_{PP} to V_{PPNOM} for one more rising clock edge (See Figure 3). Once in the programming mode, the following functions are available.

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Read Manufacturer's/Device ID

All of the PROMs contain a Manufacturer's and Device identification code. Prior to attempting to program or verify the device, the device programmer should read this code and verify that it is the correct code for the device selected by the user. If not, display message "**Manufacturer or Device ID Error.**"

To read the Manufacturer's/Device identification code, first enter the programming mode. While holding \overline{CE} High, \overline{OE} Low, apply 131,168 clock signals to the clock pin to access the ID row.

Then bring \overline{OE} High and \overline{CE} Low*. The first bit of the identification word is present when \overline{CE} goes Low and does not require a clock. Apply 15 additional clock signals to the CLK pin to read the complete device ID from the DATA0 pad.

The Manufacturer's/Device ID

Consisting of 2 bytes of data. The first byte contains the JEDEC assigned Manufacturer's ID code for Xilinx (C9). The first four bits of the second byte define the density of the PROM, while the last four bits of the second byte contain specific programming algorithm information, currently:

C for XC17V08 and XC17V16

The data is read out MSB first.

The density codes are defined as follows:

XC17V08 6(0110)

XC17V16 7(0111)

Loading and Programming a Data Word

The data word is shifted into the SPROM from DATA0, one bit at a time, on the rising edge of the clock, while \overline{CE} and \overline{OE} are High. The data word counter is temporarily held in internal latches until the address is advanced to the next address, and is programmed into the memory as an entire word upon strobing the device with V_{PP} at V_{PP1} for 100 μ s.

Program Verify a Data Word

The contents of the data word must now be verified at V_{PP2} . The data word is verified from DATA 0 while lowering \overline{CE} and capturing the data while clocking the device 128 times. The first bit of the word (LSB) is present when \overline{CE} goes low. A margin voltage (difference between V_{PP} and V_{CC}) is applied to the device to ensure charge retention on each programmed bit. Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY} . When reading data in verify mode, the Reset/ \overline{OE} signal should be driven active high while the \overline{CE} signal should be driven active low. After all 128 bits were read, bring \overline{CE} high and compare the data to the original file data. If the data does not compare, retry programming the data word by applying another programming pulse of V_{PP} at V_{PP1} for 100 μ s. Two retries should be allowed. If the data still does not compare, power the device down and issue the message: "Device Failed to Program". See Figure 1. If the word compares, increment the word counter as described below.

Increment the Address (Word) Counter

After successfully programming a data word, the address counter must be incremented. This is done on the rising edge of the clock while \overline{CE} is High and \overline{OE} is Low.

Setting user bits: RESET Polarity, activate express mode or enable a BUSY Pull-down

The polarity of the Reset/ \overline{OE} pin may be made active low, the internal pull-down resistor on the BUSY pin may be enabled and the express mode enabling eight outputs can be activated by writing zeros into a dedicated location (See Figure 5). These special mode bits are located outside of the user array. In order to program these mode bits, you need to follow the following sequence. 1) Enter the programming mode 2) lower Reset/ \overline{OE} while holding the Data pin Low 3) strobe the clock (131,072 times for the Reset/ \overline{OE} polarity or 131,264 times for the enabling of BUSY pull-down or 131,232 times to turn on the express mode option) 4) raise the Reset/ \overline{OE} pin 5) load the data latches with all zeros (see Load a Data Word above), and 6) strobe V_{PP} at V_{PP1} for T_{PGM} . These special mode bits have to be verified (sensed) at V_{PP2} while in programming mode.

Note:

The user bits actually only require the MSB of the data word to be programmed. Be careful not to have \overline{CE} and \overline{OE} Low at the same time, as this causes the device to exit programming mode.

Sensing or verifying user bits: RESET, express mode or BUSY Pull-down enable

To sense or verify the polarity of the user bits 1) enter the programming mode 2) lower Reset/ \overline{OE} while holding the Data pin High 3) strobe the clock (131,072 times for the sensing the Reset/ \overline{OE} polarity, 131,232 times to sense the express mode option or 131,264 times to determine if the BUSY pull-down is enabled) 4) set Reset/ \overline{OE} High 5) set \overline{CE} Low and 6) sense the \overline{CEO} pin. If \overline{CEO} is High, the user bit is programmed. If \overline{CEO} is Low, the user bit is unprogrammed (default). The following table describes the effect of programming the user bits:

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	<u>Unprogrammed (default)</u>	<u>Programmed</u>
Reset bit	active high	active low
Express mode	not activated (serial output)	activated (eight outputs)
Busy pull-down	disabled	enabled

Exit Programming Mode

To exit the programming mode, remove power from the device, or lower \overline{OE} , per Figure 6.

Stand Alone Verify of Data Bits

The verify operation should be performed after programming the entire memory array. Power up the device and enter programming mode (see figure 3). Verify the data bits out in 128 bit words in serial readout mode (see Figure 8). A margin voltage (difference between V_{PP} and V_{CC}) is applied to the device to ensure charge retention on each programmed bit. Set V_{CC} to V_{CCVFY} and V_{PP} to V_{PPVFY} . When reading data in verify mode, the Reset/ \overline{OE} signal should be driven active high while the \overline{CE} signal should be driven active low.

If the data fails to verify, display message “**Failed Margin Verify**”. If the data verifies, display the message “**Device Passed**”.

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Programming Mode Pin Assignments

Name	I/O	Description
Data0	I/O	The rising edge of the clock shifts a data word in or out of the SPROM one bit at a time.
Data 1-6	I/O	Data 1-7 are the output pins to provide parallel data for configuring a Xilinx FPGA in express mode.
CLK	I	Clock input. Used to increment the internal address/word counter for reading and programming.
RESET/ \overline{OE}	I	The rising edge of CLK shifts a data word into the PROM when \overline{CE} and \overline{OE} are high; it shifts a data word out of the PROM when \overline{CE} is Low and \overline{OE} is high. The address/word counter is incremented on the rising edge of CLK while \overline{CE} is held High and \overline{OE} is held Low. Note: Any modified polarity of the RESET/ \overline{OE} pin is ignored in the programming mode.
\overline{CE}	I	The rising edge of CLK shifts a data word into the PROM when \overline{CE} and \overline{OE} are High; it shifts a data word out of the PROM when \overline{CE} is Low and \overline{OE} is High. The address/word counter is incremented on the rising edge of CLK while \overline{CE} is held High and \overline{OE} is held Low.
BUSY	I	Data is held when BUSY is asserted high by the FPGA. (When the BUSY bit is programmed, the BUSY pad is pulled low internally and should also be pulled down externally on the programmer.)
GND		Ground pin
\overline{CEO}	O	The polarity of the RESET/ \overline{OE} , Express mode and BUSY pins can be read by sensing the \overline{CEO} pin. Note: The polarity of the RESET/ \overline{OE} pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
V _{CC}		V _{CC} power supply pin
V _{PP}		Programming Voltage Supply. Programming mode is entered by holding \overline{CE} and \overline{OE} High and V _{PP} at V _{PP1} for two rising clock edges and then lowering V _{PP} to V _{PPNOM} for one more rising clock edge. A word is programmed by strobing the device with V _{PP} for the duration T _{PGM} . V _{PP} must be held at V _{CC} for normal operation.
V _{CC}		V _{CC} power supply input.

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DC Programming Specifications

Symbol	Description	Min	Recommended	Max	Units
V_{CCP}^*	Supply voltage during programming		3.3		V
V_{IL}	Low-level input voltage	0.0	0.0	0.5	V
V_{IH}	High-level input voltage	2.4	V_{CC}	V_{CC}	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	2.5			V
V_{PP1}^{**}	Programming voltage	11.5	11.75	12.0	V
V_{PP2}^{***}	Margin verify voltage during programming		3.7		V
I_{PPP}	Supply current on programming pin			100	mA
V_{CCNOM}/V_{PPNOM}	Nominal Voltage		3.3		V
V_{CCVFY}	Supply voltage during stand alone margin verify		3.3		V
V_{PPVFY}	Margin voltage during stand alone margin verify		3.7		V

* Noise and voltage deviation allowed: $3.3V \pm 50$ mV.

** No overshoot is permitted on signal. V_{PP} must not be allowed to exceed V_{PP1} max.

*** Noise and voltage deviation allowed: $3.7V \pm 250$ mV.

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AC Programming Specifications

Symbol	Description	Min	Rec.	Max	Units	
1	T _{RPP}	10% to 90% rise time of V _{PP}	5		μs	
2	T _{FPP}	90% to 10% fall time V _{PP}	5		μs	
3	T _{PGM}	V _{PP} programming pulse width	90	100	110	μs
4	T _{SVC}	V _{PP} setup to CLK for entering programming	100			ns
5	T _{HVC}	V _{PP} hold from CLK for entering programming	300			ns
6	T _{SDP}	Data setup to CLK for programming	50			ns
7	T _{HDP}	Data hold from CLK for programming	0			ns
8	T _{SCC}	\overline{CE} setup from programming/verifying	100			ns
9	T _{ON}	Reset Pulse Width		5		ms
10	T _{SCV}	\overline{CE} hold from CLK for programming/verifying	100			ns
11	T _{HCV}	\overline{CE} hold from V _{PP} for programming	50			ns
12	T _{SIC}	\overline{OE} setup to CLK for incrementing address	100			ns
13	T _{HIC}	\overline{OE} hold from CLK for incrementing address	0			ns
14	T _{CAC}	CLK to data valid			20	ns
15	T _{OH}	Data hold from CLK	0			ns
16	T _{CFV}	\overline{CE} low to data valid during program-verify			250	ns
17	T _{CF}	\overline{CE} low to data valid during read			20	ns
18	T _{PRST}	Reset polarity programming pulse width		100		us
19	T _{WKU}	Chip wake up time		100		ms

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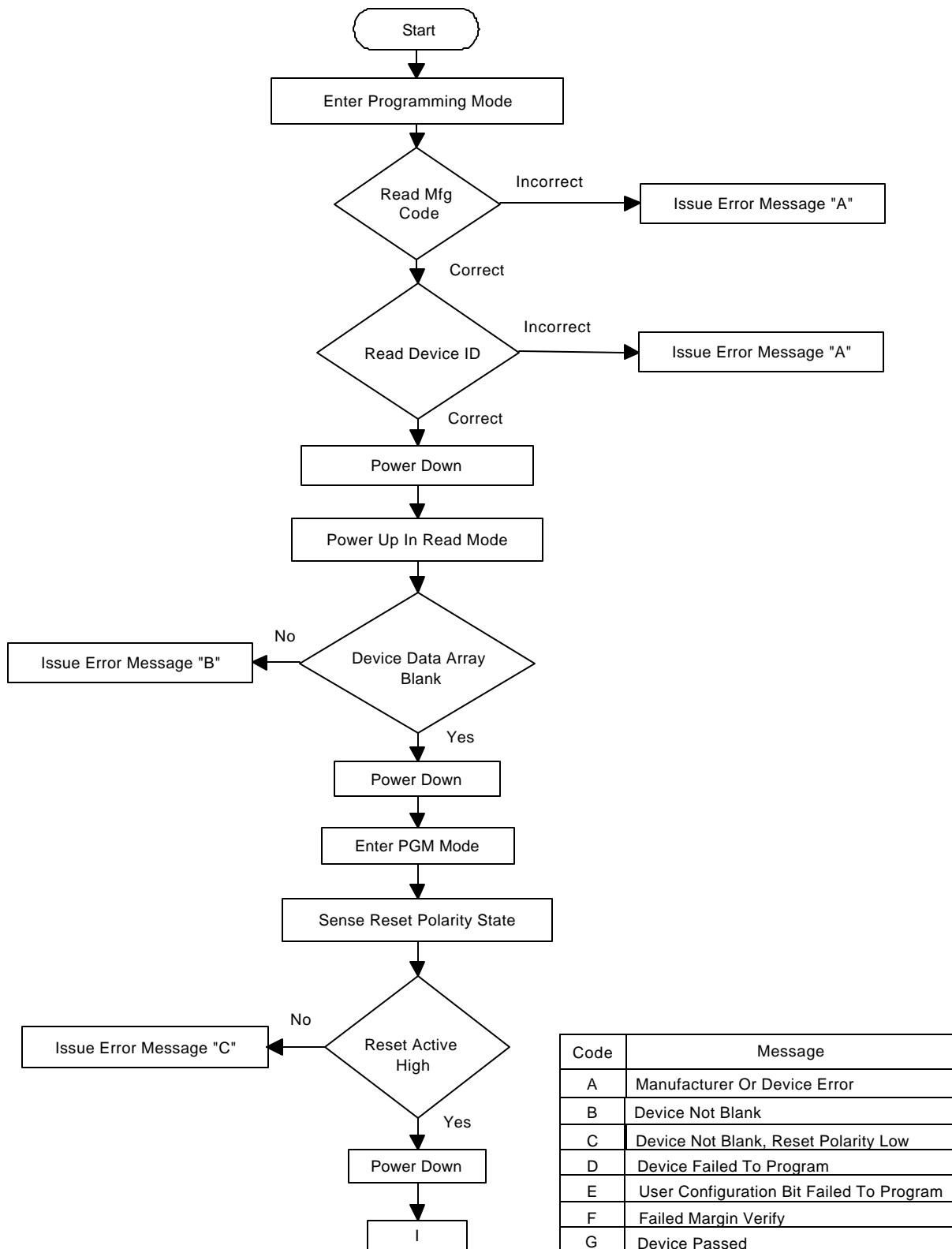


Figure 1. Programming Flow

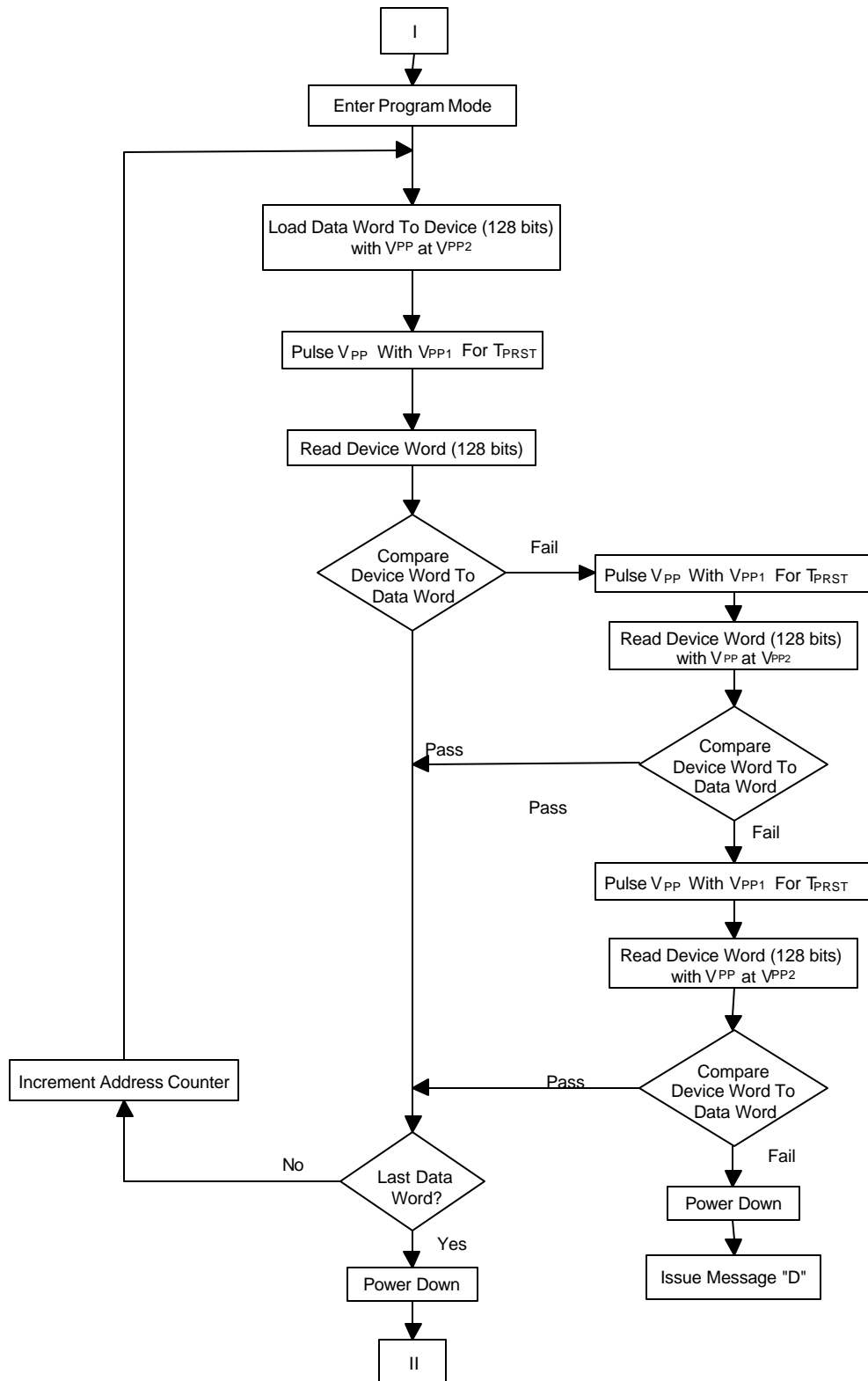


Figure 1. Programming Flow (Continued)

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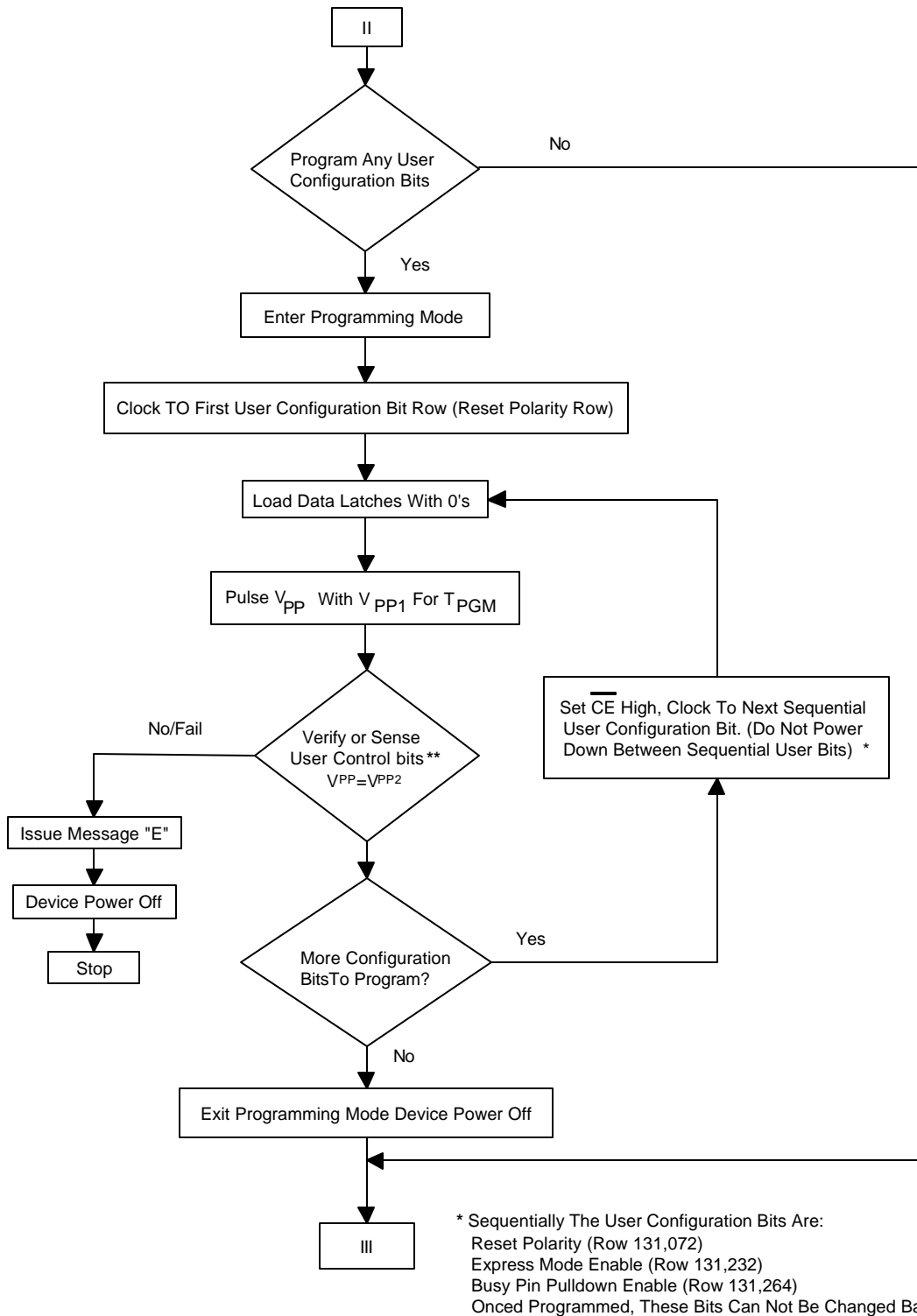


Figure 1. Programming Flow (Continued)

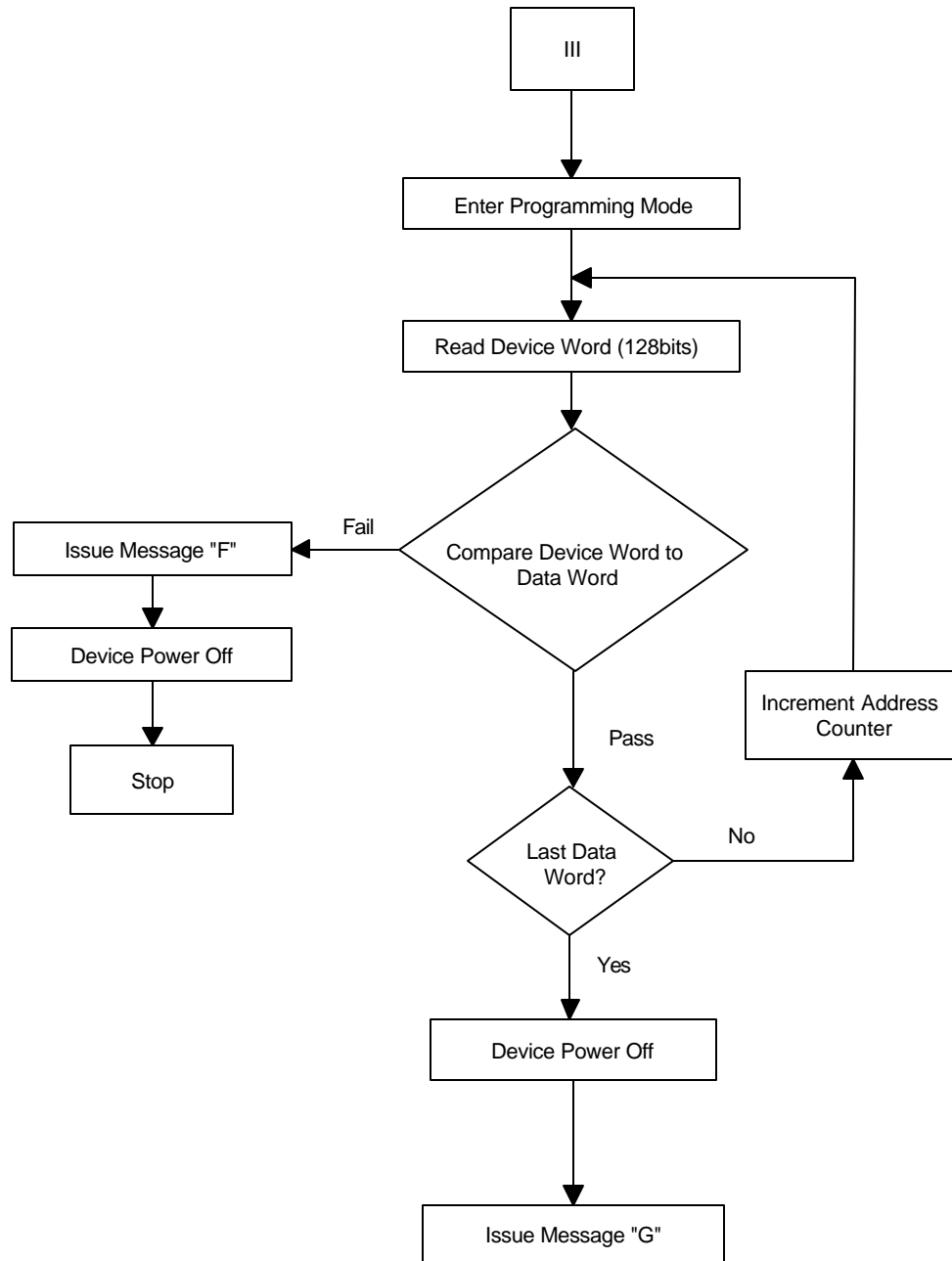


Figure 1. Programming Flow (Continued)

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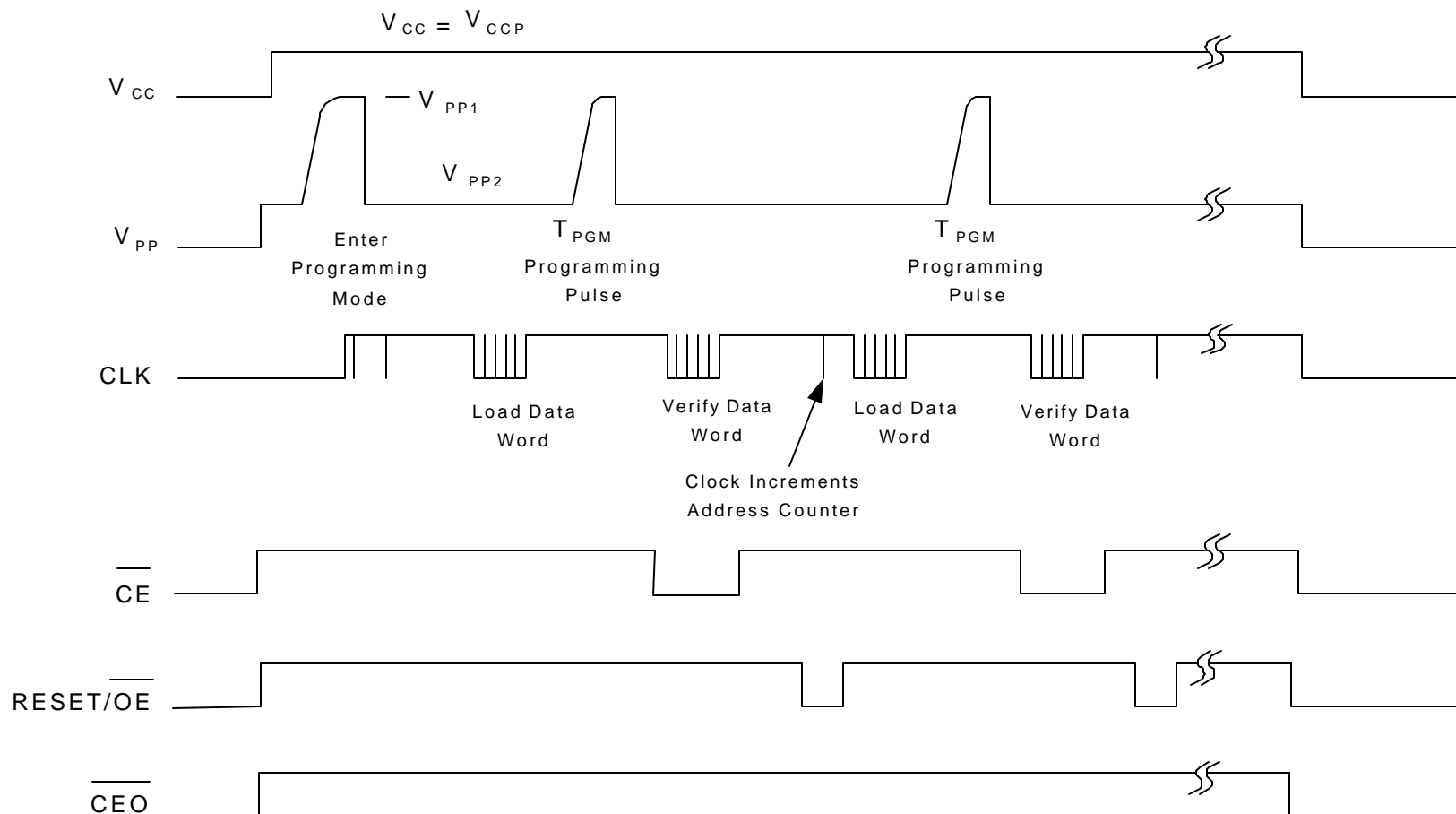
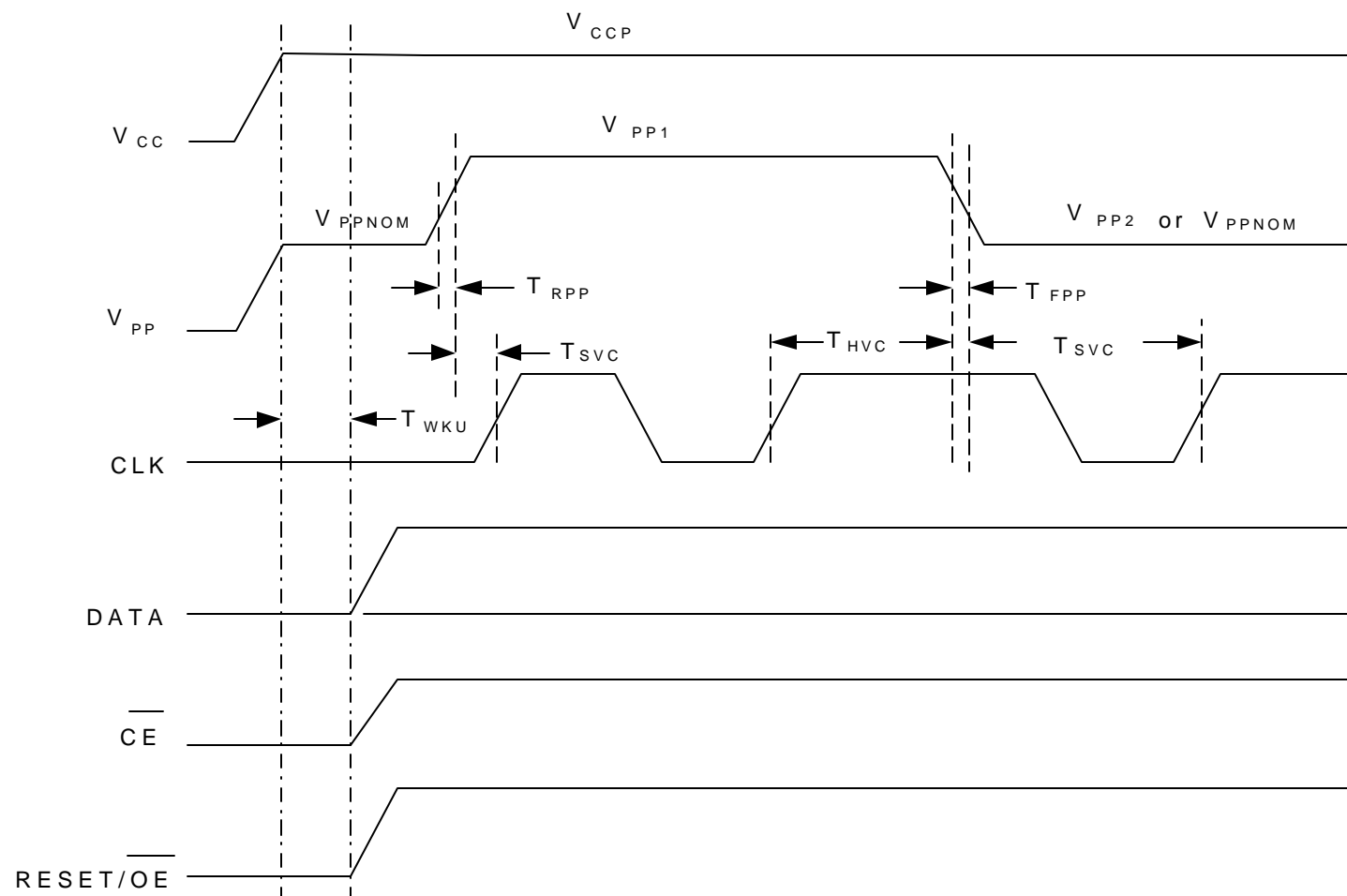


Figure 2. Programming Cycle Overview

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NOTE: If your programming hardware does not allow V_{CC} and V_{PP} to power up simultaneously, then power up V_{CC} followed by V_{PP} .

Figure 3. Enter Programming Mode

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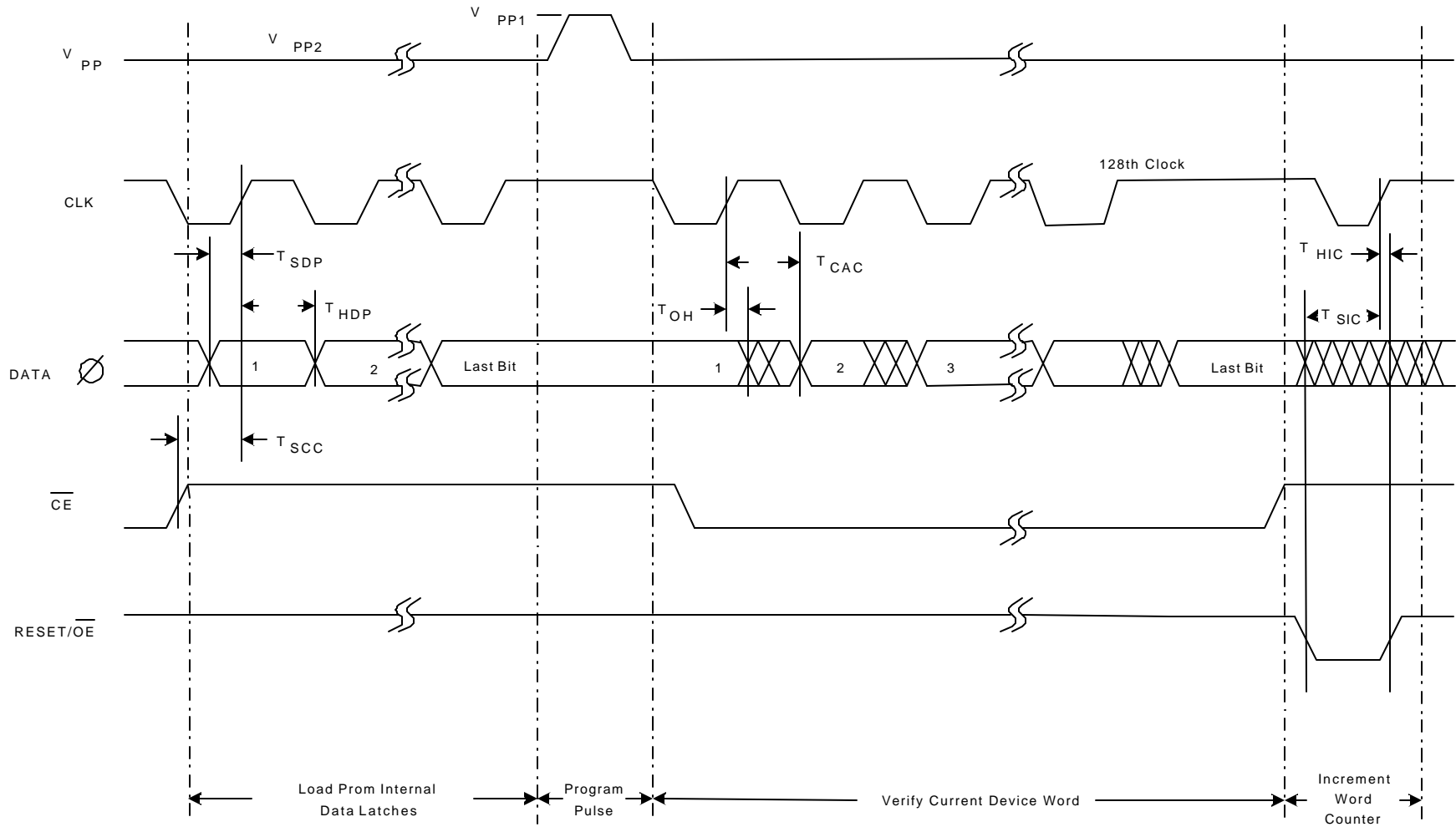
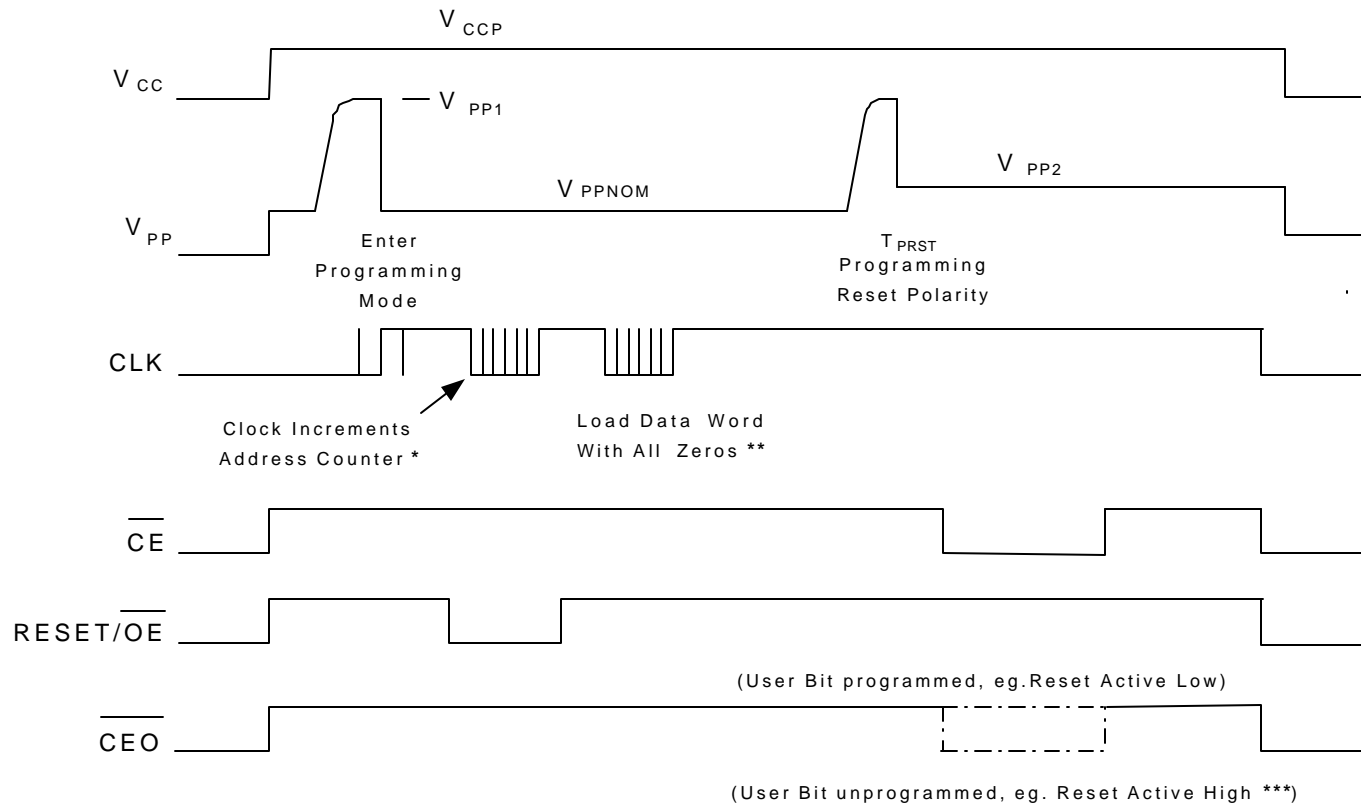


Figure 4. Details Of The Programming Cycle

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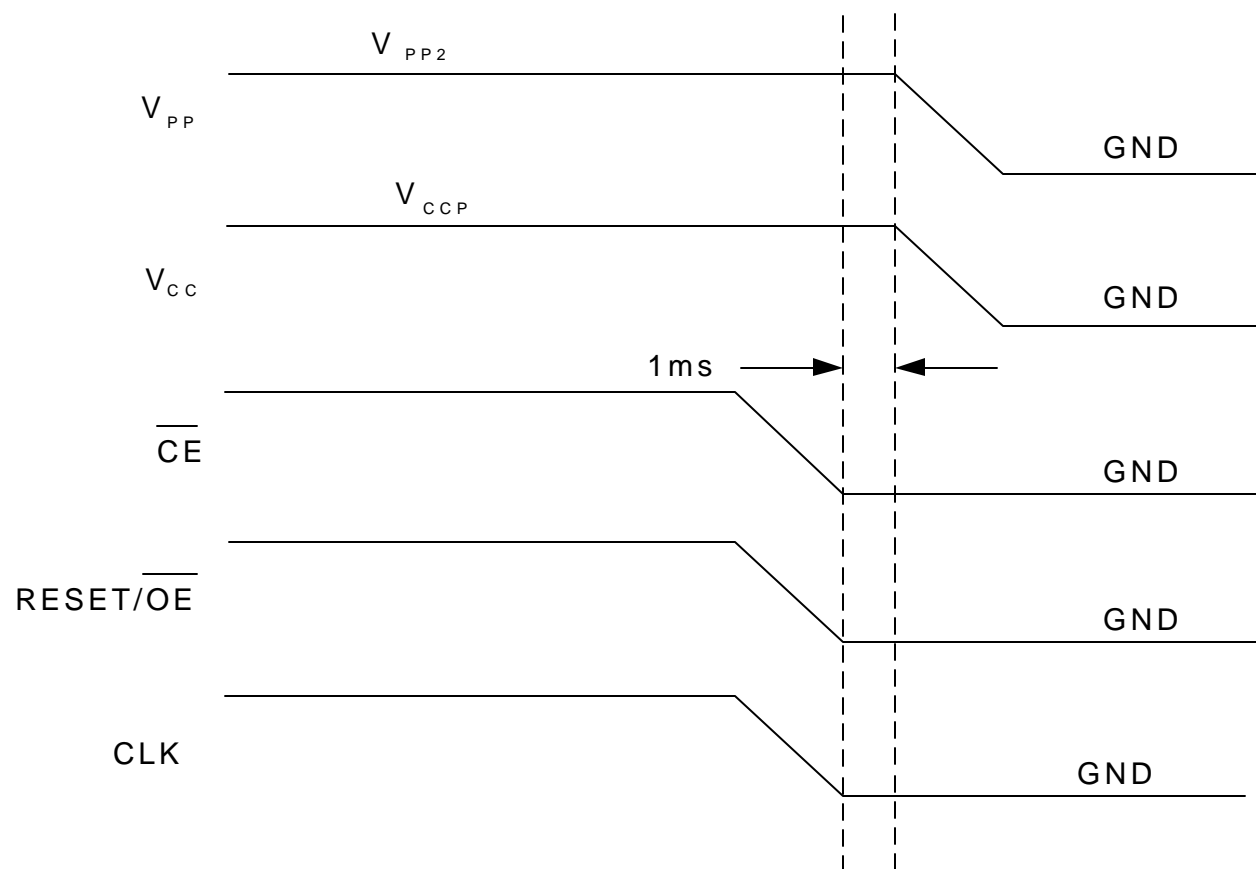


- * Number of Clocks for the User Configuration Bit location.
- ** Repeat the Full Sequence to Program Other User Configuration Bits.
- *** Operation failed to program the Reset Polarity to the Active Low state.

Figure 5. Programming User Configuration Bit

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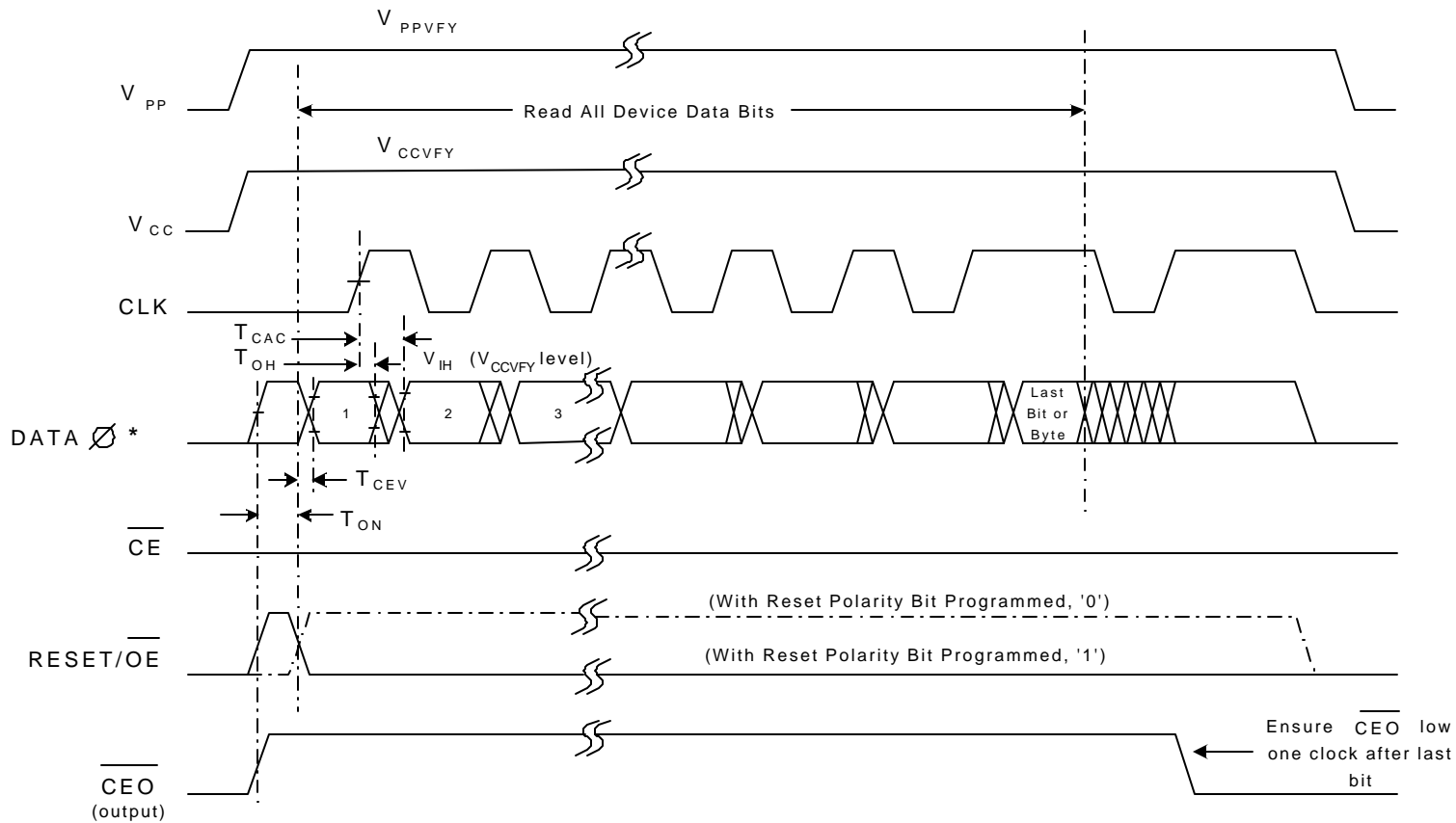


NOTE: If your programming hardware does not allow V_{PP} and V_{CC} to power down simultaneously, then power down V_{PP} followed by V_{CC} .

Figure 6. Exit Programming Mode

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* For device to be blank, Data ∅ should be a logic "1" while reading the device.

Figure 7. Details Of The Blank Check Operation

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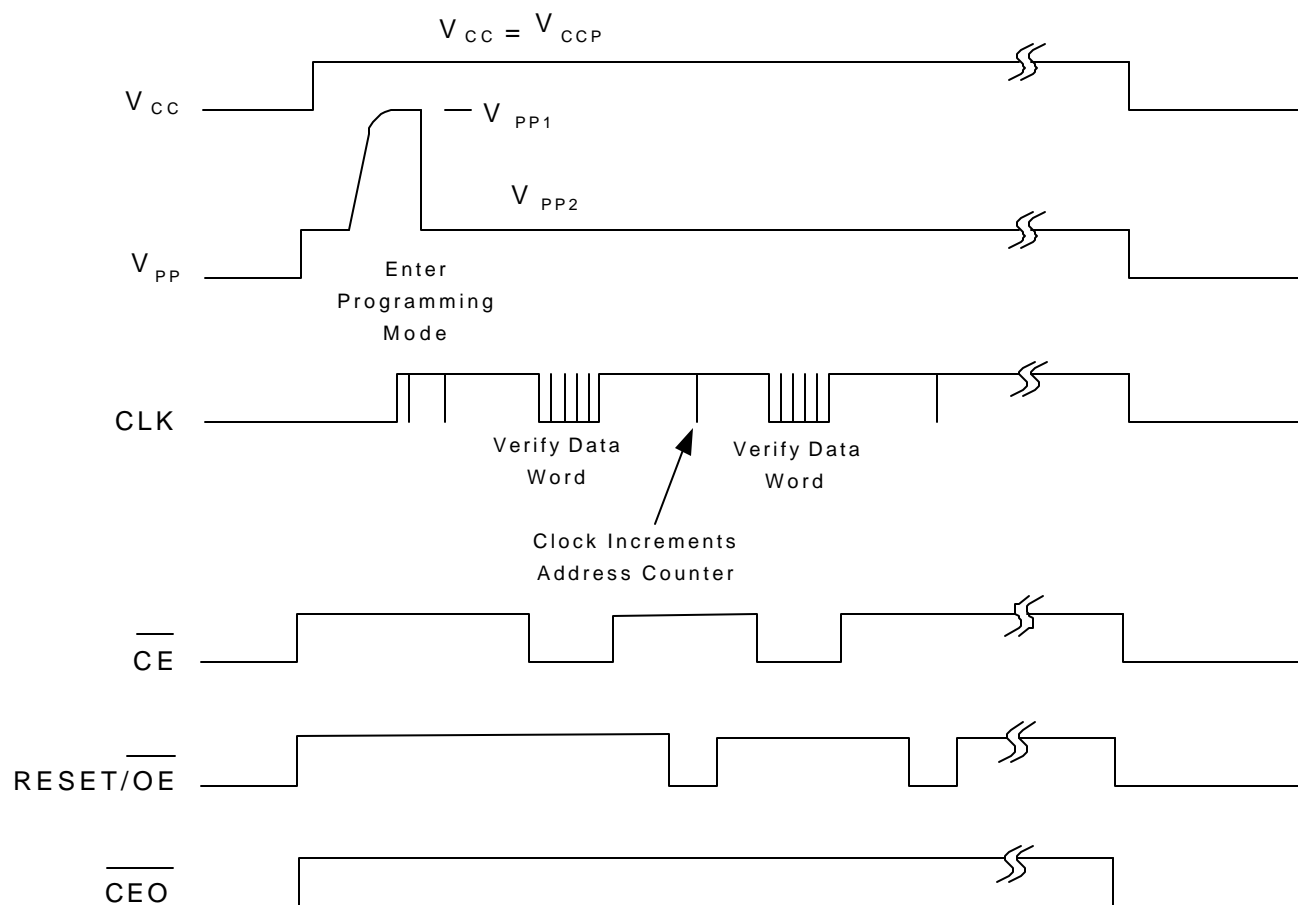


Figure 8. Stand Alone Verify and Verify After Programming