

1. Introduction

This document pertains to the following devices and packages:

9536XL - PLCC44, CSP48, and VQFP64

9572XL - PLCC44, CSP48, VQFP64, and
TQFP100

95144XL - TQFP100, TQFP144, and CSP144

95288XL - TQFP144, PQFP208, and BGA256

The device programming and verification procedures are similar to those used with standard FLASH memories. Initially, and after each erasure, all cells in the device are in the logical "0" (00H) state.

The Xilinx software generates device programming files in JEDEC format. The JEDEC file also contains information specific to each device, which will be compared to the device being programmed. Each product contains a ROM portion with a manufacturer's code to identify Xilinx as the manufacturer and a product code to identify the device. Please refer to the Add.dat file for specific code information.

2. Features

2.1 Erase

The device is electrically erasable. The algorithm has to perform a blank check on the device to ensure all bits are erased before allowing programming.

2.2 Addressing

The device is addressed as a byte-wide memory with several significant exceptions. There are several illegal addresses and some bytes in which not all bits can be programmed. The legal device addresses are contained on the included Add.dat floppy disk.

2.3 Operating Modes

The device has two operating modes: Program and Erase. Program is used for selectively changing FLASH cells within the device. Erase is the procedure used to erase the device. All other operations make use of the programming mode. This includes Stand Alone Verify, Blank Check, Load, and reading of the Signature String, Manufacturer's and Product Codes.

2.4 Signature String

The programmer or host computer must support a mode for reading and displaying the four signature string bytes of alphanumeric characters. Programming of these bytes is automatic because the Xilinx software inserts this string into the design file.

Note: All the sample design files (jedec format) included with this document, have a signature string of 'fast'. Unlike previous CPLD devices, you don't need to complement the data before displaying it. Display the data as you read it.

2.5 Device Security

The device supports a read security feature which protects the design from being copied. A secured device may still be erased and reprogrammed.

3. Special Instructions

3.1 Device/ File Checksum Calculation

Contained in each JEDEC file is a fuse checksum (C-Field), which should be used to represent the file checksum. This checksum is the 16-bit sum (i.e. modulo 65,535) of the 8-bit word containing the fuse states of the entire device. Unused bits in the final 8-bit word must be set to zero. **The same method must be used to calculate the device checksum and the two should match.**

3.2 Compatibility Checks

3.2.1 Adapter Type

The adapter should contain an electronically readable code for identification. The programming algorithm must check the adapter ID for compatibility with the target device. The JEDEC design file also contains information specific to the device pin count and fuse size, both of which must be compared to the adapter in use. The pin count, fuse size, and packages for each device are listed in the Add.dat file, supplied on the floppy disk.

4. Programming Sequence

The device programming sequence, illustrated in Figure 1, begins by verifying that the device design file and programming algorithm match the installed programmer adapter. This check is accomplished by comparing the programmer adapter ID, first to all acceptable adapter IDs in

the programmer algorithm and next to the fuse count and pin count contained in the JEDEC file. If a mismatch occurs, display message **A: “Incompatible Adapter Or File”** for current algorithm and terminate the programming sequence.

4.1 Read Manufacturer’s Code ID

Verify that the manufacturer’s code in the device matches the value listed in the Add.dat file contained on the supplied disk. If the manufacturer’s code ID does not match, display the message **B: “Manufacturer’s Code Error”** and terminate the programming sequence. The appropriate address may be found in the Add.dat file.

4.2 Read Product Code ID

Verify that the product code in the device matches the value listed in the Add.dat file contained on the supplied disk. If the product code ID does not match, display the message **C: “Product Code Error”** and terminate the programming sequence. The appropriate address may be found in the Add.dat file.

Note: Different product codes may require different program and erase voltages.

4.4 Device Blank Check

Verify that all FLASH cells are in the unprogrammed state ('0'). Blank Check is performed with V_{pp} set to V_{ppvf3} . If any one of the FLASH cells is programmed ('1'), display the message **F: “Device Not Blank”** and allow the option to erase the device. The device has to be blank prior to programming. If the device fails, display message **G: “Device Failed To Erase”** and terminate the programming sequence.

4.4 Device Programming and Margin Verify

At this point the actual programming cycle begins. To minimize the duration of the programming cycle, all FLASH cells in one 'Word Line' (WL) are first loaded before a short programming pulse is applied to the device. The amount of address in one WL varies from device to device. Specific address information of all address in all WL's can be found in the Add.dat file of each device. **(Please note the setup and hold time for the programming pulse, T_{ENSV} and T_{ENH} .)** After programming all the WLs of the device, power down the device and perform a margin verify, as illustrated in Figure 5. Power down after the margin verify cycle. The programming/ margin verify cycle is repeated until all FLASH cells pass. If any one of the cells fails margin testing, a number of retries is permitted. Each time, the full address array is reprogrammed. The number of retries (N_{MAX}) can be calculated using the following equation:

$$N_{MAX} = \frac{300 \text{ ms}}{T_{PWPGM}}$$

Where T_{PWPGM} is the actual, measured value of the programming pulse width used. If after N_{MAX} attempts, any cell still fails to pass margin test, display the message **H: “Device Failed To Program”** and terminate the programming sequence.

4.5 Post Program Verify

Once programmed and margin verified successfully, power the device down then perform a stand alone verify or post program verify (See figure 6). This operation is performed with V_{pp} at V_{ppvfy2} . If the device fails, display **message J: “Device Failed To Verify”** and terminate the programming sequence. The programmer operator should not be able to turn OFF this operation.

4.6 Secure Device

Following the programming and stand alone verify sequence, the algorithm should prompt the operator to secure the device, as illustrated in Figure 1. If the user elects not to secure the device, display the message **I: “Device Not Secured”** and terminate the programming sequence. If the user chooses to secure the device, program the security bits (see Figure 4) and display the message **E: “Device Secured”** and terminate the programming sequence. If the device fails to secure, a number of retries are permitted. The number of retries (N_{MAX}) can be calculated using the following equation:

$$N_{MAX} = \frac{300 \text{ ms}}{T_{PWPGM}}$$

Where T_{PWPGM} is the actual, measured value of the programming pulse width used for programming. If after N_{MAX} attempts, any security address still fails to pass margin verify, display the message **K: Device Failed To Secure”** and terminate the programming sequence.

If a device is Read Secured, the signature string, manufacturer’s code and product code can still be read. All other data is scrambled. Table 1 shows which operations may be performed after a device is Read Secured.

Table 1**Read Secure ***

Operation	Valid
Program **	No
Erase	Yes
Verify	No
Load	No
Blank Check	No
Signature String	Yes
Mfg/Product Code	Yes

* See Add.dat file for addresses and data.

** After erasing a secure device, you may program the device again

5. Other Device Operations

5.1 Device Content Loading

Confirm that the device is not secured before attempting to load the content of the device. If **any** security bit has been programmed ('1'), display the message **E: "Device Secured"** and terminate the read sequence. The loading operation is performed with Vpp set to Vppvf2.

5.2 Stand Alone Verify

Confirm that the device is not secured before attempting this operation. If **any** security bit has been programmed ('1'), display the message **E: "Device Secured"** and terminate the stand alone verify operation. The operation is performed with Vpp set to Vppvf2.

5.3 Stand Alone Erase

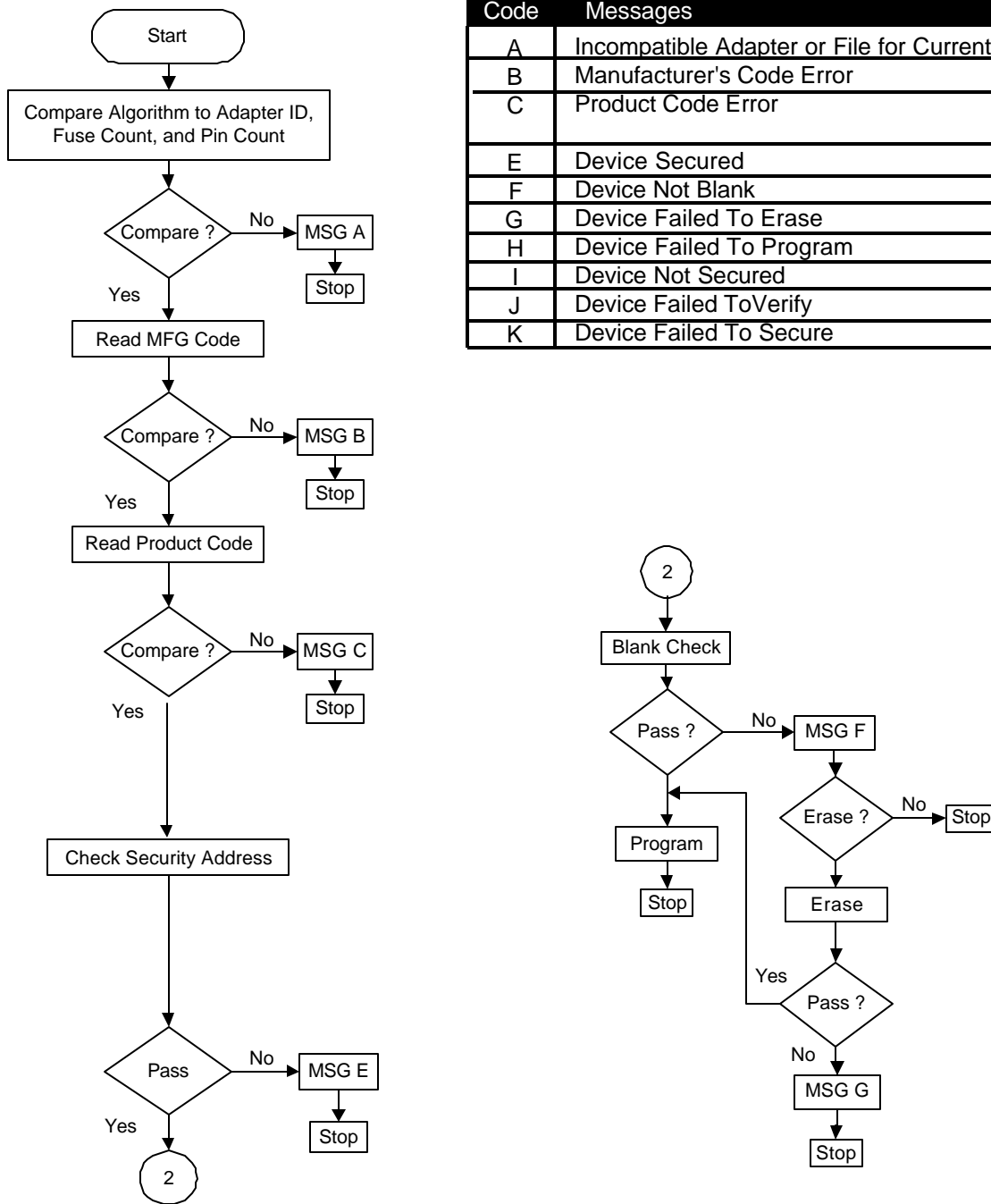
To erase the device, follow the flow in Figure 3 and the timing according to Figure 9. See the Add.dat file for the Function Block (FB) erase address. Erase the device with Vpp set to Vppers and then perform an erase verify with Vpp set to Vppbnk. If any bits failed to erase, a number of retries are permitted. The number of retries ($N_{\text{MAX-ERASE}}$) can be calculated using the following equation:

$$N_{\text{MAX-ERASE}} = \frac{3 \text{ s}}{T_{\text{ERASE}}}$$

Where T_{ERASE} is the actual, measured value of the erase pulse width used for erasing. If after $N_{\text{MAX-ERASE}}$ attempts any addresses still fails to pass erase verify, display the message **G: "Device Failed to Erase"**.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY



Code	Messages
A	Incompatible Adapter or File for Current Algorithm
B	Manufacturer's Code Error
C	Product Code Error
E	Device Secured
F	Device Not Blank
G	Device Failed To Erase
H	Device Failed To Program
I	Device Not Secured
J	Device Failed To Verify
K	Device Failed To Secure

Figure 1. Overall Programming Sequence

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

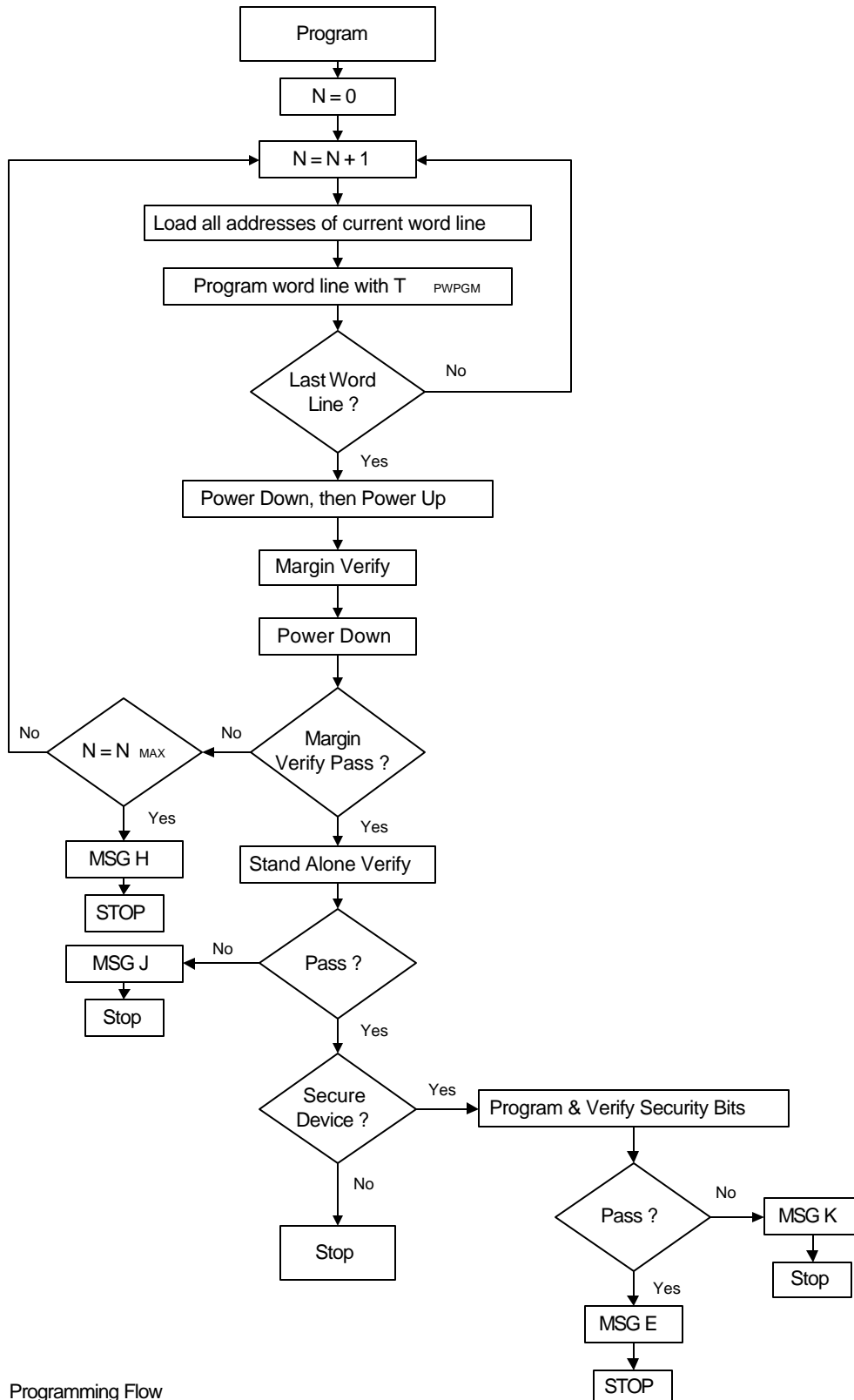


Figure 2. Programming Flow

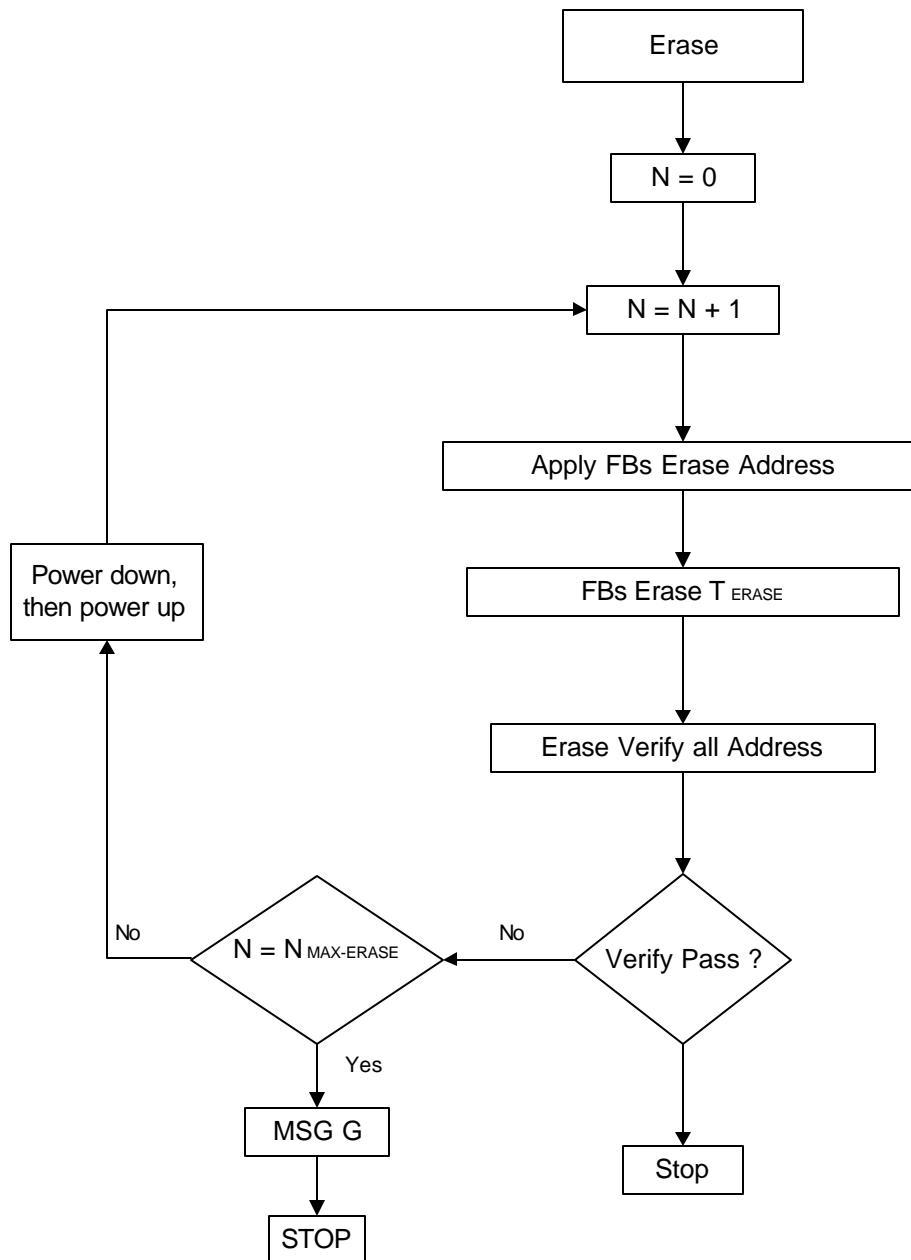


Figure 3. Erase Flow

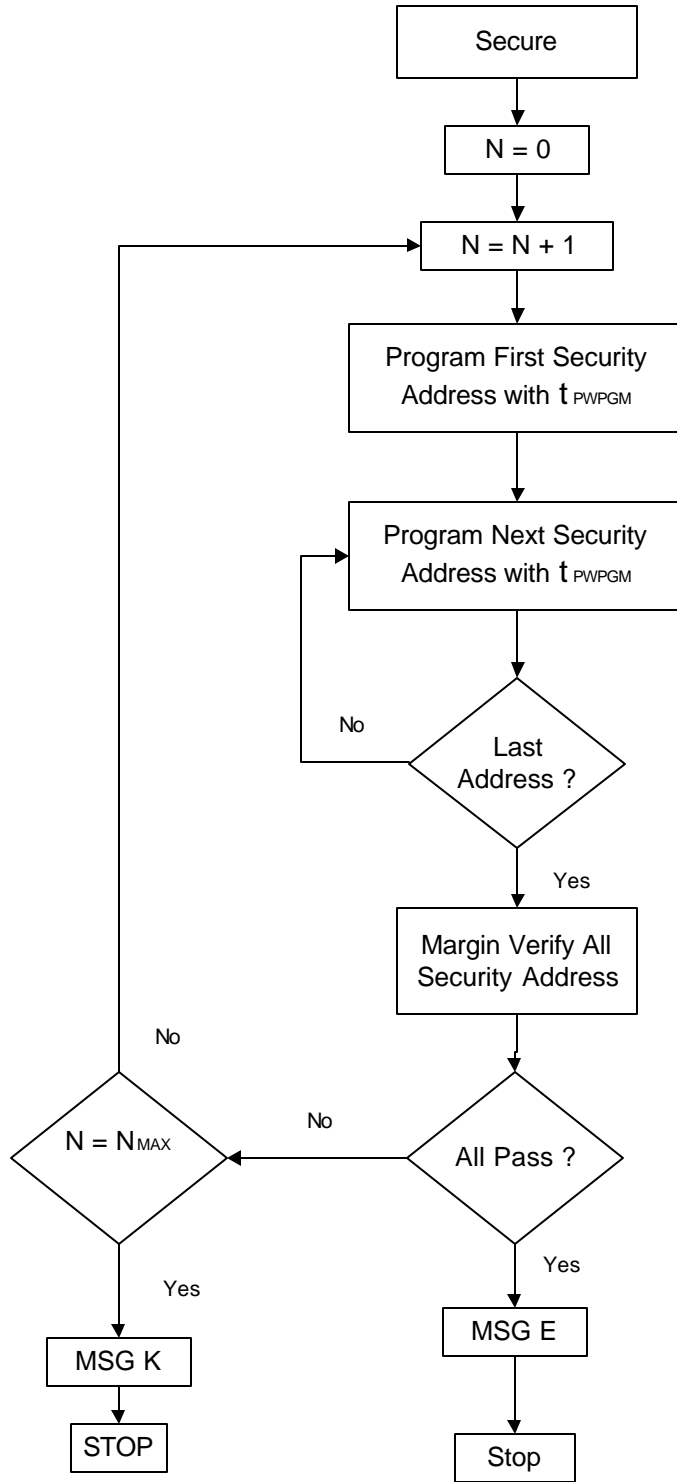


Figure 4. Secure Flow

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

Common DC Programming and Erase Characteristics $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Description	Limits		
		Min	Max	Units
I_{IL}	Input Leakage		10	μA
I_{CC}	V_{CC} Supply Current		400	mA
I_{PP}	V_{PP} Supply Current		100	mA
V_{IL}	Low-Level Input Voltage	0	0.8	V
V_{IH}	High-Level Input Voltage	2.0	5.5	V
V_{OL}	Low-Level Output Voltage		0.4	V
V_{OH}	High-Level Output Voltage	2.4		V
V_{PPTST}	V_{PP} During Test Mode Entry	7.9	8.1	V
V_{CCBNK}	V_{CC} During Blank Verify	3.2	3.4	V
V_{CCNOM}	Nominal V_{CC}	3.2	3.4	V
V_{PPNOM}	Nominal V_{PP}	3.2	3.4	V
V_{PPVF1}	Margin Verify	1.5	1.8	V
V_{PPBNK}	V_{PP} During Blank Verify	5.4	5.6	V
V_{PPVF2}	Stand Alone Verify, Secure Verify, Load	1.7	2.0	V

Note: Although min and max limits are given, Xilinx recommends that the mean be used whenever possible.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

Specific DC Programming and Erase Characteristics $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Description	Product	Code	Min	Max	Units
V_{PPERS}	V_{PP} Erase	XC9536XL	36	7.9	8.1	V
		XC9536XL	30	9.1	9.3	V
		XC9536XL	4B	9.1	9.3	V
		XC9572XL	37	7.9	8.1	V
		XC9572XL	31	9.1	9.3	V
		XC9572XL	4A	9.1	9.3	V
		XC95144XL	35	7.9	8.1	V
		XC95144XL	32	9.1	9.3	V
		XC95144XL	4C	9.1	9.3	V
		XC95288XL	3A	7.9	8.1	V
		XC95288XL	33	9.1	9.3	V
		XC95288XL	4D	9.1	9.3	V
		V_{PPPROG}	V_{PP} Program	XC9536XL	36	7.4
XC9536XL	30			8.5	8.7	V
XC9536XL	4B			8.5	8.7	V
XC9572XL	37			7.4	7.6	V
XC9572XL	31			8.5	8.7	V
XC9572XL	4A			8.5	8.7	V
XC95144XL	35			7.4	7.6	V
XC95144XL	32			8.5	8.7	V
XC95144XL	4C			8.5	8.7	V
XC95288XL	3A			7.4	7.6	V
XC95288XL	33			8.5	8.7	V
XC95288XL	4D			8.5	8.7	V

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

AC Programming Specifications

Symbol	Description	Limits		
		Min	Max	Units
T_{D1}	Delay from V_{CCNOM} to V_{PPNOM}	100		μ s
T_{D2}	Delay from V_{PPNOM} to TSTEN	10		μ s
T_{PWTST}	Test Mode Enable Pulse Width	200		μ s
T_{S1}	V_{PP} Setup Time	100		μ s
T_{S2}	VFYEN or PGMEN Setup Time	1		μ s
T_{S3}	Test Pin Setup Time	1		μ s
T_{S4}	AD_STB Setup Time	0.5		μ s
T_{H2}	PGMEN or VFYEN Hold Time	0.5		μ s
T_{H3}	Test Pin Hold Time	0.5		μ s
T_{H4}	AD_STB Hold Time	0.5		μ s
T_{PWSTB}	AD_STB Pulse Width	1		μ s
T_{AS}	Address Setup Time	0.5		μ s
T_{AH}	Address Hold Time	0.5		μ s
T_{PWPGM}^*	Program Pulse Width	20	100	ms
T_{VDV}	VFYEN to Data Valid	0.5		μ s
T_{ERASE}^{**}	Erase Pulse Width	200	300	ms
T_{VOFF1}	V_{PP} Off Before All Signals	10		μ s
T_{VOFF2}	All Signals Off Before V_{CC}	100		μ s
T_{ENSU}	Setup address & data before PGM/ERS strobe	200		μ s
T_{ENH}	Setup address & data after PGM/ERS strobe	200		μ s

* Recommended T_{PWPGM} is 50 ms

** Recommended T_{ERASE} is 200 ms

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

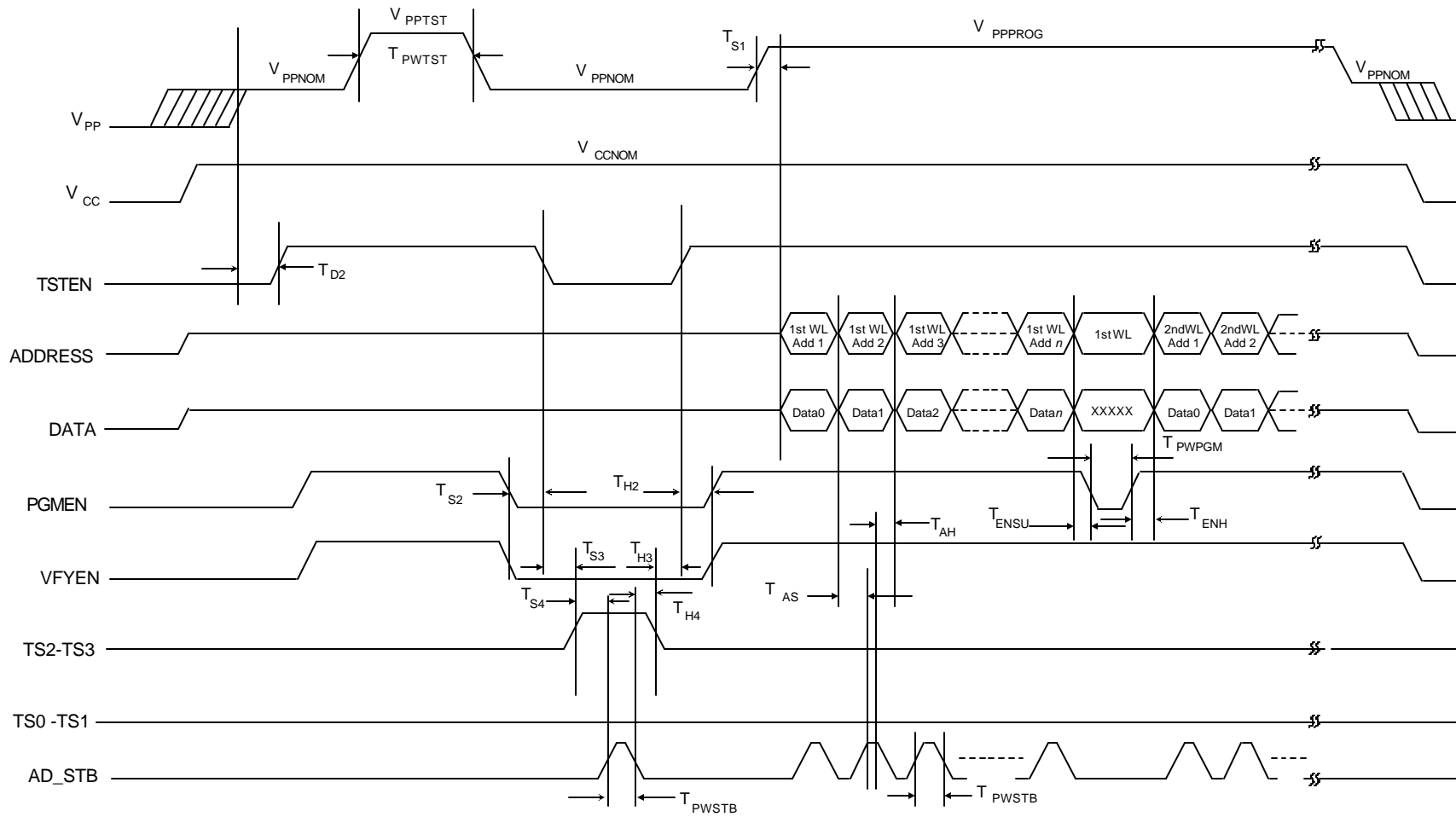
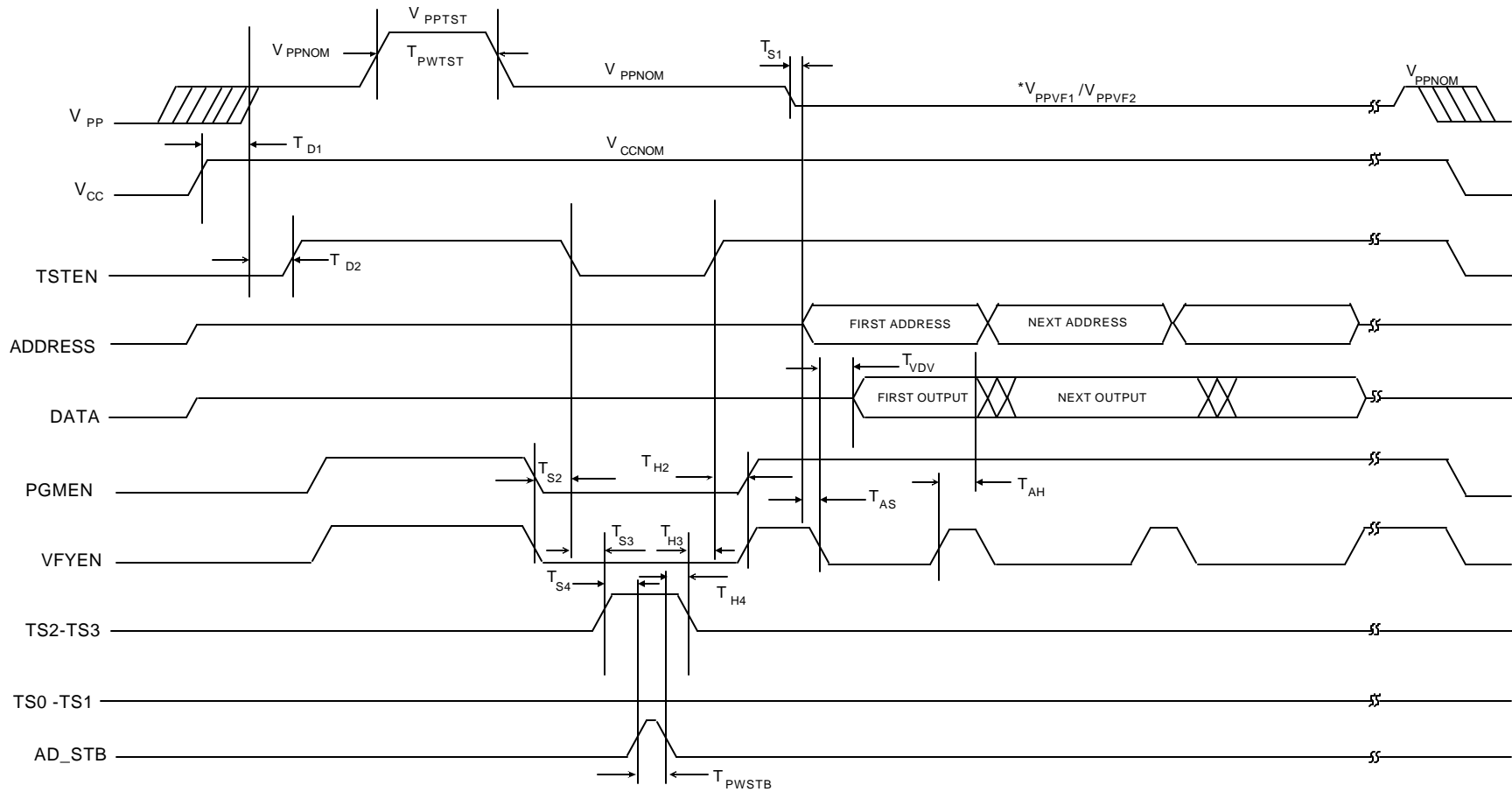


Figure 5. Program

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY



*V_{PPVF1} only used for Margin Verify

Figure 6. Margin Verify, Stand Alone Verify, Secure Verify, and Load

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

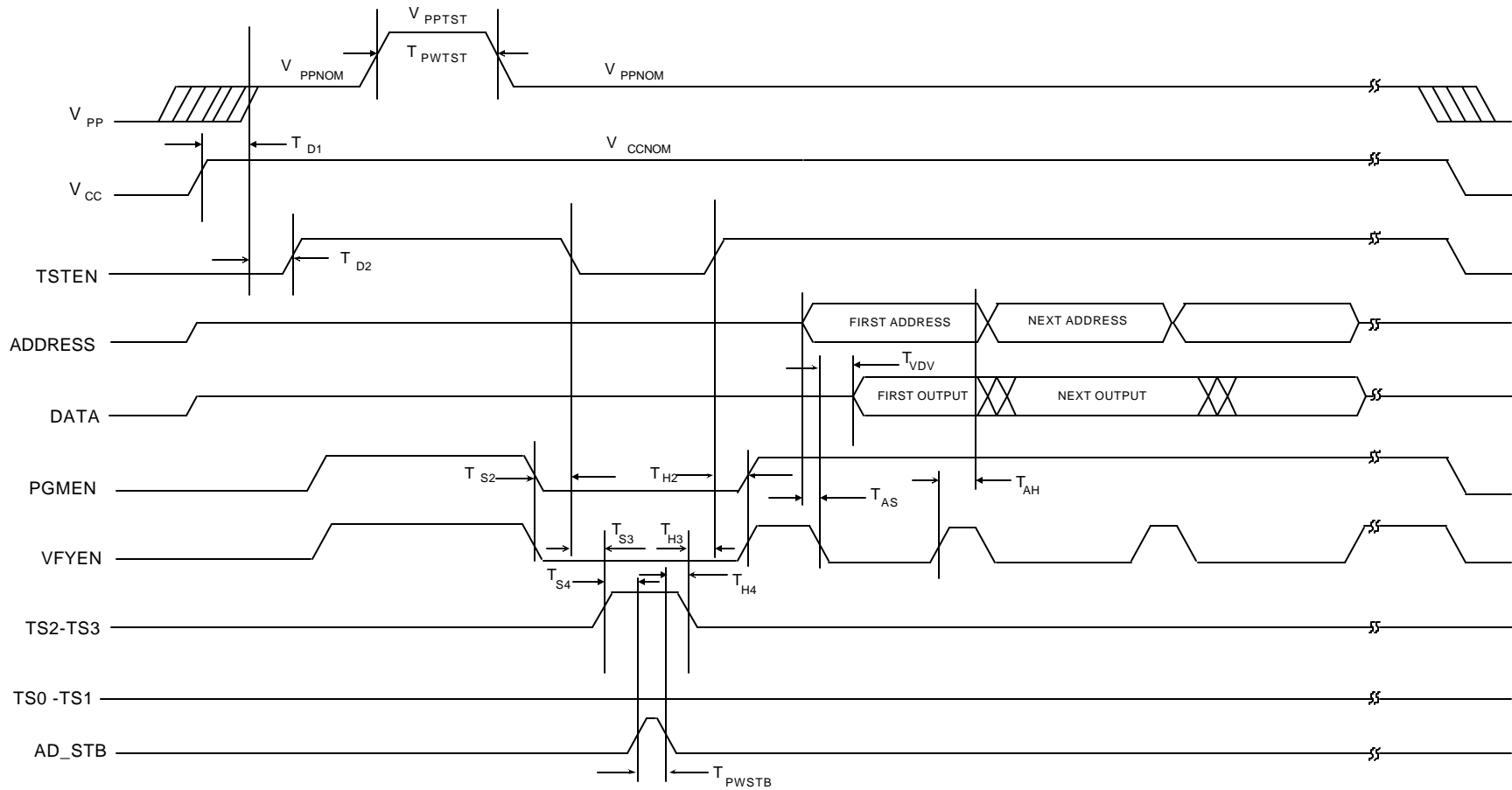


Figure 7. Manufacturer's Code, Product Code, and Signature String

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

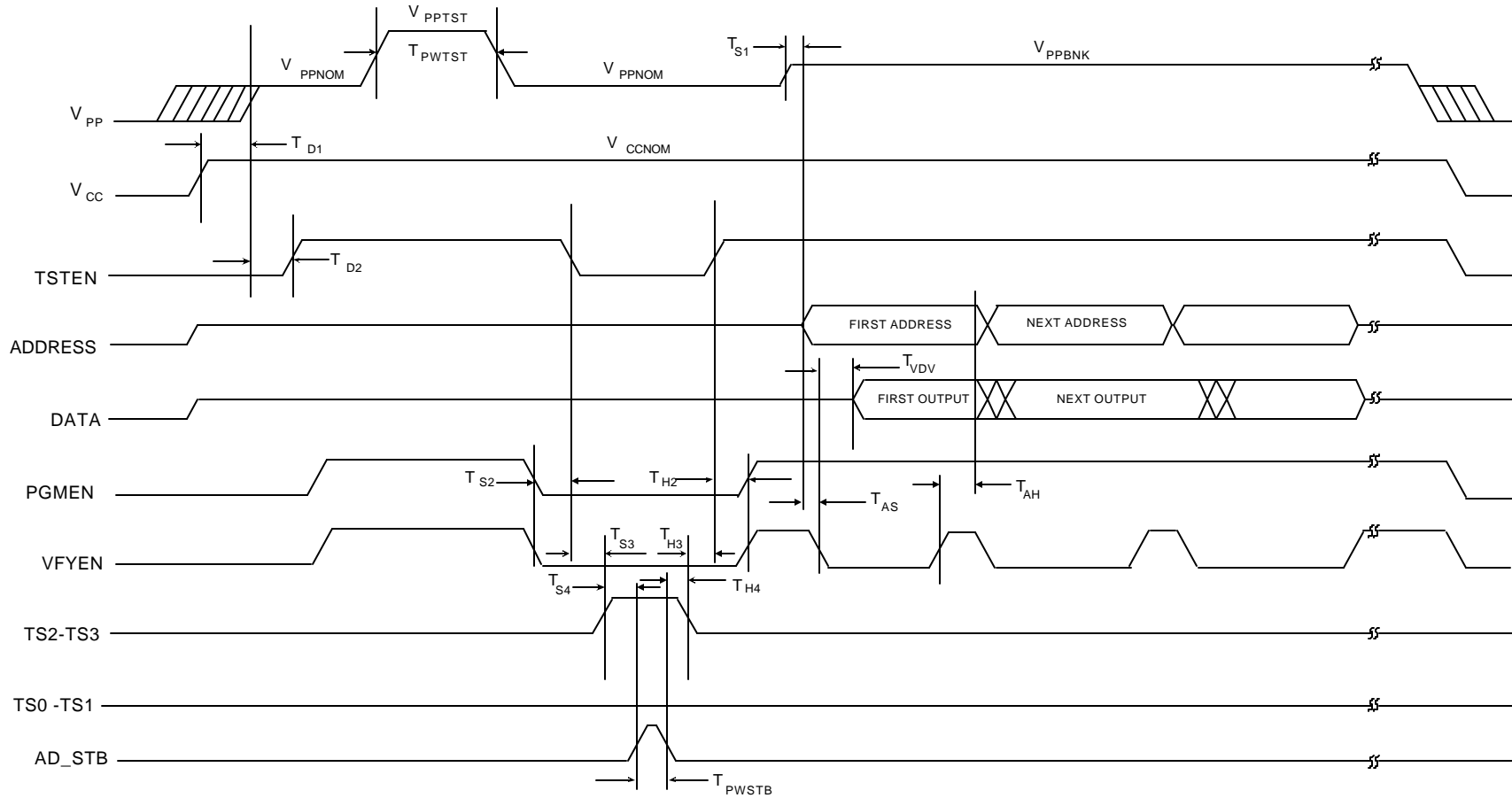


Figure 8. Blank Check

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

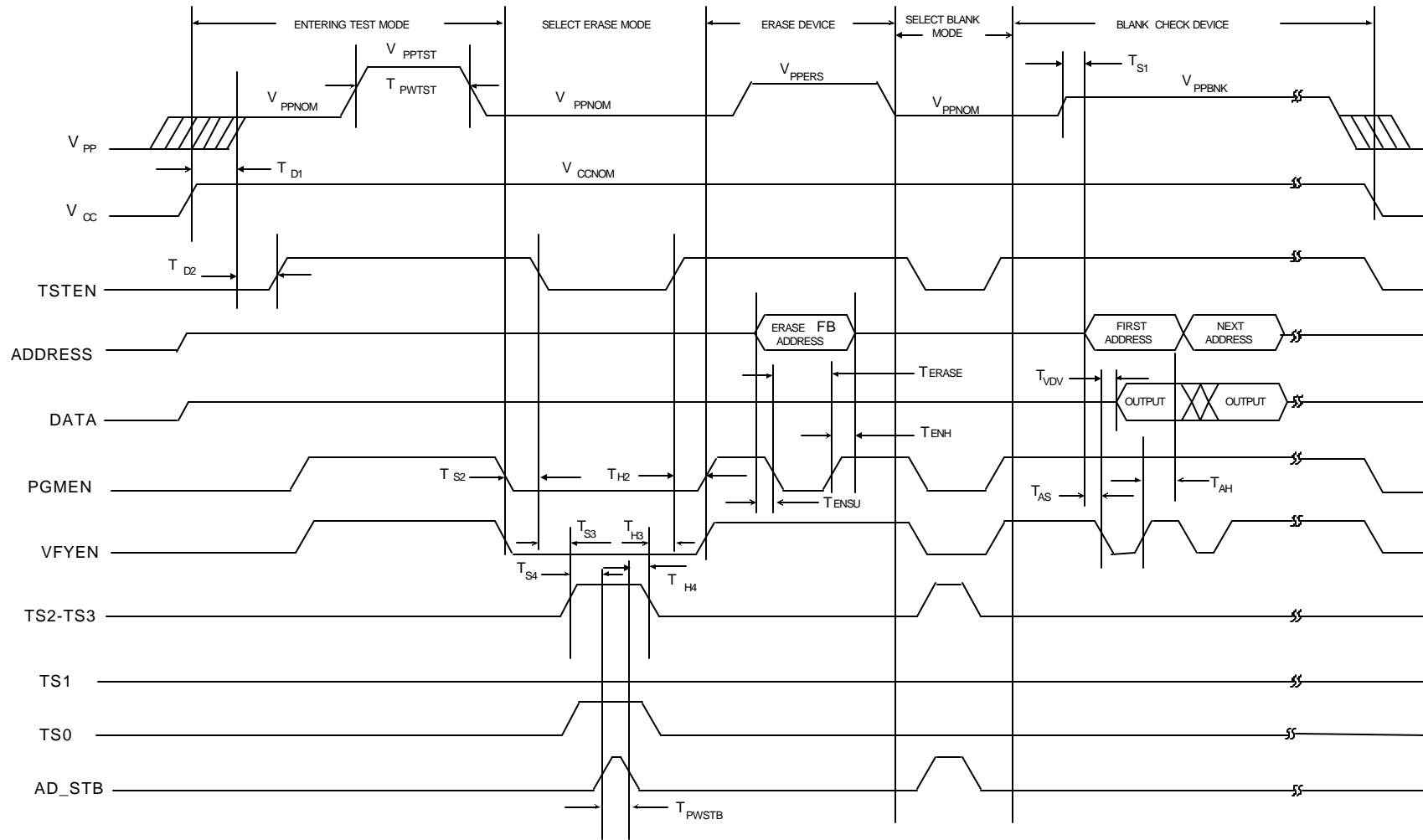


Figure9. Erase

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC9536XL Programming Signal Definitions

Pin Type	PC44	VQ44	48 CSP	VQ64
NC	40	34	F6	2
V _{PP}	41	35	F7	3
VFYEN	42	36	E6	5
*	43	37	E7	6
ADSTB	44	38	E5	7
TSTEN	1	39	D7	8
Ts2	2	40	D6	9
Ts3	3	41	C7	10
Ts0	4	42	C6	11
NC	5	43	B7	15
NC	6	44	B6	16
Ts1	7	1	A7	17
A8	8	2	A6	19
A9	9	3	C5	20
GND	10	4	A5	21
A10	11	5	B5	22
A11	12	6	A4	24
A12	13	7	B4	25
NC	14	8	A3	27
D3/TDI	15	9	B3	28
TMS	16	10	A2	29
TCK	17	11	A1	30
D0	18	12	B2	33

Pin Type	PC44	VQ44	48 CSP	VQ64
D1	19	13	B1	35
D2	20	14	C2	36
V _{CC}	21	15	C1	37
D4	22	16	C3	38
NC			D3	39
GND	23	17	D1	41
D5	24	18	D2	42
D6	25	19	E1	43
D7	26	20	E2	44
NC	27	21	F1	45
PGMEN	28	22	G1	48
NC			E4	49
A0	29	23	F2	50
A1/TDO	30	24	G2	53
GND	31	25	F3	54
V _{CC}	32	26	G3	55
A2	33	27	E3	56
A3	34	28	G4	57
A4	35	29	F4	60
A5	36	30	G5	61
A6	37	31	F5	62
A7	38	32	G6	63
NC	39	33	G7	64

NOTE: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC9572XL Programming Signal Definitions

Pin Type	PC44	VQ44	48 CSP	VQ64
NC				1
NC	40	34	F6	2
V _{PP}	41	35	F7	3
NC				4
A0	42	36	E6	5
*	43	37	E7	6
A1	44	38	E5	7
TSTEN	1	39	D7	8
A2	2	40	D6	9
PGMEN	3	41	C7	10
VFYEN	4	42	C6	11
NC			D4	12
NC				13
GND				14
NC	5	43	B7	15
NC	6	44	B6	16
A3	7	1	A7	17
NC				18
D0	8	2	A6	19
D1	9	3	C5	20
GND	10	4	A5	21
D2	11	5	B5	22
NC				23
D3	12	6	A4	24
D4	13	7	B4	25
V _{CC}				26
A4	14	8	A3	27
A5/TDI	15	9	B3	28
TMS	16	10	A2	29
A6/TCK	17	11	A1	30
NC			C4	31
NC				32

Pin Type	PC44	VQ44	48 CSP	VQ64
D5	18	12	B2	33
NC				34
D6	19	13	B1	35
D7	20	14	C2	36
V _{CC}	21	15	C1	37
NC	22	16	C3	38
NC			D3	39
NC				40
GND	23	17	D1	41
A7	24	18	D2	42
A8	25	19	E1	43
A9	26	20	E2	44
A10	27	21	F1	45
NC				46
NC				47
A11	28	22	G1	48
NC			E4	49
A12	29	23	F2	50
NC				51
NC				52
A13/TDO	30	24	G2	53
GND	31	25	F3	54
V _{CC}	32	26	G3	55
ADSTB	33	27	E3	56
NC	34	28	G4	57
NC				58
NC				59
TS0	35	29	F4	60
TS1	36	30	G5	61
TS2	37	31	F5	62
TS3	38	32	G6	63
NC	39	33	G7	64

NOTE: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC9572XL Programming Signal Definitions (Cont.)

Pin Type	TQ100
NC	1
NC	3
NC	4
V _{PP}	5
NC	6
A0	8
NC	9
A1	10
*	11
NC	12
TSTEN	13
NC	14
PGMEN	15
A2	16
VFYEN	17
A3	18
NC	20
GND	21
NC	22
NC	23
NC	25
V _{CC}	26
NC	27
A4	28
D0	29
D1	30
GND	31
D2	32
A5	33
D3	35
A6	36

PIN TYPE	TQ100
D4	37
V _{CC}	38
NC	39
NC	40
NC	41
NC	42
GND	44
TDI	45
TMS	47
TCK	48
A7	49
A8	50
V _{CC}	51
D5	52
NC	53
NC	54
D6	55
D7	56
V _{CC}	57
NC	58
NC	59
A9	60
A10	61
GND	62
A11	63
NC	64
NC	65
NC	66
NC	67
NC	68

PIN TYPE	TQ100
GND	69
NC	70
NC	71
NC	72
NC	74
GND	75
NC	76
NC	77
NC	78
NC	79
NC	81
NC	82
TDO	83
GND	84
NC	85
NC	86
NC	87
V _{CC}	88
ADSTB	89
A12	90
A13	91
NC	92
NC	93
TS0	94
TS1	95
TS2	96
TS3	97
V _{CC}	98
NC	99
GND	100

NOTE: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC95144XL Programming Signal Definitions

Pin Type	TQ100	CS144	TQ144
V _{CC}		A1	1
NC	1	B1	2
NC	2	C2	3
NC		C1	4
NC	3	D4	5
NC	4	D3	6
NC		D2	7
V _{PP}	5	D1	8
NC	6	E4	9
NC	7	E3	10
VFYEN	8	E2	11
NC		E1	12
ADSTB**	9	F4	13
NC		F3	14
ADSTB**	10	F2	15
PGMEN	11	F1	16
NC	12	G2	17
GND		G1	18
TSTEN	13	G3	19
NC	14	G4	20
TS0	15	H1	21
TS1	16	H2	22
NC		H3	23
TS2	17	H4	24
NC		J1	25
TS3	18	J2	26
NC	19	J3	27
NC	20	J4	28
GND	21	K1	29
NC	22	K2	30
NC		K3	31
NC	23	L1	32
NC	24	L2	33
NC	25	L3	34
NC		M1	35
GND		M2	36

Pin Type	TQ100	CS144	TQ144
V _{CC}	26	N1	37
NC	27	N2	38
NC		M3	39
A8	28	N3	40
NC		K4	41
V _{CC}		L4	42
A9	29	M4	43
NC		N4	44
A10	30	K5	45
NC		L5	46
GND	31	M5	47
NC		N5	48
A11	32	K6	49
A12	33	L6	50
NC	34	M6	51
A13	35	N6	52
A14	36	M7	53
NC	37	N7	54
V _{CC}	38	L7	55
NC	39	K7	56
NC	40	N8	57
NC	41	M8	58
NC		L8	59
NC	42	K8	60
NC	43	N9	61
GND	44	M9	62
TDI	45	L9	63
NC	46	K9	64
TMS	47	N10	65
NC		M10	66
TCK	48	L10	67
NC		N11	68
D0	49	M11	69
NC		L11	70
D1	50	N12	71
GND		M12	72

Note: Pins marked with * must be connected to soft GND.

****** The signal ADSTB should be applied to 2 pins on the device simultaneously.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC95144XL Programming Signal Definitions (Cont.)

Pin Type	TQ100	CS144	TQ144
V _{CC}	51	N13	73
D2	52	M13	74
NC		L12	75
NC	53	L13	76
NC		K10	77
NC	54	K11	78
NC		K12	79
D3	55	K13	80
NC		J10	81
D4	56	J11	82
NC		J12	83
V _{CC}	57	J13	84
D5	58	H10	85
NC	59	H11	86
D6	60	H12	87
D7	61	H13	88
GND		G12	89
GND	62	G13	90
NC	63	G11	91
NC	64	G10	92
NC	65	F13	93
NC	66	F12	94
NC		F11	95
NC	67	F10	96
NC		E13	97
NC	68	E12	98
GND	69	E11	99
NC	70	E10	100
NC		D13	101
NC	71	D12	102
NC		D11	103
NC	72	C13	104
NC	73	C12	105
NC	74	C11	106
NC		B13	107
GND	75	B12	108

Pin Type	TQ100	CS144	TQ144
V _{CC}		A13	109
NC	76	A12	110
NC		B11	111
NC	77	A11	112
NC	78	D10	113
GND		C10	114
NC		B10	115
NC	79	A10	116
NC		D9	117
NC		C9	118
NC	80	B9	119
NC	81	A9	120
NC	82	D8	121
TDO	83	C8	122
GND	84	B8	123
NC	85	A8	124
NC	86	B7	125
NC	87	A7	126
V _{CC}	88	C7	127
A0	89	D7	128
A1	90	A6	129
A2	91	B6	130
NC	92	C6	131
A3	93	D6	132
NC		A5	133
A4	94	B5	134
NC		C5	135
A5	95	D5	136
NC		A4	137
A6	96	B4	138
NC		C4	139
A7	97	A3	140
V _{CC}	98	B3	141
NC		C3	142
NC	99	A2	143
GND	100	B2	144

Note: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC95288XL Programming Signal Definitions

Pin Type	TQ144	PQ208	BG256
V _{CC}	1	1	P
GND		2	G
GND			B1
NC	2	3	C2
NC		4	D2
NC	3	5	D3
NC	4	6	E4
NC	5	7	C1
NC			D1
NC		8	E3
NC			E2
NC	6	9	E1
NC	7	10	F3
V _{PP}	8	11	G4
NC		12	F2
V _{CC}			F1
GND		13	G
NC		14	G3
V _{CC}			P
NC	9	15	G2
NC	10	16	G1
VFYEN	11	17	H4
NC	12	18	H3
*	13	19	H2
NC			H1
NC	14	20	J4
NC			J3
ADSTB	15	21	J2
PGMEN	16	22	J1
NC	17	23	K2
GND	18	24	K3
TSTEN	19	25	K1
V _{CC}		26	P
GND		27	G
NC		28	L1
NC		29	L2

Pin Type	TQ144	PQ208	BG256
NC	20	30	L3
TS0	21	31	L4
TS1	22	32	M1
NC			M2
NC	23	33	M3
NC			M4
TS2	24	34	N1
NC	25	35	N2
TS3	26	36	N3
NC	27	37	N4
NC	28	38	P1
GND			G
V _{CC}			P2
V _{CC}			P
NC		39	R1
NC		40	P3
NC		41	R2
GND	29	42	T1
NC		43	P4
NC			R3
NC	30	44	T2
NC			U1
NC	31	45	T3
NC	32	46	U2
NC	33	47	V1
NC		48	T4
NC	34	49	U3
NC		50	V2
NC	35	51	V3
GND	36	52	G
V _{CC}	37	53	P
NC		54	Y2
NC	38	55	W4
NC			V4
NC	39	56	U5
NC			Y3

Note: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC95288XL Programming Signal Definitions (Cont.)

Pin Type	TQ144	PQ208	BG256
A8	40	57	Y4
NC	41	58	V5
V _{CC}	42	59	W5
GND			Y5
A9	43	60	V6
NC	44	61	U7
NC		62	W6
A10	45	63	Y6
NC	46	64	V7
V _{CC}		65	P
NC		66	U8
NC		67	W7
NC			Y7
GND	47	68	G
NC		69	V8
NC			W8
NC	48	70	Y8
NC		71	U9
A11	49	72	V9
NC		73	W9
V _{CC}			Y9
GND			W10
V _{CC}			V10
GND			Y10
A12	50	74	Y11
NC	51	75	W11
A13	52	76	V11
A14	53	77	U11
A15	54	78	Y12
V _{CC}	55	79	P
NC			W12
NC		80	V12
GND		81	G
NC	56	82	U12
NC	57	83	Y13
NC	58	84	W13

Pin Type	TQ144	PQ208	BG256
NC		85	V13
V _{CC}			U13
GND			Y14
NC	59	86	W14
NC		87	Y15
NC	60	88	V14
NC	61	89	W15
NC		90	Y16
NC		91	U14
GND			G
V _{CC}		92	P
GND	62	93	V15
TD1	63	94	W16
NC			Y17
NC	64	95	V16
TMS	65	96	W17
NC	66	97	Y18
TCK	67	98	U16
NC	68	99	V17
V _{CC}			W18
D0	69	100	Y19
NC		101	V18
NC	70	102	W19
D1	71	103	Y20
GND	72	104	G
V _{CC}	73	105	P
NC		106	V19
NC		107	U19
GND		108	U18
NC		109	T17
D2	74	110	V20
NC			U20
NC		111	T18
NC	75	112	T19
V _{CC}			T20
NC		113	R18

Note: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC95288XL Programming Signal Definitions (Cont.)

Pin Type	TQ144	PQ208	BG256
NC	76	114	P17
GND			R19
NC	77	115	R20
NC	78	116	P18
V _{CC}			P
GND			G
NC	79	117	P19
D3	80	118	P20
NC		119	N17
NC		120	N18
NC	81	121	N19
NC			N20
D4	82	122	M17
NC	83	123	M18
V _{CC}	84	124	M19
D5	85	125	M20
NC	86	126	L19
D6	87	127	L18
D7	88	128	L20
GND	89	129	G
GND	90	130	K20
NC	91	131	K19
V _{CC}		132	P
NC	92	133	K18
NC	93	134	K17
NC	94	135	J20
NC	95	136	J19
NC			J18
NC	96	137	J17
NC	97	138	H20
NC	98	139	H19
NC		140	H18
GND	99	141	G
NC		142	H17
NC		143	G20
NC		144	G19

Pin Type	TQ144	PQ208	BG256
V _{CC}			F20
V _{CC}			P
GND			G18
NC	100	145	F19
NC	101	146	E20
NC	102	147	G17
NC	103	148	F18
NC			E19
NC	104	149	D20
NC	105	150	E18
NC		151	D19
NC	106	152	C20
V _{CC}		153	E17
NC	107	154	D18
NC		155	C18
GND	108	156	G
V _{CC}	109	157	P
NC	110	158	B18
V _{CC}			B17
NC	111	159	C17
NC	112	160	D16
NC		161	A18
NC	113	162	A17
NC			C16
GND	114	163	B16
NC	115	164	A16
NC		165	C15
NC	116	166	D14
GND			G
NC		167	B15
NC		168	A15
NC		169	C14
GND			D13
V _{CC}			B14
NC	117	170	A14
NC	118	171	C13

Note: Pins marked with * must be connected to soft GND.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XL FAMILY

XC95288XL Programming Signal Definitions (Cont.)

Pin Type	TQ144	PQ208	BG256
V _{CC}		172	P
NC	119	173	B13
NC	120	174	A13
NC	121	175	D12
NC			C12
TDO	122	176	B12
GND	123	177	G
NC	124	178	A12
NC	125	179	B11
NC	126	180	C11
GND			A11
V _{CC}	127	181	P
V _{CC}			A10
A0	128	182	B10
NC		183	C10
V _{CC}		184	P
A1	129	185	D10
A2	130	186	A9
NC	131	187	B9
A3	132	188	C9
NC		189	D9
GND		190	G
NC	133	191	A8
NC			B8

Pin Type	TQ144	PQ208	BG256
A4	134	192	C8
NC			D8
NC		193	A7
NC		194	B7
GND			A6
V _{CC}			C7
V _{CC}			P
NC		195	B6
NC		196	A5
NC	135	197	D7
GND			G
A5	136	198	C6
NC	137	199	B5
A6	138	200	A4
NC	139	201	C5
NC			B4
A7	140	202	A3
NC			D5
NC		203	C4
V _{CC}	141	204	B3
NC	142	205	B2
NC	143	206	A2
GND	144	207	G
NC		208	C3

Note: Pins marked with * must be connected to soft GND.