


Rev	Revision Description	Drawn	Date	Appvd	Date
ENG	Initial Specification		8/29/00		
EO2	Added External Vpp 9500XV Programming		4/13/01		
01	Released		6/28/01		
02	Added jedec files to Matrix object		8/1/01		
03	Removed Version Code		9/21/01		



Specification for Programming  
XC9500XV Devices

DRAWN BY **BE**      DATE 8/29/00

**TOLERANCES**

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CHECKED BY

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ENG APPROVAL

DATE

MFG APPROVAL

DATE

SIZE

DRAWING NUMBER

REV.

**A**

**SPD0013**

**03**

SCALE

SHEET 1 OF

36

Unless otherwise specified,  
dimensions are in inches.

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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XC9500XV FAMILY

## 1. Introduction

This document pertains to the following devices and packages:

9536XV - PLCC44, CSP48, VQFP44

9572XV - PLCC44, CSP48, VQFP44, and  
TQFP100

95144XV - TQFP100, TQFP144, and CSP144

95288XV - TQFP144, PQFP208, FGA256,  
and CSP280

The device programming and verification procedures are similar to those used with standard FLASH memories. Initially, and after each erasure, all cells in the device are in the logical "0" (00H) state.

The Xilinx software generates device programming files in JEDEC format. The JEDEC file also contains information specific to each device, which will be compared to the device being programmed. Each product contains a ROM portion with a manufacturer's code to identify Xilinx as the manufacturer and a product code to identify the device. Please refer to the Add.dat file for specific code information.

## 2. Features

### 2.1 Erase

The device is electrically erasable. The algorithm has to perform a blank check on the device to ensure all bits are erased before allowing programming.

### 2.2 Addressing

The device is addressed as a byte-wide memory with several significant exceptions. There are several illegal addresses and some bytes in which not all bits can be programmed. The legal device addresses are contained on the included Add.dat floppy disk.

### 2.3 Operating Modes

The device has two operating modes: Program and Erase. Program is used for selectively changing FLASH cells within the device. Erase is the procedure used to erase the device. All other operations make use of the programming mode. This includes Stand Alone Verify, Blank Check, Load, and reading of the Signature String, Manufacturer's and Product Codes.

### 2.4 Signature String

The programmer or host computer must support a mode for reading and displaying the four signature string bytes of alphanumeric characters. Programming of these bytes is automatic because the Xilinx software inserts this string into the design file.

Note: All the sample design files (jedec format) included with this document, have a signature string of 'fast'. Unlike previous CPLD devices, you don't need to complement the data before displaying it. Display the data as you read it.

### 2.5 Device Security

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The device supports a read security feature which protects the design from being copied. A secured device may still be erased and reprogrammed.

## 3. Special Instructions

### 3.1 Device/ File Checksum Calculation

Contained in each JEDEC file is a fuse checksum (C-Field), which should be used to represent the file checksum. This checksum is the 16-bit sum (i.e. modulo 65,535) of the 8-bit word containing the fuse states of the entire device. Unused bits in the final 8-bit word must be set to zero. **The same method must be used to calculate the device checksum and the two should match.**

### 3.2 Compatibility Checks

#### 3.2.1 Adapter Type

The adapter should contain an electronically readable code for identification. The programming algorithm must check the adapter ID for compatibility with the target device. The JEDEC design file also contains information specific to the device pin count and fuse size, both of which must be compared to the adapter in use. The pin count, fuse size, and packages for each device are listed in the Add.dat file, supplied on the floppy disk.

## 4. Programming Sequence

The device programming sequence, illustrated in Figure 1, begins by verifying that the device design file and programming algorithm match the installed programmer adapter. This check is accomplished by comparing the programmer adapter ID, first to

all acceptable adapter IDs in the programmer algorithm and next to the fuse count and pin count contained in the JEDEC file. If a mismatch occurs, display message **A: “Incompatible Adapter Or File”** for current algorithm and terminate the programming sequence.

### 4.1 Read Manufacturer’s Code ID

Verify that the manufacturer’s code in the device matches the value listed in the Add.dat file contained on the supplied disk. If the manufacturer’s code ID does not match, display the message **B: “Manufacturer’s Code Error”** and terminate the programming sequence. The appropriate address may be found in the Add.dat file.

### 4.2 Read Product Code ID

Verify that the product code in the device matches the value listed in the Add.dat file contained on the supplied disk. If the product code ID does not match, display the message **C: “Product Code Error”** and terminate the programming sequence. The appropriate address may be found in the Add.dat file.

### 4.3 Device Blank Check

Verify that all FLASH cells are in the unprogrammed state ('0'). Blank Check is performed with Vpp set to VppBlank. If any one of the FLASH cells is programmed ('1'), display the message **E: “Device Not Blank”** and allow the option to erase the device. The device has to be blank prior to programming. If the device fails,

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display message **F: “Device Failed To Erase”** and terminate the programming sequence.

## 4.4 Device Programming and Margin Verify

At this point the actual programming cycle begins. To minimize the duration of the programming cycle, all FLASH cells in one ‘Word Line’ (WL) are first loaded before a short programming pulse is applied to the device. The amount of address in one WL varies from device to device. Specific address information of all address in all WL’s can be found in the Add.dat file of each device. **(Please note the setup and hold time for the programming pulse,  $T_{ENSV}$  and  $T_{ENH}$ .)** After programming all the WLs of the device, power down the device and perform a margin verify, as illustrated in Figure 6a. Power down after the margin verify cycle. The programming/ margin verify cycle is repeated until all FLASH cells pass. If any one of the cells fails margin testing, a number of retries is permitted. Each time, the full address array is reprogrammed. The number of retries ( $N_{MAX}$ ) can be calculated using the following equation:

$$N_{MAX} = \frac{300 \text{ ms}}{T_{PWPGM}}$$

Where  $t_{PWPGM}$  is the actual, measured value of the programming pulse width used. If after  $N_{MAX}$  attempts, any cell still fails to pass margin test, display the message **G: “Device Failed To Program”** and terminate the programming sequence.

## 4.5 Post Program Verify

Once programmed and margin verified successfully, power the device down then perform a stand alone verify or post program verify (See figure 6b). This operation is performed with  $V_{pp}$  at  $V_{ppvfy2}$ . If the device fails, display message **I: “Device Failed To Verify”** and terminate the programming sequence.

## 4.6 ISC\_DONE Bits

Two bits (ISCD & ISCDX) control whether or not outputs are enabled based on the configuration of the device. Specifically, if the ISCD bit is set and the ISCDX bit is unset, the outputs are enabled according to device configuration.

These bits are left in their default state (00) and hence the outputs are disabled by default.

Following the programming and stand alone verify sequence, the ISC\_DONE bits gets programmed, as illustrated in Figure 4a. If the device fails to ISC\_DONE, a number of retries are permitted. The number of retries ( $N_{MAX}$ ) can be calculated using the following equation:

$$N_{MAX} = \frac{300 \text{ ms}}{T_{PWPGM}}$$

Where  $T_{PWPGM}$  is the actual, measured value of the programming pulse width used for programming. If after  $N_{MAX}$  attempts, any ISC\_DONE address still fails to pass margin verify, display the message **K: “Device Failed To ISC\_DONE”** and terminate the programming sequence.

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**Table 1**

**Read Secure\***

Operation	Valid
Program	No
Erase	Yes
Verify	No
Load	No
Blank Check	No
Signature String	Yes
Mfg/Product Code	Yes

· See Add.dat file for addresses.

## 4.7 Secure Device

Following the programming , stand alone verify sequence, and ISC\_DONE, the algorithm should prompt the operator to secure the device, as illustrated in Figure 4. If the user elects not to secure the device, display the message **H: “Device Not Secured”** and terminate the programming sequence. If the user chooses to secure the device, program the security bits (see Figure 4) and display the message **D: “Device Secured”** and terminate the programming sequence. If the device fails to secure, a number of retries are permitted. The number of retries ( $N_{MAX}$ ) can be calculated using the following equation:

$$N_{MAX} = \frac{300 \text{ ms}}{T_{PWPGM}}$$

Where  $T_{PWPGM}$  is the actual, measured value of the programming pulse width used for programming. If after  $N_{MAX}$  attempts, any security address still fails to pass margin verify, display the message **J: “Device Failed To Secure”** and terminate the programming sequence.

If a device is Read Secured, the signature string, manufacturer’s code and product code can still be read. All other data is scrambled. Table 1 shows which operations may be performed after a device is Read Secured.

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## 5. Other Device Operations

### 5.1 Device Content Loading

Confirm that the device is not secured before attempting to load the content of the device. If **any** security bit has been programmed ('1'), display the message "**Device Secured**" and terminate the read sequence. The loading operation is performed with Vpp set to Vppvf2.

### 5.2 Stand Alone Verify

Confirm that the device is not secured before attempting this operation. If **any** security bit has been programmed ('1'), display the message "**Device Secured**" and terminate the stand alone verify operation. The operation is performed with Vpp set to Vppvf2.

### 5.3 Stand Alone Erase

To erase the device, follow the flow in Figure 3 and the timing according to Figure 9. See the Add.dat file for the Function Block (FB) erase address. Erase the device with Vpp set to Vppers and then perform an erase verify with Vpp set to Vppbnk. If any bits failed to erase, a number of retries are permitted. The number of retries ( $N_{\text{MAX-ERASE}}$ ) can be calculated using the following equation:

$$N_{\text{MAX-ERASE}} = \frac{3 \text{ s}}{T_{\text{ERASE}}}$$

Where  $T_{\text{ERASE}}$  is the actual, measured value of the erase pulse width used for erasing. If after  $N_{\text{MAX-ERASE}}$  attempts any addresses still fails to pass erase verify, display the message "**Device Failed to Erase**".

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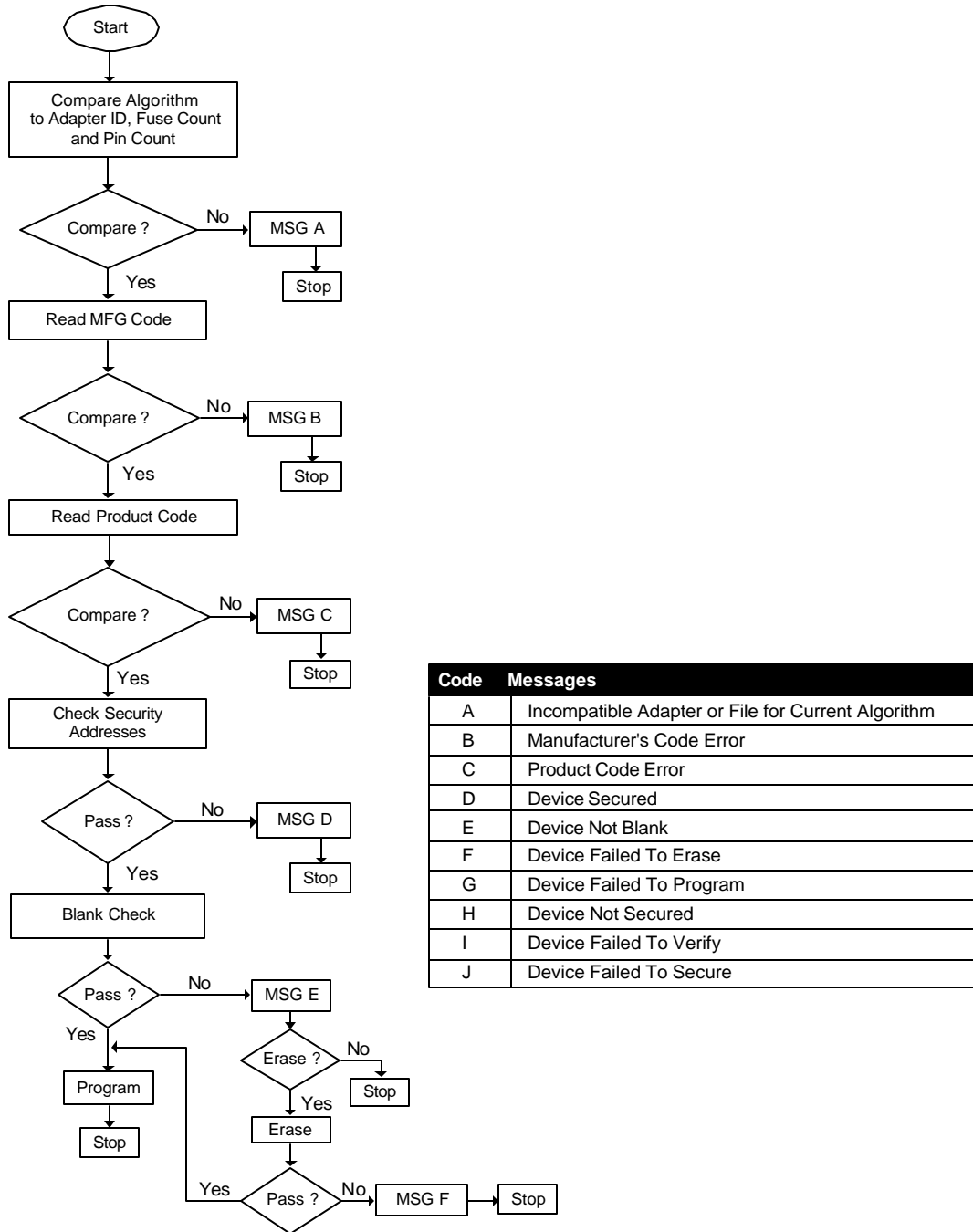


Figure 1. Overall Programming Sequence

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

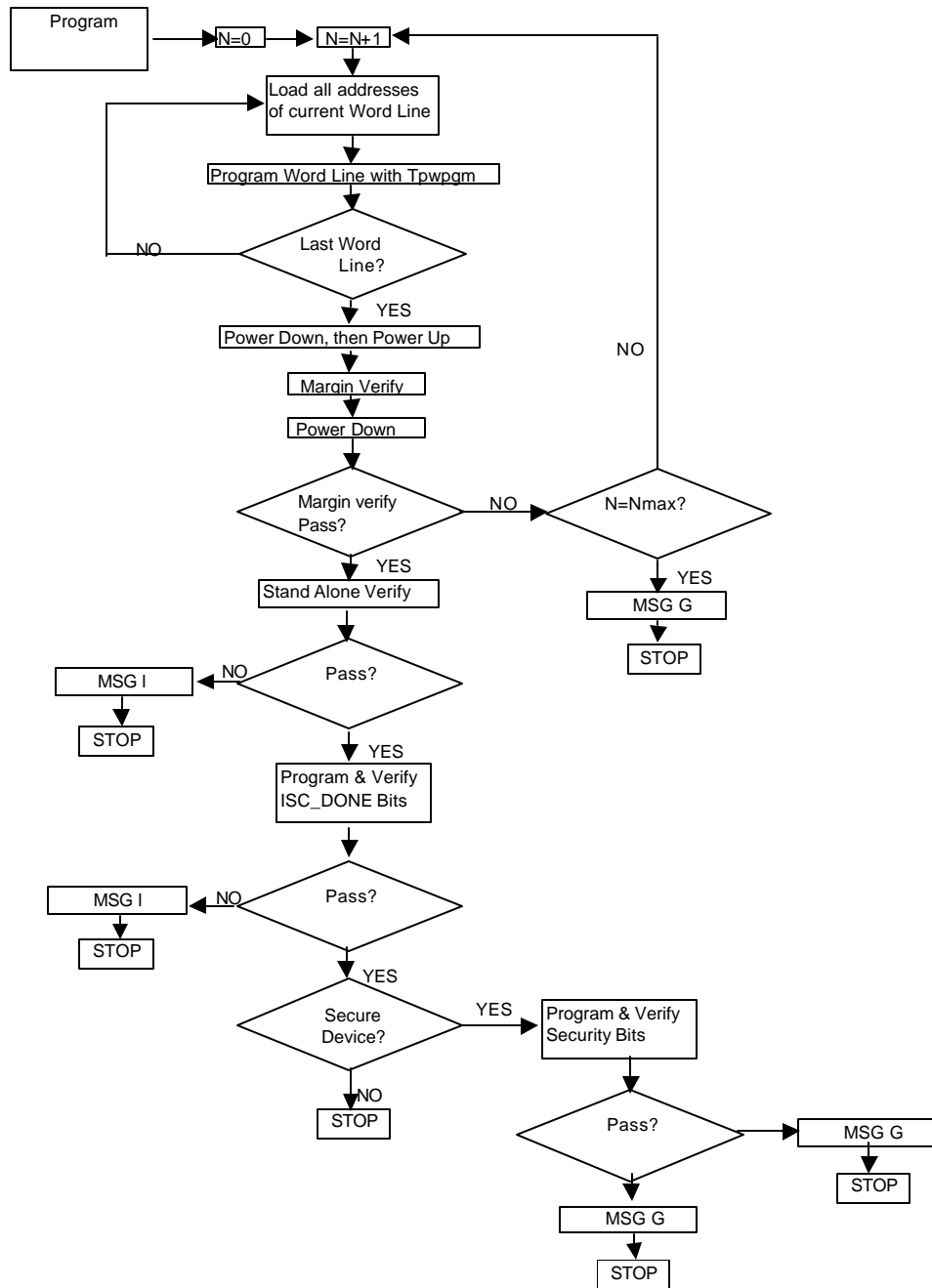


Figure 2. Programming Flow

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

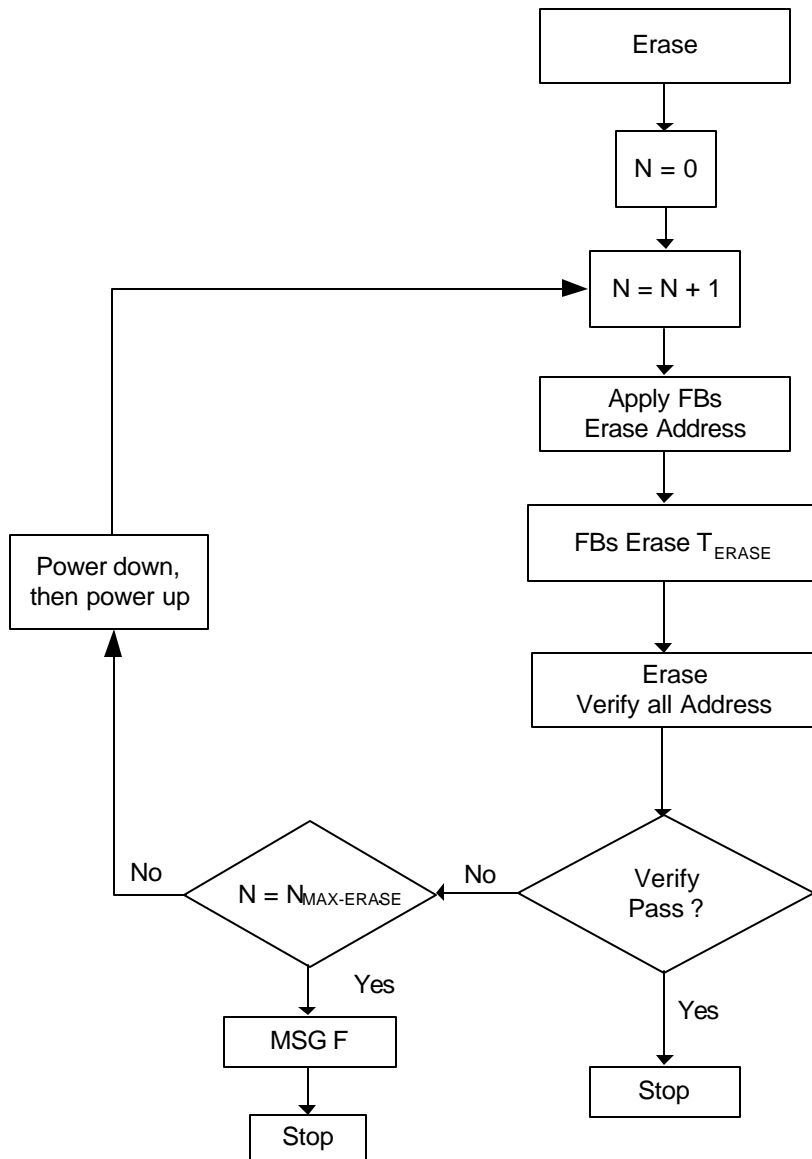


Figure 3. Erase Flow

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

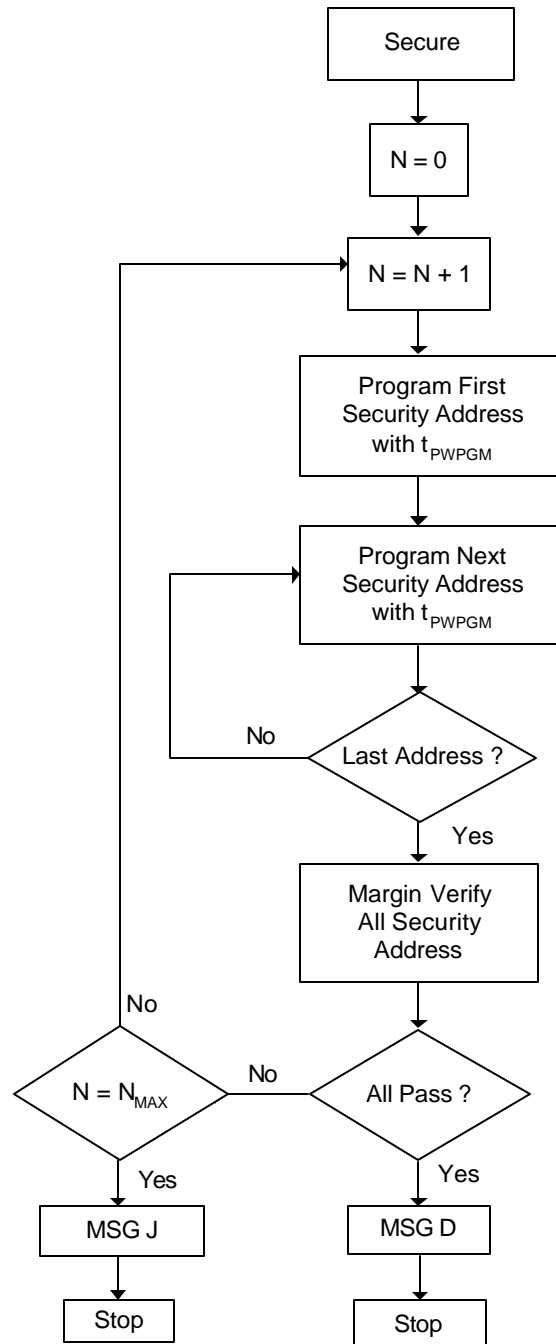


Figure 4. Secure Flow

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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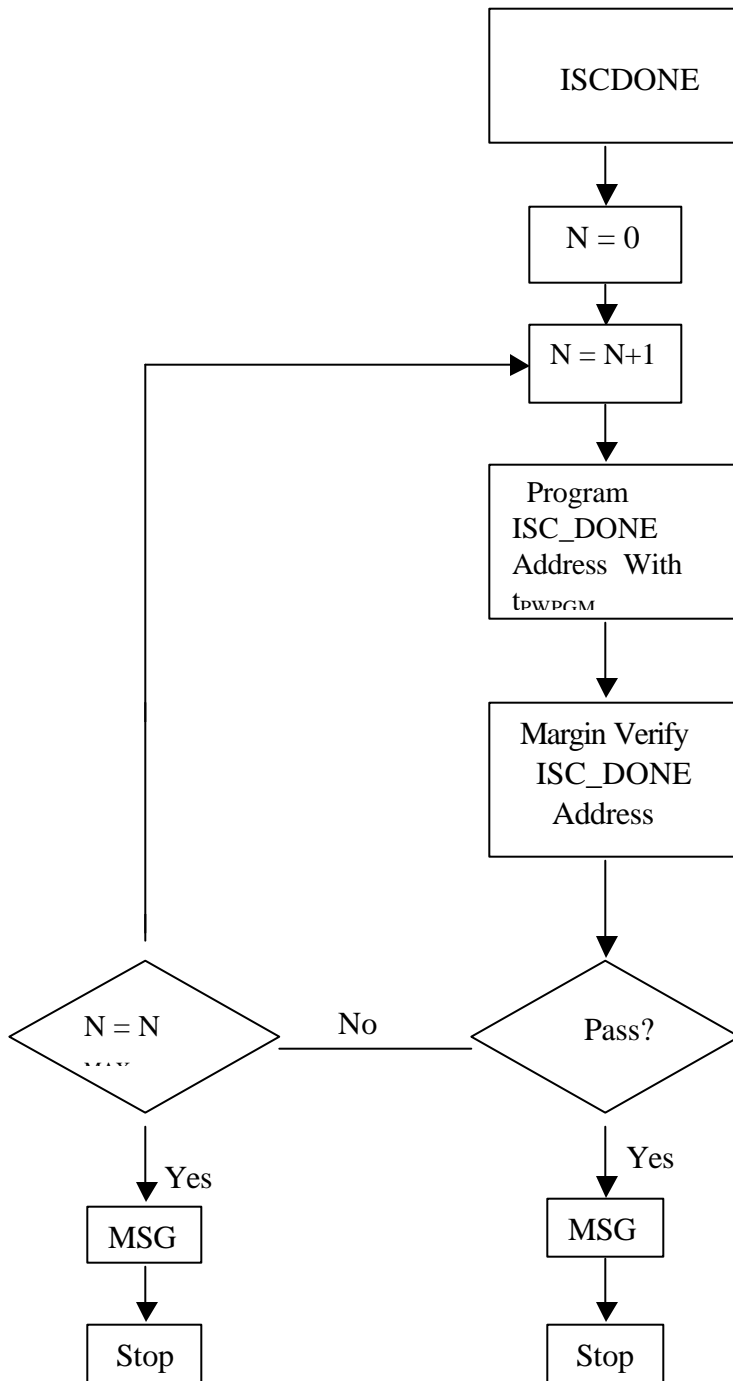


Figure 4a. ISCDONE Flow

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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## Common DC Programming and Erase Characteristics $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Description	Limits		
		Min	Max	Units
$I_{IL}$	Input Leakage		10	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Supply Current		400	mA
$I_{PP}$	$V_{PP}$ Supply Current		100	mA
$V_{IL}$	Low-Level Input Voltage	-0.5	0.8	V
$V_{IH}$	High-Level Input Voltage	1.7	3.6	V
$V_{OL}$	Low-Level Output Voltage for 3.3V operation ( $I_{OL} = 8 \text{ mA}$ , $V_{CC0} = 3.0\text{V}$ )		0.4	V
	Low-Level Output Voltage for 2.5V operation ( $I_{OL} = 8 \text{ mA}$ , $V_{CC0} = 2.3\text{V}$ )		0.4	V
	Low-Level Output Voltage for 1.8V operation ( $I_{OL} = 8 \text{ mA}$ , $V_{CC0} = 1.7\text{V}$ )		0.6	V
$V_{OH}$	High-Level Output Voltage for 3.3V operation ( $I_{OH} = -4 \text{ mA}$ , $V_{CC0} = 3.0\text{V}$ )	2.4		V
	High-Level Output Voltage for 2.5V operation ( $I_{OH} = -2 \text{ mA}$ , $V_{CC0} = 2.3\text{V}$ )	1.9		V
	High-Level Output Voltage for 1.8V operation ( $I_{OH} = -2 \text{ mA}$ , $V_{CC0} = 1.7\text{V}$ )	1.4		V
$V_{PPTST}$	$V_{PP}$ During Test Mode Entry	8.45	8.55	V
$V_{CCBNK}$	$V_{CC}$ During Blank Verify	2.4	2.6	V
$V_{PPNOM}$	Nominal $V_{PP}$	2.4	2.6	V
$V_{PPVF1}$	Margin Verify	2.4	2.6	V
$V_{PPBNK}$	$V_{PP}$ During Blank Verify	4.45	4.55	V
$V_{PPVF2}$	Stand Alone Verify, Secure Verify, Load	2.4	2.6	V

Note: Although min and max limits are given, Xilinx recommends that the mean be used whenever possible.

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## Specific DC Programming and Erase Characteristics $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Description	Product	Product Code	Min	Max	Units
$V_{CCNOM}$	Nominal $V_{CC}$	XC9536XV	42	2.375	2.625	V
		XC9572XV	41	2.375	2.625	V
		XC95144XV	40	2.375	2.625	V
		XC95288XV	43	2.375	2.625	V
$V_{PPERS}$	$V_{PP}$ Erase	XC9536XV	42	8.85	8.95	V
		XC9572XV	41	8.85	8.95	V
		XC95144XV	40	8.85	8.95	V
		XC95288XV	43	8.85	8.95	V
$V_{PPROG}$	$V_{PP}$ Program	XC9536XV	42	8.45	8.55	V
		XC9572XV	41	8.45	8.55	V
		XC95144XV	40	8.45	8.55	V
		XC95288XV	43	8.45	8.55	V

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## AC Programming Specifications

Symbol	Description	Limits		
		Min	Max	Units
$T_{D1}$	Delay from $V_{CCNOM}$ to $V_{PPNOM}$	100		$\mu$ s
$T_{D2}$	Delay from $V_{PPNOM}$ to TSTEN	10		$\mu$ s
$T_{PWTST}$	Test Mode Enable Pulse Width	200		$\mu$ s
$T_{S1}$	$V_{PP}$ Setup Time	100		$\mu$ s
$T_{S2}$	VFYEN or PGMEN Setup Time	1		$\mu$ s
$T_{S3}$	Test Pin Setup Time	1		$\mu$ s
$T_{S4}$	AD_STB Setup Time	1		$\mu$ s
$T_{H2}$	PGMEN or VFYEN Hold Time	1		$\mu$ s
$T_{H3}$	Test Pin Hold Time	1		$\mu$ s
$T_{H4}$	AD_STB Hold Time	1		$\mu$ s
$T_{PWSTB}$	AD_STB Pulse Width	2		$\mu$ s
$T_{AS}$	Address Setup Time	1		$\mu$ s
$T_{AH}$	Address Hold Time	1		$\mu$ s
$T_{PWPGM}^*$	Program Pulse Width	20	21 <sup>*</sup>	ms
$T_{VDV}$	VFYEN to Data Valid	1		$\mu$ s
$T_{ERASE}^{**}$	Erase Pulse Width	200	210 <sup>**</sup>	ms
$T_{VOFF1}$	$V_{PP}$ Off Before All Signals	10		$\mu$ s
$T_{VOFF2}$	All Signals Off Before $V_{CC}$	100		$\mu$ s
$T_{ENSU}$	Setup address & data before PGM/ERS strobe	200		$\mu$ s
$T_{ENH}$	Setup address & data after PGM/ERS strobe	200		$\mu$ s

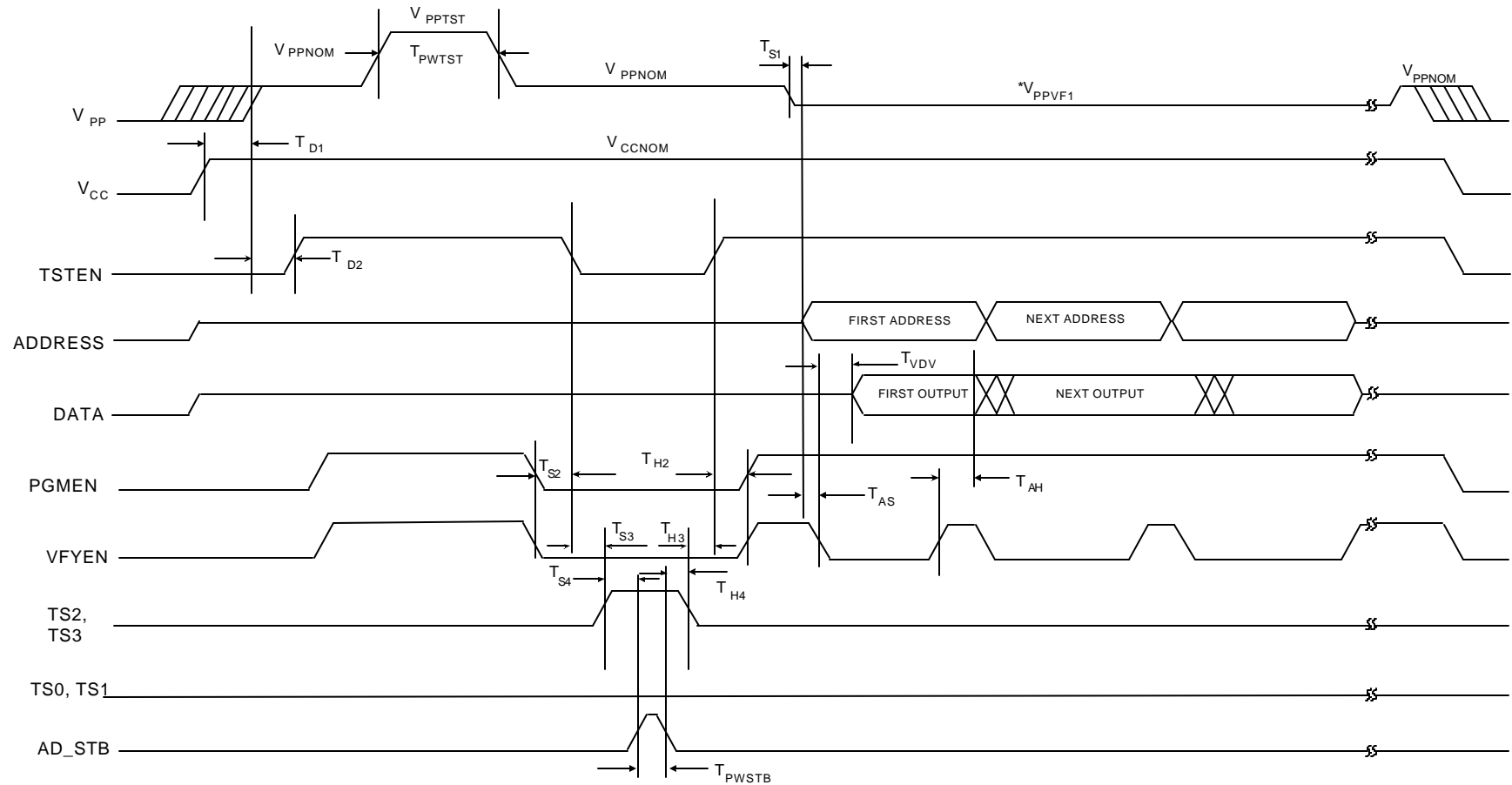
\* Recommended  $T_{PWPGM}$  is 20 ms,  $T_{PWPGM}$  Max is Recommended by Product Group

\*\* Recommended  $T_{ERASE}$  is 200 ms,  $T_{ERASE}$  Max is Recommended by Product Group



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\*V<sub>PPVF1</sub> only used for Margin Verify  
Figure 6a. Margin Verify

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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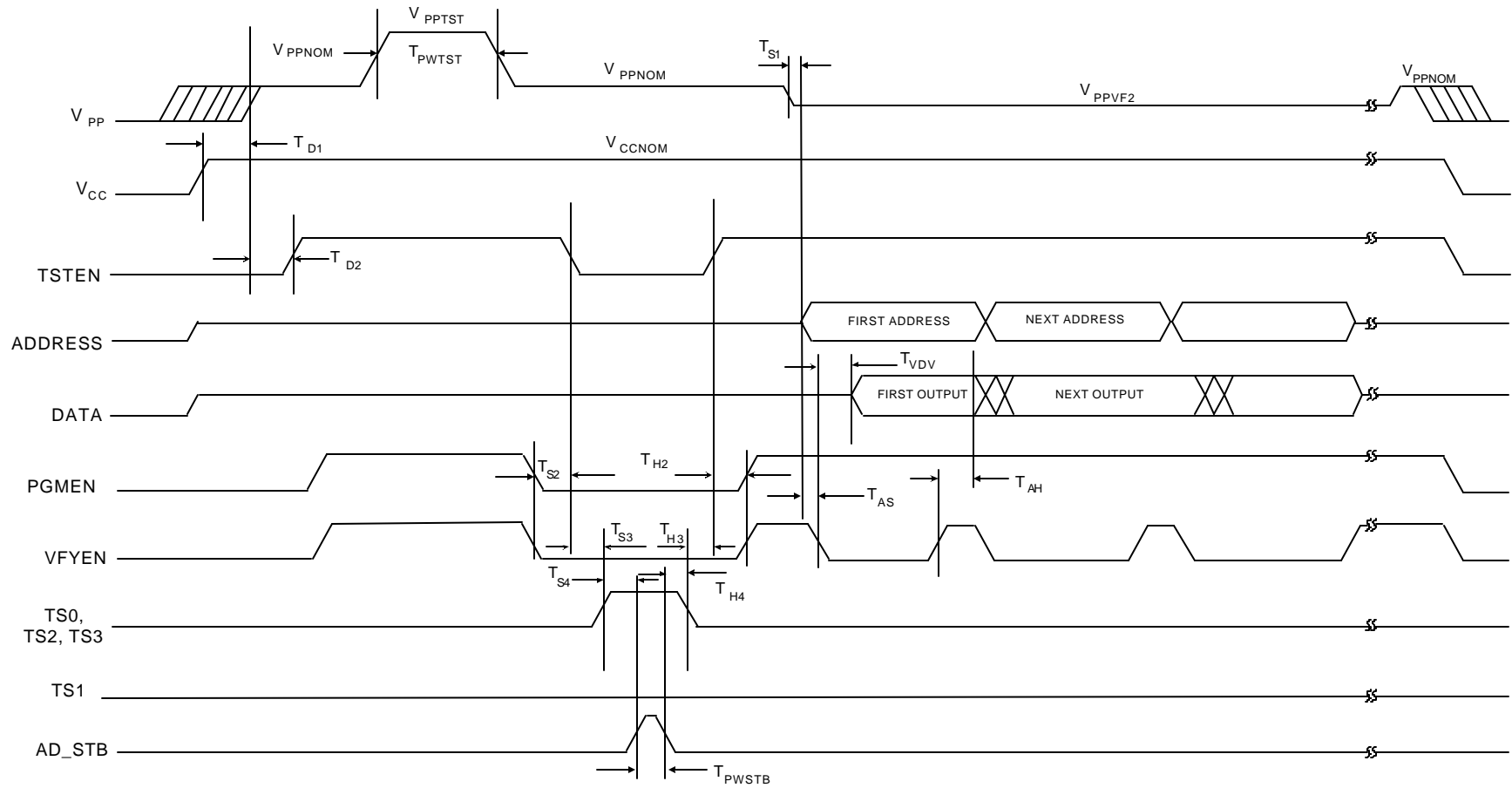


Figure 6b. Stand Alone Verify, Secure Verify, and Load



# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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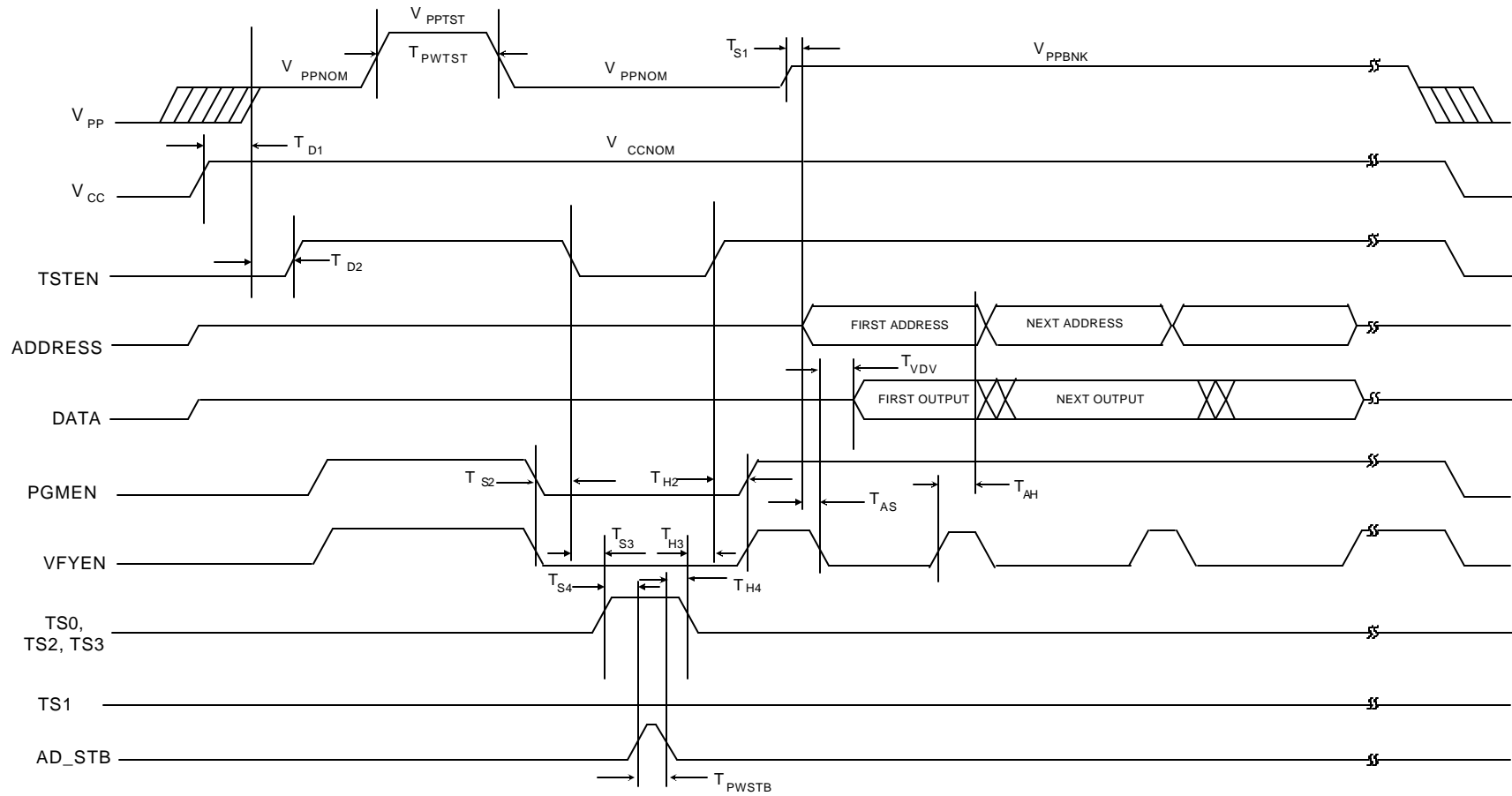


Figure 8. Blank Check

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

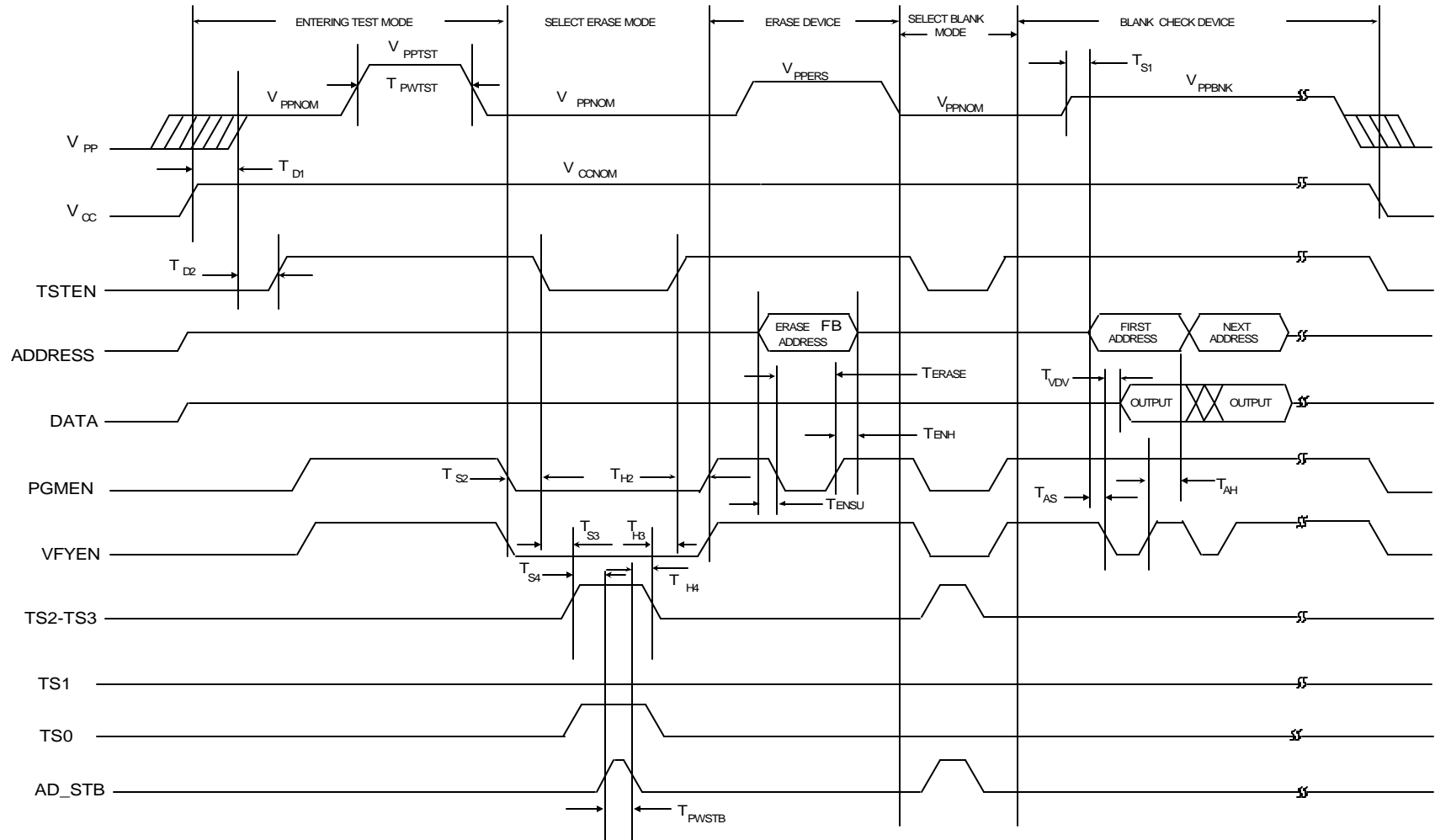


Figure9. Erase

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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XC9500XV FAMILY

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## XC9536XV Programming Signal Definitions

Pin Type	PC44	VQ44	48 CSP
NC	40	34	F6
V <sub>PP</sub>	41	35	F7
VFYEN	42	36	E6
*	43	37	E7
ADSTB	44	38	E5
TSTEN	1	39	D7
Ts2	2	40	D6
Ts3	3	41	C7
Ts0	4	42	C6
NC	5	43	B7
NC	6	44	B6
Ts1	7	1	A7
A8	8	2	A6
A9	9	3	C5
GND	10	4	A5
A10	11	5	B5
A11	12	6	A4
A12	13	7	B4
NC	14	8	A3
D3/TDI	15	9	B3
TMS	16	10	A2
TCK	17	11	A1
D0	18	12	B2

Pin Type	PC44	VQ44	48 CSP
D1	19	13	B1
D2	20	14	C2
V <sub>cc</sub>	21	15	C1
D4	22	16	C3
NC			D3
GND	23	17	D1
D5	24	18	D2
D6	25	19	E1
D7	26	20	E2
NC	27	21	F1
PGMEN	28	22	G1
NC			E4
A0	29	23	F2
A1/TDO	30	24	G2
GND	31	25	F3
V <sub>cc</sub>	32	26	G3
A2	33	27	E3
A3	34	28	G4
A4	35	29	F4
A5	36	30	G5
A6	37	31	F5
A7	38	32	G6
NC	39	33	G7

**NOTE:** Pins marked with \* must be connected to soft GND.

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## XC9572XV Programming Signal Definitions

Pin Type	PC44	VQ44	48 CSP
NC			
NC	40	34	F6
V <sub>PP</sub>	41	35	F7
NC			
A0	42	36	E6
*	43	37	E7
A1	44	38	E5
TSTEN	1	39	D7
A2	2	40	D6
PGMEN	3	41	C7
VFYEN	4	42	C6
NC			D4
NC			
GND			
NC	5	43	B7
NC	6	44	B6
A3	7	1	A7
NC			
D0	8	2	A6
D1	9	3	C5
GND	10	4	A5
D2	11	5	B5
NC			
D3	12	6	A4
D4	13	7	B4
V <sub>CC</sub>			
A4	14	8	A3
A5/TDI	15	9	B3
TMS	16	10	A2
A6/TCK	17	11	A1
NC			C4
NC			

Pin Type	PC44	VQ44	48 CSP
D5	18	12	B2
NC			
D6	19	13	B1
D7	20	14	C2
V <sub>CC</sub>	21	15	C1
NC	22	16	C3
NC			D3
NC			
GND	23	17	D1
A7	24	18	D2
A8	25	19	E1
A9	26	20	E2
A10	27	21	F1
NC			
NC			
A11	28	22	G1
NC			E4
A12	29	23	F2
NC			
NC			
A13/TDO	30	24	G2
GND	31	25	F3
V <sub>CC</sub>	32	26	G3
ADSTB	33	27	E3
NC	34	28	G4
NC			
NC			
TS0	35	29	F4
TS1	36	30	G5
TS2	37	31	F5
TS3	38	32	G6
NC	39	33	G7

**NOTE:** Pins marked with \* must be connected to soft GND.

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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## XC9572XV Programming Signal Definitions (Cont.)

Pin Type	TQ100
NC	1
NC	3
NC	4
V <sub>PP</sub>	5
NC	6
A0	8
NC	9
A1	10
*	11
NC	12
TSTEN	13
NC	14
PGMEN	15
A2	16
VFYEN	17
A3	18
NC	20
GND	21
NC	22
NC	23
NC	25
V <sub>CC</sub>	26
NC	27
A4	28
D0	29
D1	30
GND	31
D2	32
A5	33
D3	35
A6	36

PIN TYPE	TQ100
D4	37
V <sub>CC</sub>	38
NC	39
NC	40
NC	41
NC	42
GND	44
<b>TDI</b>	45
<b>TMS</b>	47
<b>TCK</b>	48
A7	49
A8	50
V <sub>CC</sub>	51
D5	52
NC	53
NC	54
D6	55
D7	56
V <sub>CC</sub>	57
NC	58
NC	59
A9	60
A10	61
GND	62
A11	63
NC	64
NC	65
NC	66
NC	67
NC	68

PIN TYPE	TQ100
GND	69
NC	70
NC	71
NC	72
NC	74
GND	75
NC	76
NC	77
NC	78
NC	79
NC	81
NC	82
<b>TDO</b>	83
GND	84
NC	85
NC	86
NC	87
V <sub>CC</sub>	88
ADSTB	89
A12	90
A13	91
NC	92
NC	93
TS0	94
TS1	95
TS2	96
TS3	97
V <sub>CC</sub>	98
NC	99
GND	100

**NOTE: Pins marked with \* must be connected to soft GND.**

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## XC95144XV Programming Signal Definitions

Pin Type	TQ100	CS144	TQ144
V <sub>CC</sub>		A1	1
NC	1	B1	2
NC	2	C2	3
NC		C1	4
NC	3	D4	5
NC	4	D3	6
NC		D2	7
V <sub>PP</sub>	5	D1	8
NC	6	E4	9
NC	7	E3	10
VFYEN	8	E2	11
NC		E1	12
ADSTB**	9	F4	13
NC		F3	14
ADSTB**	10	F2	15
PGMEN	11	F1	16
NC	12	G2	17
GND		G1	18
TSTEN	13	G3	19
NC	14	G4	20
TS0	15	H1	21
TS1	16	H2	22
NC		H3	23
TS2	17	H4	24
NC		J1	25
TS3	18	J2	26
NC	19	J3	27
NC	20	J4	28
GND	21	K1	29
NC	22	K2	30
NC		K3	31
NC	23	L1	32
NC	24	L2	33
NC	25	L3	34
NC		M1	35
GND		M2	36

Pin Type	TQ100	CS144	TQ144
V <sub>CC</sub>	26	N1	37
NC	27	N2	38
NC		M3	39
A8	28	N3	40
NC		K4	41
V <sub>CC</sub>		L4	42
A9	29	M4	43
NC		N4	44
A10	30	K5	45
NC		L5	46
GND	31	M5	47
NC		N5	48
A11	32	K6	49
A12	33	L6	50
NC	34	M6	51
A13	35	N6	52
A14	36	M7	53
NC	37	N7	54
V <sub>CC</sub>	38	L7	55
NC	39	K7	56
NC	40	N8	57
NC	41	M8	58
NC		L8	59
NC	42	K8	60
NC	43	N9	61
GND	44	M9	62
<b>TDI</b>	45	L9	63
NC	46	K9	64
<b>TMS</b>	47	N10	65
NC		M10	66
<b>TCK</b>	48	L10	67
NC		N11	68
D0	49	M11	69
NC		L11	70
D1	50	N12	71
GND		M12	72

Note: Pins marked with \* must be connected to soft GND.

\*\* The signal ADSTB should be applied to 2 pins on the device simultaneously.

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## XC95144XV Programming Signal Definitions (Cont.)

Pin Type	TQ100	CS144	TQ144
V <sub>CC</sub>	51	N13	73
D2	52	M13	74
NC		L12	75
NC	53	L13	76
NC		K10	77
NC	54	K11	78
NC		K12	79
D3	55	K13	80
NC		J10	81
D4	56	J11	82
NC		J12	83
V <sub>CC</sub>	57	J13	84
D5	58	H10	85
NC	59	H11	86
D6	60	H12	87
D7	61	H13	88
GND		G12	89
GND	62	G13	90
NC	63	G11	91
NC	64	G10	92
NC	65	F13	93
NC	66	F12	94
NC		F11	95
NC	67	F10	96
NC		E13	97
NC	68	E12	98
GND	69	E11	99
NC	70	E10	100
NC		D13	101
NC	71	D12	102
NC		D11	103
NC	72	C13	104
NC	73	C12	105
NC	74	C11	106
NC		B13	107
GND	75	B12	108

Pin Type	TQ100	CS144	TQ144
V <sub>CC</sub>		A13	109
NC	76	A12	110
NC		B11	111
NC	77	A11	112
NC	78	D10	113
GND		C10	114
NC		B10	115
NC	79	A10	116
NC		D9	117
NC		C9	118
NC	80	B9	119
NC	81	A9	120
NC	82	D8	121
<b>TDO</b>	83	C8	122
GND	84	B8	123
NC	85	A8	124
NC	86	B7	125
NC	87	A7	126
V <sub>CC</sub>	88	C7	127
A0	89	D7	128
A1	90	A6	129
A2	91	B6	130
NC	92	C6	131
A3	93	D6	132
NC		A5	133
A4	94	B5	134
NC		C5	135
A5	95	D5	136
NC		A4	137
A6	96	B4	138
NC		C4	139
A7	97	A3	140
V <sub>CC</sub>	98	B3	141
NC		C3	142
NC	99	A2	143
GND	100	B2	144

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

**Note: Pins marked with \* must be connected to soft GND.**

## XC95288XV Programming Signal Definitions

Pin Type	TQ144	PQ208	FG256	CS280
V <sub>CC</sub>	1	1	P	C3
GND		2	G	G
GND			G	G
NC	2	3	D3	C2
NC		4	D2	B1
NC	3	5	E3	C1
NC	4	6	C2	D4
NC	5	7	D4	D3
NC			B1	D2
NC		8	E4	D1
NC			C1	E3
NC	6	9	E5	E2
NC	7	10	E2	E4
V <sub>PP</sub>	8	11	F4	E1
NC		12	F2	F3
V <sub>CC</sub>			P	F2
GND		13	G	G
NC		14	E6	F4
V <sub>CC</sub>			P	F1
NC	9	15	D1	G3
NC	10	16	G4	G2
VFYEN	11	17	E1	G1
NC	12	18	G3	G4
*	13	19	G2	H1
NC			F5	H3
NC	14	20	F1	H2
NC			G5	H4
ADSTB	15	21	H2	J1
PGMEN	16	22	H4	J2
NC	17	23	G1	J3
GND	18	24	G	G
TSTEN	19	25	H3	J4
V <sub>CC</sub>		26	P	K1
GND		27	G	G
NC		28	H1	K2
NC		29	H5	K3

Pin Type	TQ144	PQ208	FG256	CS280
NC	20	30	J1	K4
TS0	21	31	J5	L1
TS1	22	32	J2	L2
NC			J3	L3
NC	23	33	K1	L4
NC			J4	M1
TS2	24	34	K2	M2
NC	25	35	K5	M3
TS3	26	36	L1	M4
NC	27	37	K3	N1
NC	28	38	L2	N2
GND			G	G
V <sub>CC</sub>			P	N3
V <sub>CC</sub>			P	N4
NC		39	L5	P1
NC		40	M1	P2
NC		41	L4	P3
GND	29	42	G	G
NC		43	N1	P4
NC			L3	R1
NC	30	44	M2	R3
NC			M4	R2
NC	31	45	P1	R4
NC	32	46	M3	T1
NC	33	47	N2	T2
NC		48	N4	T3
NC	34	49	R1	U1
NC		50	N3	V1
NC	35	51	P2	U2
GND	36	52	G	G
V <sub>CC</sub>	37	53	P	V2
NC		54	P4	V3
NC	38	55	P5	W2
NC			T2	W3
NC	39	56	N5	T4
NC			R4	U4

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

**Note: Pins marked with \* must be connected to soft GND.**

## XC95288XV Programming Signal Definitions (Cont.)

Pin Type	TQ144	PQ208	FG256	CS280
A8	40	57	M5	V4
NC	41	58	R5	W4
V <sub>CC</sub>	42	59	P	U5
GND			G	G
A9	43	60	R6	V5
NC	44	61	N6	T5
NC		62	R3	W5
A10	45	63	M6	U6
NC	46	64	T3	V6
V <sub>CC</sub>		65	P	T6
NC		66	T4	W6
NC		67	P7	U7
NC			T5	V7
GND	47	68	G	G
NC		69	N7	W7
NC			R7	T7
NC	48	70	M7	W8
NC		71	T6	U8
A11	49	72	N8	V8
NC		73	T7	T8
V <sub>CC</sub>			P	W9
GND			G	G
V <sub>CC</sub>			P	V9
GND			G	G
A12	50	74	R8	U9
NC	51	75	P8	T9
A13	52	76	T8	W10
A14	53	77	M8	V10
A15	54	78	T9	U10
V <sub>CC</sub>	55	79	P	T10
NC			P9	W11
NC		80	R9	V11
GND		81	G	G
NC	56	82	M9	U11

Pin Type	TQ144	PQ208	FG256	CS280
NC		85	R10	V12
V <sub>CC</sub>			P	U12
GND			G	G
NC	59	86	T11	T12
NC		87	P10	W13
NC	60	88	T12	V13
NC	61	89	N10	U13
NC		90	T13	T13
NC		91	M11	W14
GND			G	G
V <sub>CC</sub>		92	P	V14
GND	62	93	G	G
TD1	63	94	R11	U14
NC			N11	T14
NC	64	95	T14	W15
TMS	65	96	N12	U15
NC	66	97	R12	V15
TCK	67	98	P12	T15
NC	68	99	T15	W16
V <sub>CC</sub>			P	V16
D0	69	100	R14	U16
NC		101	N13	W17
NC	70	102	R13	W18
D1	71	103	P13	V17
GND	72	104	G	G
V <sub>CC</sub>	73	105	P	V18
NC		106	P15	U18
NC		107	N14	V19
GND		108	G	G
NC		109	R16	U19
D2	74	110	N15	T16
NC			M15	T17
NC		111	M13	T18
NC	75	112	P16	T19

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

NC	57	83	T10	T11
NC	58	84	M10	W12

V <sub>CC</sub>			P	R17
NC		113	N16	R18

**Note: Pins marked with \* must be connected to soft GND.**

## XC95288XV Programming Signal Definitions (Cont.)

Pin Type	TQ144	PQ208	FG256	CS280
NC	76	114	M14	R16
GND			G	G
NC	77	115	L15	R19
NC	78	116	L13	P17
V <sub>CC</sub>			P	P18
GND			G	G
NC	79	117	M12	P16
D3	80	118	M16	P19
NC		119	K14	N17
NC		120	L16	N18
NC	81	121	K13	N19
NC			K15	N16
D4	82	122	L12	M19
NC	83	123	K16	M17
V <sub>CC</sub>	84	124	P	M18
D5	85	125	J14	M16
NC	86	126	J15	L19
D6	87	127	J13	L18
D7	88	128	J16	L17
GND	89	129	G	G
GND	90	130	G	G
NC	91	131	K12	L16
V <sub>CC</sub>		132	P	K19
NC	92	133	J12	K18
NC	93	134	H15	K17
NC	94	135	H14	K16
NC	95	136	G16	J19
NC			H13	J18
NC	96	137	G15	J17
NC	97	138	H16	J16
NC	98	139	F16	H19
NC		140	H12	H18

Pin Type	TQ144	PQ208	FG256	CS280
V <sub>CC</sub>			P	G18
V <sub>CC</sub>			P	G17
GND			G	G
NC	100	145	E15	G16
NC	101	146	F13	F19
NC	102	147	D16	F18
NC	103	148	F14	F17
NC			C16	F16
NC	104	149	E14	E19
NC	105	150	D15	E17
NC		151	G12	E18
NC	106	152	C15	E16
V <sub>CC</sub>		153	P	D19
NC	107	154	D14	D18
NC		155	B16	D17
GND	108	156	G	G
V <sub>CC</sub>	109	157	P	C19
NC	110	158	B13	B19
V <sub>CC</sub>			P	C18
NC	111	159	B14	B18
NC	112	160	C13	B17
NC		161	A15	A18
NC	113	162	C12	A17
NC			B12	D16
GND	114	163	G	G
NC	115	164	D13	C16
NC		165	A14	B16
NC	116	166	E13	A16
GND			G	G
NC		167	A13	C15
NC		168	C11	B15
NC		169	A12	D15

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

GND	99	141	G	G
NC		142	E16	H17
NC		143	G14	H16
NC		144	F15	G19

GND			G	G
V <sub>CC</sub>			P	A15
NC	117	170	B11	C14
NC	118	171	D11	B14

Note: Pins marked with \* must be connected to soft GND.

## XC95288XV Programming Signal Definitions (Cont.)

Pin Type	TQ144	PQ208	FG256	CS280
V <sub>CC</sub>		172	P	D14
NC	119	173	A11	A14
NC	120	174	D10	C13
NC	121	175	B10	B13
NC			E12	A13
<b>TDO</b>	122	176	A10	D13
GND	123	177	G	G
NC	124	178	F12	A12
NC	125	179	B9	C12
NC	126	180	C9	B12
GND			G	G
V <sub>CC</sub>	127	181	P	D12
V <sub>CC</sub>			P	A11
A0	128	182	A9	B11
NC		183	D9	C11
V <sub>CC</sub>		184	P	D11
A1	129	185	E10	A10
A2	130	186	E11	B10
NC	131	187	A8	C10
A3	132	188	C8	D10
NC		189	B8	A9
GND		190	G	G
NC	133	191	D8	B9
NC			A7	C9

Pin Type	TQ144	PQ208	FG256	CS280
A4	134	192	E9	D9
NC			B7	A8
NC		193	D7	B8
NC		194	A6	C8
GND			G	G
V <sub>CC</sub>			P	D8
V <sub>CC</sub>			P	A7
NC		195	B6	B7
NC		196	E8	C7
NC	135	197	A5	D7
GND			G	G
A5	136	198	D6	A6
NC	137	199	B5	B6
A6	138	200	C6	C6
NC	139	201	A4	D6
NC			E7	A5
A7	140	202	A3	C5
NC			C5	B5
NC		203	A2	D5
V <sub>CC</sub>	141	204	P	A4
NC	142	205	B4	B4
NC	143	206	C4	C4
GND	144	207	G	G
NC		208	B3	A3

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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XC9500XV FAMILY

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**Note: Pins marked with \* must be connected to soft GND.**

## XC95288XV Programming Signal Definitions (Cont.)

Pin Type	FG256	CS280
POWER (P)	C7, C10, D5, D12, F3, F6, F7, F8, F9, F10, F11, G11, G13, H6, H11, J6, J11, K4, K6, K11, L6, L7, L8, L9, L10, L11, L14, N9, P6, P11	A4, A7, A11, A15, C3, C18, C19, D8, D11, D12, D14, D19, F1, F2, G18, K1, K19, M19, N3, N4, P18, R17, T6, T10, U5, U12, V2, V9, V14, V16, V18, W9
GND (G)	A1, A16, B2, B15, C3, C14, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, P3, P14, R2, R15, T1, T16	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15
NC	-	A1, A2, A19, B2, B3, C17, U3, U17, W1, W19

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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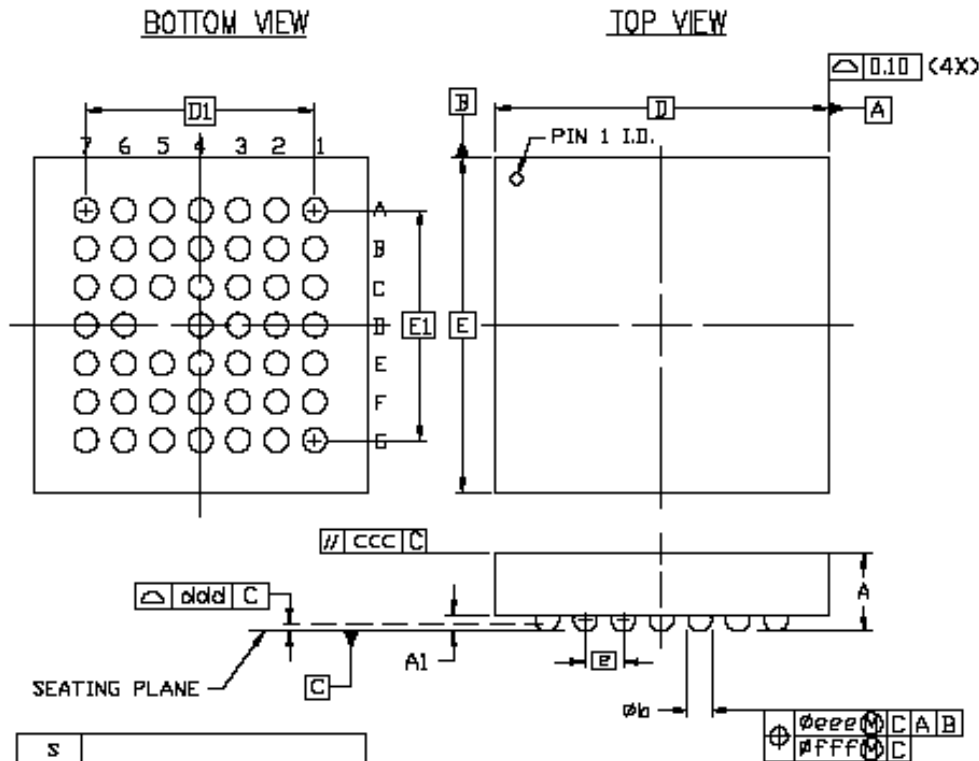
XC9500XV FAMILY

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## Chip Scale Package - CS48



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.30	<i>xxx</i>	1.80
A1	0.35	0.40	0.45
D/E	7.00 BSC		
D1/E1	4.80 BSC		
e	0.80 BSC		
phi b	0.45	0.50	0.55
ccc	<i>xxx</i>	<i>xxx</i>	0.10
ddd	<i>xxx</i>	<i>xxx</i>	0.10
eee	<i>xxx</i>	<i>xxx</i>	0.15
fff	<i>xxx</i>	<i>xxx</i>	0.08
M	7		

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.

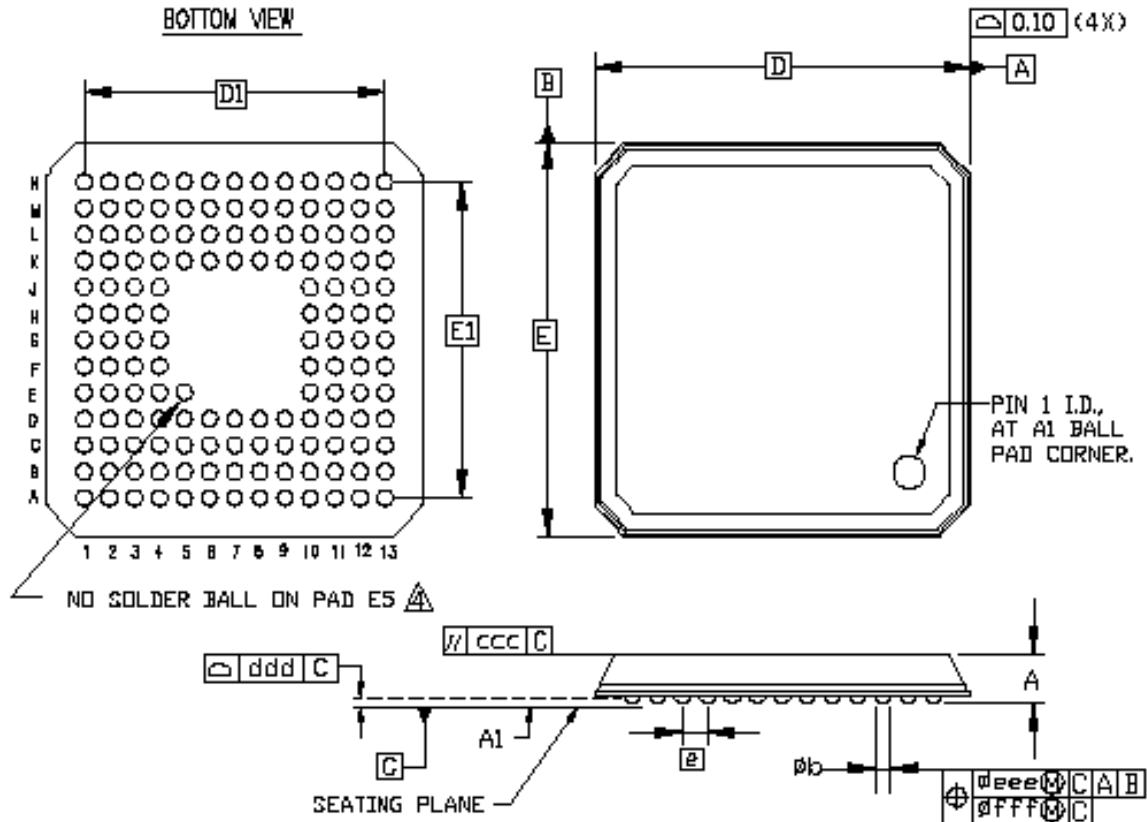
48-BALL CHIP SCALE BGA (CS48)

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## Chip Scale Package - CS144

BOTTOM VIEW



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.20
A <sub>1</sub>	0.35	0.40	0.45
D/E	12.00 BSC		
D <sub>1</sub> /E <sub>1</sub>	9.60 BSC		
e	0.80 BSC		
Pb	0.45	0.50	0.55
CCC			0.10
ddd			0.12
eee			0.15
FFF			0.08
M	13		

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-205-BE (DEPOPULATED).

PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144-BALL CHIP SCALE BGA (CS144)

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

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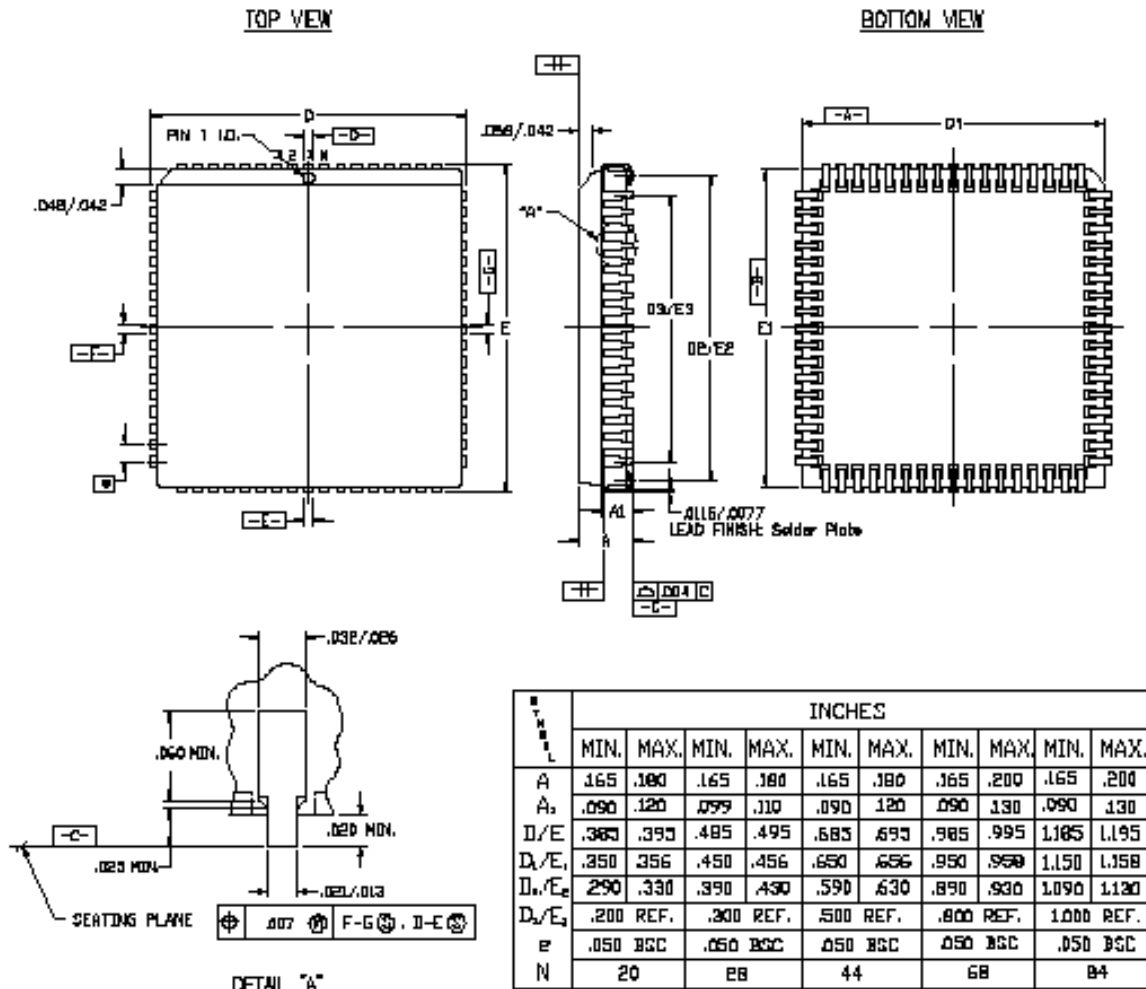
XC9500XV FAMILY

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# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## PLCC Packages - PC20, PC28, PC44, PC68, PC84



### NOTES:

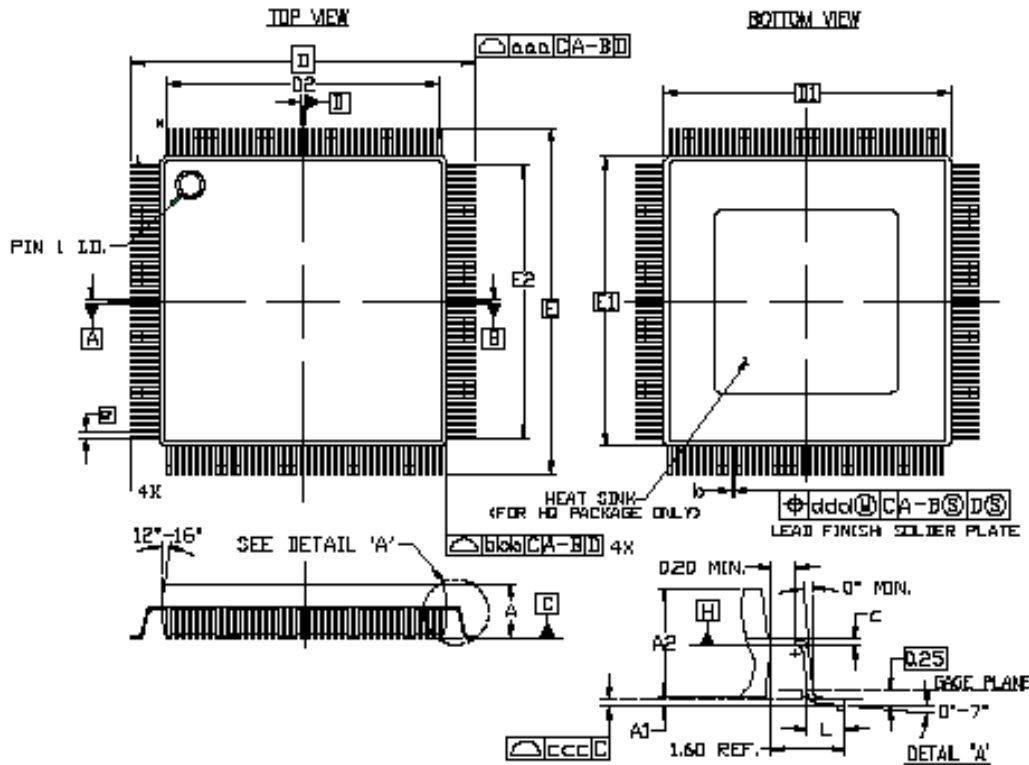
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE.
3. 'N' IS NUMBER OF TERMINALS.
4. CONFORM TO JEDEC MO-047
5. TOP OF PACKAGE MAY BE SMALLER THAN BOTTOM BY .010".

20, 28, 44, 68 and 84-PIN PLCC (PC20 THRU PC84)

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## PQ/HQFP Packages - PQ44, PQ160, PQ208, PQ240, HQ160, HQ208, HQ240



DIMENSION	PQ44			PQ/HQ160			PQ/HQ208			PQ/HQ240		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.15	2.15	2.35	3.70	3.70	4.10	3.70	3.70	4.10	3.70	3.70	4.10
A1	0.05	0.05	0.25	0.25	0.33	0.50	0.25	0.33	0.50	0.25	0.30	0.50
A2	1.95	2.00	2.10	3.20	3.40	3.60	3.20	3.40	3.60	3.20	3.40	3.60
A3/E	13.20 BSC			31.20 BSC			30.60 BSC			34.60 BSC		
A4/E1	10.00 BSC			28.00 BSC			28.00 BSC			32.00 BSC		
A5/E2	8.00 REF.			25.35 REF.			25.50 REF.			29.50 REF.		
L	0.73	0.88	1.03	0.73	0.88	1.03	0.50	0.60	0.75	0.50	0.60	0.75
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
b	0.30	0.30	0.45	0.22	0.22	0.40	0.17	0.22	0.27	0.17	0.22	0.27
c	0.13	0.13	0.23	0.13	0.13	0.23	0.09	0.13	0.20	0.09	0.13	0.20
aaa	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
bbb	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20
ccc	0.10	0.10	0.10	0.10	0.10	0.10	0.08	0.08	0.08	0.08	0.08	0.08
ddd	0.20	0.20	0.20	0.13	0.13	0.13	0.08	0.08	0.08	0.08	0.08	0.08
N	44			160			208			240		
REF.	JEDEC MS-022-AB			JEDEC MS-022-DD1			JEDEC MO-143-FA-1			JEDEC MO-143-GA		

### NOTES:

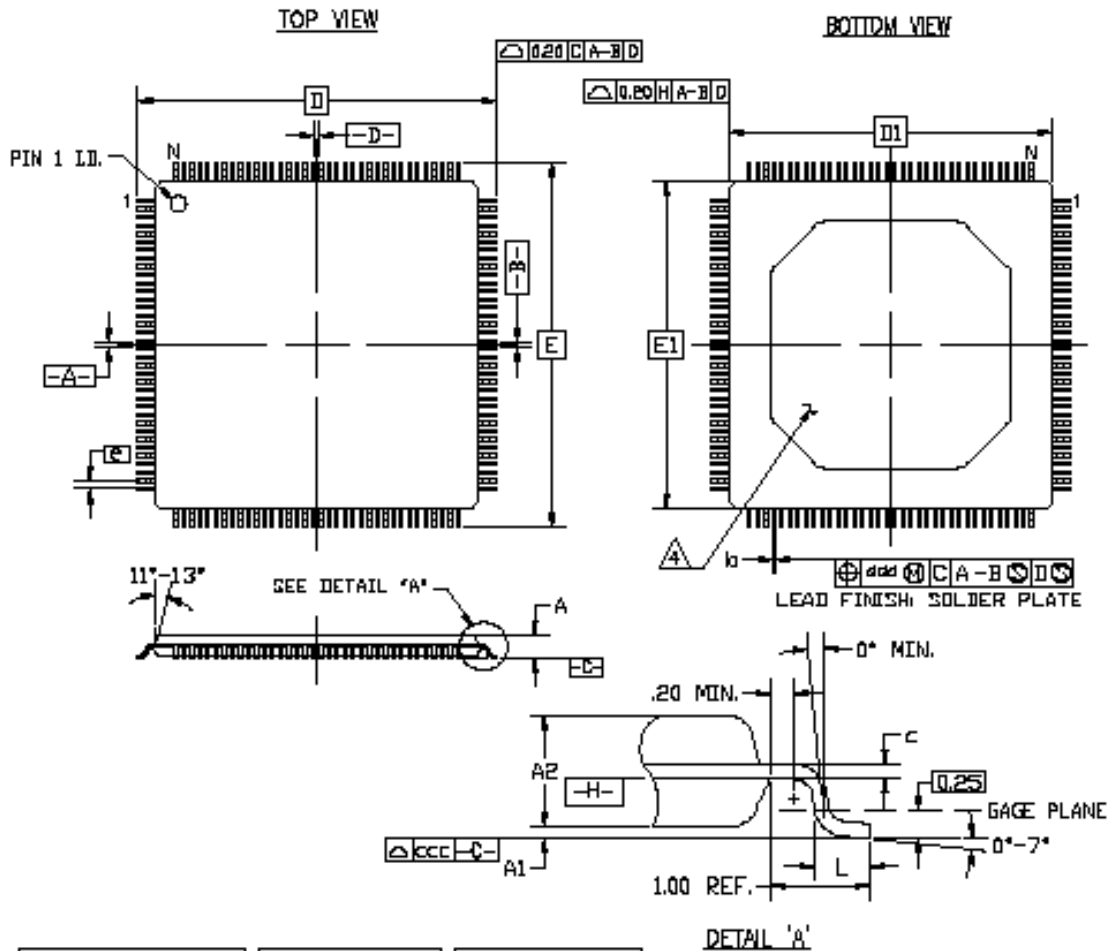
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN THE BOTTOM DIMENSIONS BY 0.20mm.
4. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

44, 160, 208, 240-PIN PQFP/HEAT SINK PQFP (PQ44, PQ/HQ160, 208, 240)

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## TQFP/HTQFP Packages - TQ100, TQ144, TQ176, HT100, HT144, HT176



Symbol	TQ/HT100			TQ/HT144			TQ/HT176		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~	~	1.60	~	~	1.60	~	~	1.60
A1	0.05	~	0.15	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.30	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45
D/E	16.00 BSC			22.00 BSC			26.00 BSC		
D1/E1	14.00 BSC			20.00 BSC			24.00 BSC		
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
b	0.50 BSC			0.50 BSC			0.50 BSC		
b	0.17	0.22	0.27	0.17	0.22	0.27	0.17	0.22	0.27
c	0.09	~	0.20	0.09	~	0.20	0.09	~	0.20
ccc	~	~	0.08	~	~	0.08	~	~	0.08
ddd	~	~	0.08	~	~	0.08	~	~	0.08
N	100			144			176		
REF.	JEDEC MS-026-BED			JEDEC MS-026-BFB			JEDEC MS-026-BGA		

NOTE:

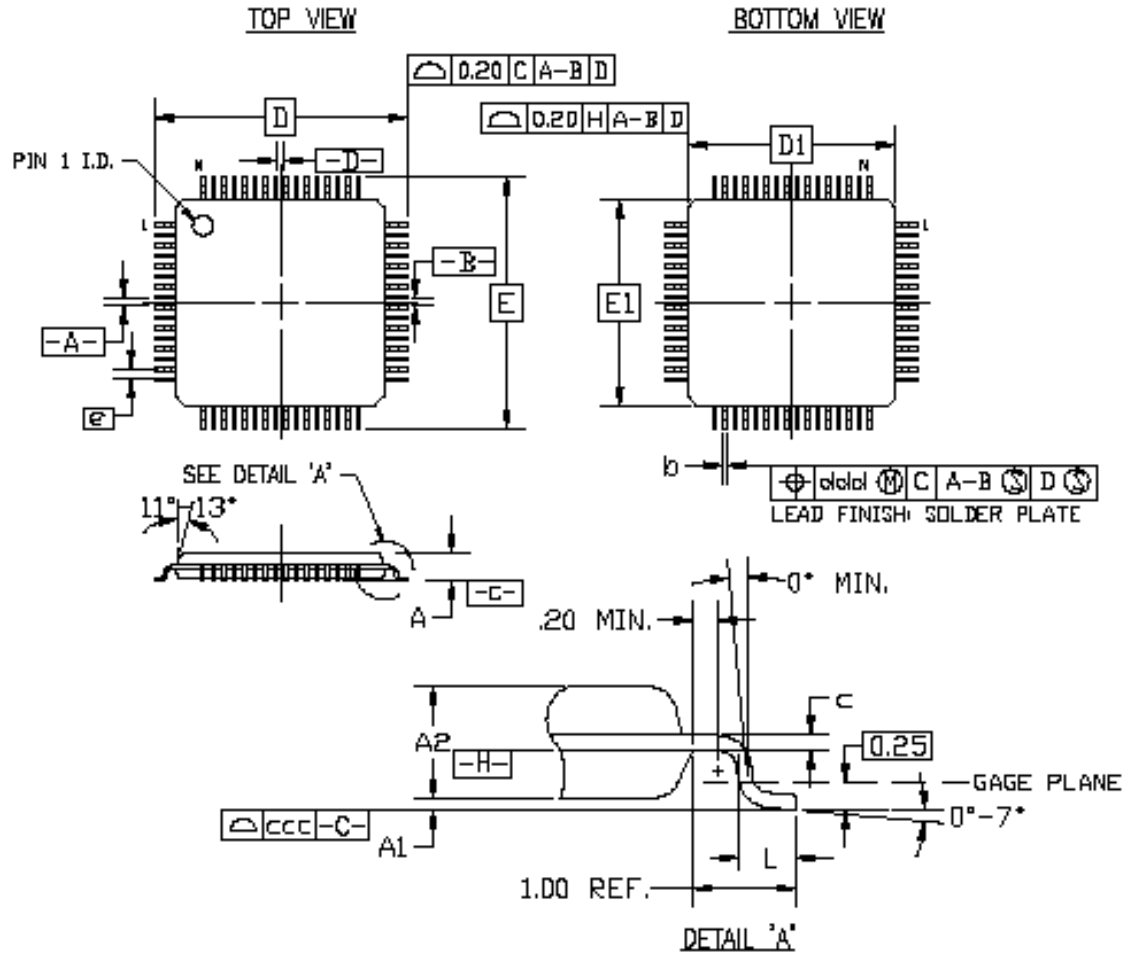
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5-1982
  2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
  3. PACKAGE TOP DIMENSION MAY BE SMALLER THAN THE BOTTOM DIMENSION BY 0.15mm.
- ⚠ THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HT".

100, 144, 176-PIN TQFP/HEAT SINK TQFP (TQ/HT100, 144, 176)

# XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500XV FAMILY

## VQFP Packages - VQ44, VQ64, VQ100



DIMENSION	VQ44			VQ64			VQ100		
	MILLIMETERS			MILLIMETERS			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~	~	1.20	~	~	1.20	~	~	1.20
A1	0.05	~	0.15	0.05	0.10	0.15	0.05	0.10	0.15
A2	0.95	1.00	1.05	0.95	1.00	1.05	0.95	1.00	1.05
D/E	12.00 BSC.			12.00 BSC.			16.00 BSC.		
D1/E1	10.00 BSC.			10.00 BSC.			14.00 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27	0.17	0.22	0.27
c	0.09	~	0.20	0.09	~	0.20	0.09	~	0.20
e	0.80 BSC.			0.50 BSC.			0.50 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
CCC	~	~	0.10	~	~	0.08	~	~	0.08
ddd	~	~	0.20	~	~	0.08	~	~	0.08
N	44			64			100		
REF.	JEDEC MS-026-ACB			JEDEC MS-026-ACB			JEDEC MS-026-AED		

### NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.

44, 64, 100-PIN PLASTIC VERY THIN QFP (VQ44, VQ64, VQ100)