



Rev	Revision Description	Drawn	Date	Appvd	Date
ENG	Initial Specification	BE/CH	2/11/00		
E01	Added .dat file to text document and Jedec files checked into Matrix object	CH	2/18/00		
E02	Added pages 31-53	CH	3/24/00		
E03	Added pages 54-67	CH	3/29/00		
E04	Added porten information from M. Lovejoy	CH	4/5/00		
E05	Added additional fuse map file.	CH	5/25/00		
E06	Replaced .dat files	CH	6/2/00		
E07	Include XCR3032XL	EH	4/29/01		
E08	Remove Program – Verify command, Corrected INIT pause times, Added Verify pause times, Added pause after ERASE	RD	7/10/01		
E09	Remove Gray Code Address Table to separate file	EH	8/24/01		
E10	Include XCR3384XL, XCR3512XL and new packages for XCR3064XL(PC44, CS48, CP56), XCR3128XL(CS144) and XCR3256XL(CS280, FT256)	EH / PP	8/31/01		
E11	Added 32 bit USERCODE programming	RD	11/21/03		
E12	Updated UES to include all bits	RD	05/24/04		
E13	Describing programming of the UES in details more similar to the actual software implementation	RD	05/25/04		

The Fuse Maps for this family is contained in Excel Spead Sheet files named PZ256.xls, PZ128.xls and 64xpla3JEDfm.xls Copies of these spread sheets are checked into the Matrix object for this specification.

<p>CONFIDENTIAL</p> <p>This document is the property of Xilinx Incorporated and contains information which is confidential and proprietary to Xilinx. No part of this document may be copied, reproduced or disclosed to third parties without the written consent of Xilinx Incorporated.</p>			<p>Specification for Programming Device XCR3032XL, XCR3064XL, XCR3128XL, XCR3256XL, XCR3384XL and XCR3512XL.</p>		
<p>TOLERANCES</p> <p> .X .XX .XXX</p>	CHECKED BY	DATE	<p>SIZE</p> <p>A</p>	<p>DRAWING NUMBER</p> <p>SPD0010</p>	<p>REV.</p> <p>E13</p>
	ENG APPROVAL	DATE			
	MFG APPROVAL	DATE			

Unless otherwise specified,
dimensions are in inches.

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SCALE

SHEET 1 OF

51

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

1. Introduction

This document pertains to the following devices and packages:

3032XL	VQ44, PC44, CS48
3064XL	VQ44, VQ100, PC44, CS48, CP56
3128XL	VQ100, TQ144, CS144
3256XL	TQ144, PQ208, CS280, FT256
3384XL	PQ208, TQ144, FT256, FG324
3512XL	PQ208, FT256, FG324

The device programming and verification procedures are similar to those used with standard non-volatile (NV) memories. Memory cells can be erased only as a single array, while programming of groups of individual cells is performed. Note that after successful completion of an erase operation, all cells in the device are in the logical “1” state. Erase and program operations are performed via the JTAG port and IEEE 1149.1 sixteen state TAP controller.

The Xilinx software generates device-programming files in JEDEC format. The JEDEC file also contains information specific to each device, which will be compared to the device being programmed. The manufacturer’s code to identify Xilinx (or in some cases Philips) as the manufacturer and the product code to identify the device are read via the Device Identification Register of the IEEE Standard 1149.1. Please refer to tables in a later section for codes.

2. Features

2.1 Erase

The device is electrically erasable. The algorithm has to perform a check on the device to ensure all bits are erased before allowing

programming. Note that erased cells are verified to logical 1 state.

2.2 Addressing

The device is addressed with a 9-bit address for the 3512, the 3384 and the 3256 device, an 8-bit address for both the 3128 and the 3064 devices and a 7-bit address for the 3032 device. The MSB selects upper (logical 1) or lower (logical 0) for a given address. The address, less MSB, is indexed with a Gray code count starting from zero and counting sequentially up to a maximum Gray code count. However, some bits of some addresses are “don't cares”; the fuse map for each device is available as an Excel spreadsheet. The legal device addresses are contained in the device specific Add.dat file.

2.3 Operations

The device has several independent operations: Program, Erase, Verify, and Initialize. To use these instructions, an enable command (ISP_ENABLE) must be executed via the JTAG controller. Furthermore, after performing the desired independent operations, a disable command (ISP_DISABLE) must be executed to properly configure all registers when returning to test-logic-reset state in the JTAG controller. Program is used for selectively changing groups of NV-cells within the device. Erase is the procedure used to erase all cells in the device in one operation. Verify is used to read NV-cell content. Initialize is to force configuration of the device to that loaded in the NV-memory without power cycling.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

2.4 Signature String

The programmer or host computer must support a mode for reading and displaying the data stored in the user storage area. Note that this storage area does not conform to IEEE 1149.1 signature specifications accessed by the 1149.1 Standard USERCODE instruction. The size of the user storage is shown in the Add.dat file. Note that the number of bits varies for XPLA3 family devices. Because the signature string is not part of the JEDEC file, programming of these bytes is an independent operation from the operation of programming configuration bits and can be performed at anytime.

Note that the user electronic signature string is not in the JEDEC file, but rather an arbitrary bit string defined by the customer.

2.5 Device Security

The device supports a read security feature, which protects the design from being copied. A secured device may still be erased and reprogrammed.

3. Special Instructions

3.1 Device/ File Checksum Calculation

Contained in each JEDEC file is a fuse checksum (C-Field), which should be used to represent the file checksum. The checksum is to be implemented according to JEDEC Standard Number 3A. **The same method must be used to calculate the device checksum and the two should match.**

Transmission checksum according to JEDEC Standard Number 3A can be implemented as well.

3.2 Compatibility Checks

3.2.1 Adapter Type

The adapter should contain an electronically readable code for identification. The programming algorithm must check the adapter ID for compatibility with the target device. The JEDEC design file also contains information specific to the device pin count and fuse size, both of which must be compared to the adapter in use. The pin count, fuse size, and packages for each device are listed in the corresponding Add.dat.

4. Programming Sequence

The device programming sequence, illustrated in Figure 1, begins by verifying that the device design file and programming algorithm match the installed programmer adapter. This check is accomplished by first comparing the programmer adapter ID to all acceptable adapter IDs in the programmer algorithm and next to the fuse count and pin count contained in the JEDEC file. If a mismatch occurs, display message **A: "Incompatible Adapter Or File"** for current algorithm and terminate the programming sequence.

4.1 Read Manufacturer's Code ID

Read the manufacturer's code in the device contained in the Device Identification Register defined in IEEE 1149.1 Standard. This register is read via ISP port with the IEEE 1149.1 IDCODE instruction. Note that the manufacturer code can be Xilinx and in some case Philips; the code translations are listed in Table 3. of this document. The next step is to verify that the

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

device part number listed in the JEDEC file is a valid part number for the manufacturer determined from the Device Identification Register. If the device part number is not valid for the device manufacturer, display the message **B: “Manufacturer’s Code Error”** and terminate the programming sequence.

4.2 Read Product Code ID

Read the product codes, both architecture and number of macrocells codes, of the device contained in the Device Identification Register defined in IEEE 1149.1 Standard. This register is read via ISP port with the IEEE 1149.1 IDCODE instruction. The code translations are listed in Table 4. of this document. The next step is to verify that the device part number listed in the JEDEC file is a correct for the architecture and number of macrocells determined from the Device Identification Register. If the device part number is not correct for the device architecture and number of macrocells, display the message **C: “Product Code Error”** and terminate the programming sequence.

4.3 Device Erase Check

Verify that all NV-cells are in the unprogrammed state ('1'). Bulk erase check is performed with ISP verify command (ISP_VERIFY) for each address. Recall that an ISP_ENABLE instruction must be executed prior to sequentially shifting in addresses, executing verify operation and shifting out data for actual data comparison. If any of the NV-cells are programmed ('0'), display the message **E: “Device Not Erased”** and allow the option to erase the device. The device has to be bulk

erased prior to programming. If the device fails, display message **F: “Device Failed To Erase”** and terminate the programming sequence.

A. Device Programming

At this point the actual programming cycle begins. The address and data are first loaded before a short programming pulse is applied to the device. This programming procedure should follow the verify procedure where an ISP_ENABLE command was executed first in the procedure and an ISP_DISABLE should not be part of the procedure. The number of address and data bits varies from device to device. Specific address information of all address and number of data bits can be found in the Add.dat file of each device. Programming is performed utilizing the sixteen-state TAP controller, hence, timing is insured.

4.5 Post-Program Verify

After programming all the addresses of the device, perform data verification, as illustrated in Figure 2. This verification procedure should follow the verify and programming procedure where an ISP_ENABLE command was executed first in the procedure and an ISP_DISABLE should not be part of the procedure. If any cell fails to verify, display the message **G: “Device Failed To Program”** and terminate the programming sequence. Note that this operation can be performed at any time.

4.6 Secure Device

Following the programming and post-program verify sequence, the algorithm should query the operator to secure the device, as illustrated in

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Figure 2. If the user elects not to secure the device, display the message **H: “Device Not Secured”** and terminate the programming sequence with an ISP_DISABLE instruction. If the user chooses to secure the device, program the security bit (see Figure 4), display the message **D: “Device Secured”** and terminate the programming sequence with an ISP_DISABLE instruction. If the device fails to verify secure, display the message **J: Device Failed To Secure”** and terminate the programming sequence with an ISP_DISABLE instruction. This procedure should follow the programming sequence without an ISP_DISABLE command being included until completing the secure query and response to query.

If a device is Read Secured, the signature string, manufacturer’s code and product code can still be read. All other data can not be read. Table 1 shows which operations may be performed after a device is Read Secured.

Note that the device is not Read Secured after programming the security bit until either an ISP init instruction is executed or the power is cycled.

Table 1

Read Secure*

Operation	Valid
Program	No
Erase	Yes
Verify	No
Blank Check	No
Signature String	Yes
Mfg/Product Code	Yes

* See Add.dat file for security bit address.

5. Other Device Operations

5.1 Device Bulk Erase

To erase the device, follow the flow in Figure 3 and the timing according to Figure **XXXX**. Note that all NV-memory (user configuration bits and signature string) are erased with this operation. Recall that an ISP_ENABLE instruction must be executed prior to executing the erase operation. If verification of any logic one (1) state of any bit fails after performing the erase operation, then display the message **“Device Failed to Erase** and terminate the programming sequence with an ISP_DISABLE instruction.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

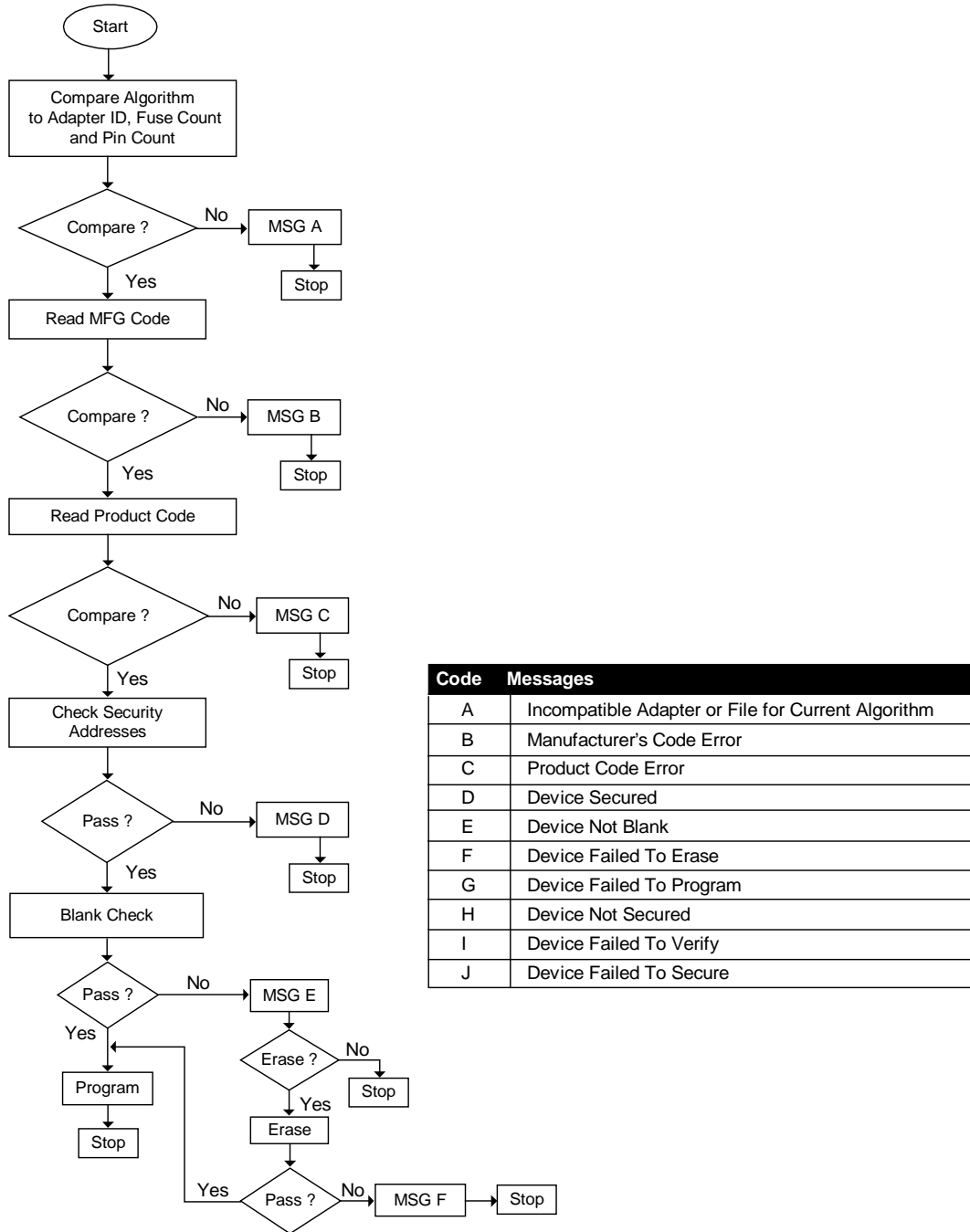


Figure 1. Overall Programming Sequence

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

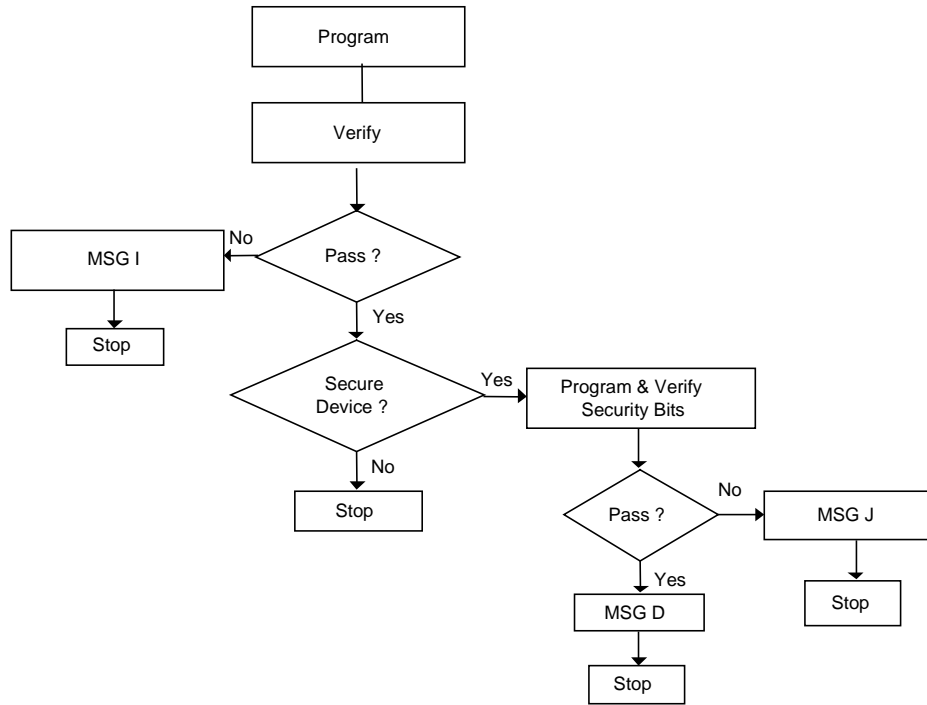


Figure 2. Programming Flow

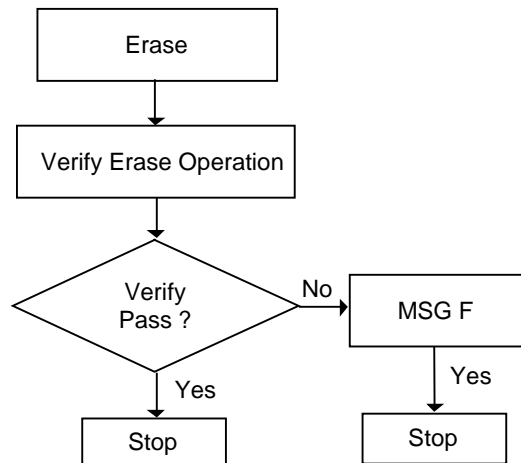


Figure 3. Erase Flow

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

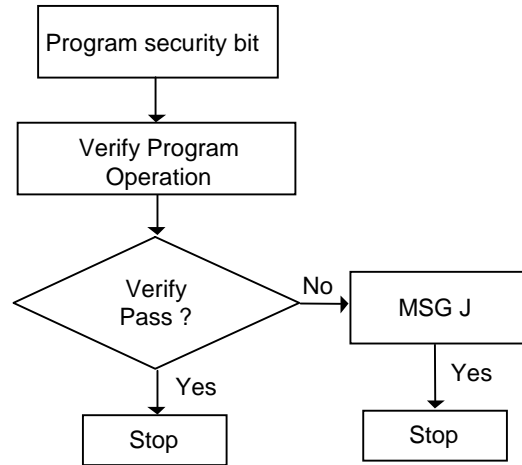


Figure 4. Secure Flow

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Table 2. Common DC Programming and Erase Characteristics $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Symbol	Description	Limits		
		Min	Max	Units
I_{IL}	Input Leakage		10	μA
I_{CC}	V_{CC} Supply Current		80	mA
V_{IL}	Low-Level Input Voltage	0	0.8	V
V_{IH}	High-Level Input Voltage	2.0	5.5	V
V_{OL}	Low-Level Output Voltage		0.4	V
V_{OH}	High-Level Output Voltage	2.4		V
V_{CCBNK}	V_{CC}	3.0	3.6	V

Note: Xilinx recommends that the mean be used whenever possible.

Table 3. Manufacturer ID codes

Manufacturer	ID code
Xilinx	00001001001
Philips	00000010101

Note: The Philips ID Code only applies to the original 3 die released from the Philips Fab (XCR3064XL, XCR3128XL, XCR3256XL). All newly released devices (after Dec 01) will only use the Xilinx ID Code.

Table 4. Device ID codes

Product	Package	Package Code	Architecture Code	Macrocell Count Code
3032XL	VQ44	110	010	000001
3032XL	PC44	101	010	000001
3032XL	CS48	100	010	000001
3064XL	VQ44	110	010	000100

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Product	Package	Package Code	Architecture Code	Macrocell Count Code
3064XL	VQ100	001	010	000100
3064XL	PC44	101	010	000100
3064XL	CS48	100	010	000100
3064XL	CP56	000	010	000100
3128XL	VQ100	001	010	001000
3128XL	TQ144	011	010	001000
3128XL	CS144	100	010	001000
3256XL	TQ144	011	010	010100
3256XL	PQ208	100	010	010100
3256XL	CS280	101	010	010100
3256XL	FT256	110	010	010100
3384XL	TQ144	011	010	010101
3384XL	PQ208	100	010	010101
3384XL	FT256	110	010	010101
3384XL	FG324	010	010	010101
3512XL	PQ208	100	010	010111
3512XL	FT256	110	010	010111
3512XL	FG324	010	010	010111

Table 5. AC Programming Specifications

Symbol	Description	Limits		
		Min	Max	Units
T _{PWPGM}	Program Pulse Width	10	11	ms
T _{ERASE}	Erase Pulse Width	100	110	ms

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3032XL Programming Signal Definitions

Function	VQ44 Pin Number	PC44 Pin Number	CS48 Pin Number
A3 / TDI	1	7	B1
A4	2	8	C2
A5	3	9	C1
PORT_EN	4	10	C3
A6	5	11	D3
A7	6	12	D1
A8 / TMS	7	13	D2
A9	8	14	E1
VDDE	9	15	E2
A10	10	16	F1
A11	11	17	G1
A12	12	18	E4
A13	13	19	F2
A14	14	20	G2
A15	15	21	F3
GND	16	22	E3
VDDI	17	23	G4
B15	18	24	F4
B14	19	25	G5
B13	20	26	F5
B12	21	27	G6
B11	22	28	G7
B10	23	29	F7
GND	24	30	E6
B9	25	31	E7
B8 / TCK	26	32	E5
B7	27	33	D7
B6	28	34	D6
VDDE	29	35	C7
B5	30	36	C6
B4	31	37	D4
B3 / TDO	32	38	B7
B2	33	39	B6
B1	34	40	A6
B0	35	41	C5
GND	36	42	A5
IN3 / GCLK3	37	43	B5
IN2 / GCLK2	38	44	A4
IN1 / GCLK1	39	1	B4
IN0 / GCLK0	40	2	A3
VDDI	41	3	B3
A0	42	4	A2
A1	43	5	A1
A2	44	6	C4

CS48 No connect Package balls: B2,G3,F6,A7

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3064XL Programming Signal Definitions

Function	PC44 Pin Number	VQ44 Pin Number	CS48 Pin Number	CP56 Pin Number	VQ100 Pin Number
B7				A3	100
VDDE					3
B8 / TDI	7	1	B1	C1	4
B9	8	2	C2	D1	6
B10	9	3	C1	D3	8
B11					9
B12					10
PORT_EN	10	4	C3	E1	11
B13	11	5	D3	E3	12
B14	12	6	D1	F1	13
B15					14
D0 / TMS	13	7	D2	G1	15
D1	14	8	E1	F3	16
D2					17
VDDE	15	9	E2	H1	18
D3	16	10	F1	G3	19
D4	17	11	G1	J1	20
D5					21
D6					23
D7				K1	25
GNDE					26
D8	18	12	E4	K4	29
D9	19	13	F2	K2	30
D10	20	14	G2	K3	31
D11	21	15	F3	H3	32
D12			G3	H4	33
VDDE	23		G4	H5	34
D13					35
D14				K5	36
D15					37
GNDE	22	16	E3	K6	38
VDDI	23	17	G4	H5	39
C15					40
C14				K7	41
C13					42
GNDE					43
C12	24	18	F4	H6	44
C11	25	19	G5	H7	45
C10	26	20	F5	H8	46
C9	27	21	G6	J10	47
C8	28	22	G7	K9	48
VDDE					51
C7				K10	52
C6			F6	K8	54

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3064XL Programming Signal Definitions Continued

Function	PC44 Pin Number	VQ44 Pin Number	CS48 Pin Number	CP56 Pin Number	VQ100 Pin Number
C5					56
C4					57
C3	29	23	F7	H10	58
GNDE	30	24	E6	G10	59
C2					60
C1	31	25	E7	G8	61
C0 / TCK	32	26	E5	F10	62
A15					63
A14	33	27	D7	E10	64
A13	34	28	D6	F8	65
VDDE	35	29	C7	D10	66
A12					67
A11					68
A10	36	30	C6	E8	69
A9	37	31	D4	D8	71
A8 / TDO	38	32	B7	C10	73
GNDE					74
A7	39	33	B6	B10	75
A6					76
A5			A7	A10	79
A4				A5	80
A3				A9	81
VDDE					82
A2					83
A1	40	34	A6	A8	84
A0	41	35	C5	C8	85
GNDE	42	36	A5	A7	86
CLK3 / IN3	43	37	B5	A6	87
CLK2 / IN2	44	38	A4	C7	88
CLK1 / IN1	1	39	B4	C6	89
CLK0 / IN0	2	40	A3	C5	90
VDDI	3	41	B3	A4	91
B0	4	42	A2	C4	92
B1	5	43	A1	C3	93
B2	6	44	C4	A1	94
GNDE					95
B3					96
B4				B1	97
B5					98
B6				A2	99

Note: VQ100 No Connects: 1-2, 5, 7, 22, 24, 27-28, 49-50, 53, 55, 70, 72, 77-78

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3128XL Programming Signal Definitions

Function	TQ144 Pin Number	CS144 Pin Number	VQ100 Pin Number	Function	TQ144 Pin Number	CS144 Pin Number	VQ100 Pin Number
VDDE		D4	3	G2	54	N6	36
GNDE	3	D3		G1	55	M7	37
F1 / TDI	4	D2	4	G0	56	N7	
F2	5	D1	5	GNDI	57	L7	38
F3	6	E4	6	VDDI	58	K7	39
F4	7	E3	7	GNDE	59	N8	
F5	8	E2	8	D0	60	M8	
F6	9	E1	9	D1	61	L8	40
F10	10	F4	10	D2	62	K8	41
F11	11	F3		D3	63	N9	42
F12	12	F2		GNDE	64	M9	43
PORT_EN	13	F1	11	D4	65	L9	44
F13	14	G2	12	D5	66	K9	45
F14	15	G1	13	D6	67	N10	46
F15	16	G3	14	D10	68	M10	47
GNDE	17	G4		D11	69	L10	48
H0	18	H1		D12	70	N11	49
H1 / TMS	20	H2	15	D13	71	M11	50
H2	21	H3	16	D14	72	L11	
H3	22	H4	17	VDDE	73	N12	
H4	23	J1		D15	74	M12	
VDDE	24	J2	18	VDDE	76	L13	51
H5	25	J3	19	C15	77	K10	
H6	26	J4	20	C14	78	K11	52
H10	27	K1	21	C13	79	K12	53
H11	28	K2	22	C12	80	K13	54
H12	29	K3	23	C11	81	J10	55
H13	30	L1	24	C10	82	J11	56
H14	31	M2	25	C6	83	J12	57
H15	32	N1		C5	84	J13	58
GNDE	33	N2	26	GNDE	85	H10	59
G15	37	M3		C4	86	H11	
G14	38	N3		C3	87	H12	60
G13	39	K4	27	C2	88	H13	61
G12	40	L4	28	C1 / TCK	89	G12	62
G11	41	M4	29	C0	90	G13	
G10	42	N4	30	A15	91	G11	
G6	44	K5	31	A14	92	G10	63
G5	45	L5	32	A13	93	F13	64
G4	46	M5	33	A12	94	F12	65
VDDE	50	N5	34	VDDE	95	F11	66
VDDI	51	K6		A11	96	F10	
GNDI	52	L6		A10	97	E13	67
G3	53	M6	35	A6	98	E12	68

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3128XL Programming Signal Definitions Continued

Function	TQ144 Pin Number	CS144 Pin Number	VQ100 Pin Number	Function	TQ144 Pin Number	CS144 Pin Number	VQ100 Pin Number
A5	99	E11	69	CLK3 / IN3	125	B7	87
A4	100	E10	70	CLK2 / IN2	126	A7	88
A3	101	D13	71	CLK1 / IN1	127	C7	89
A2	102	D12	72	CLK0 / IN0	128	D7	90
A1 / TDO	104	D11	73	GNDI	129	A6	
GNDE	105	C13	74	VDDI	130	B6	91
A0	106	B12		E15	131	C6	
B0	107	A13	75	E14	132	D6	92
B1	109	A12	76	E13	133	A5	93
B2	110	B11	77	E12	134	B5	94
B3	111	A11	78	GNDE	135	C5	95
B4	112	D10	79	E11	136	D5	
B5	113	C10	80	E10	137	A4	
B6	114	B10	81	E6	138	B4	96
VDDE	115	A10	82	E5	139	C4	97
B10	116	D9	83	E4	140	A3	98
B11	117	C9	84	E3	141	B3	99
B12	118	B9	85	E2	142	C3	100
B13	119	A9		E1	143	A2	1
B14	120	D8		VDDE	144	B2	
B15	121	C8		E0	1	A1	2
VDDI	123	B8		F0	2	B1	
GNDI	124	A8	86				

Notes:

TQ144 No Connects: 19, 34-36, 43, 47-49, 75, 103, 108, 122

CS144 No Connects: B13, C1, C2, C11, C12, L2, L3, L12, M1, M13, N13

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3256XL Programming Signal Definitions

Function	TQ144 Pin No.	PQ208 Pin No.	FT256 Pin No.	CS280 Pin No.	Function	TQ144 Pin No.	PQ208 Pin No.	FT256 Pin No.	CS280 Pin No.
I1	1	154	C1	C3	P4	31	113	L5	R2
I0	2	153	D3	B1	P11	32	112	P1	R4
VDDE					GNDE	33		GND*	GND*
GNDE	3	152	GND*	GND*	P12		111	M4	T3
J0/TDI[0]	4 (TDI)	151	D1	D2	P13	34	110	R1	U1
J1		150	E4	D1	P14	35	109	N3	V1
J2	5	149	D2	E3	P15	36	108	T1	U2
J3	6	148	E3	E2	VDDE		107	VDDE*	V2
J4	7	147	E1	E4	GNDE			GND*	GND*
J11	8	146	F4	E1	O15	37	102	R4	W3
J12		145	F1	F5	O14		101	P5	U4
J13	9	144	G5	F3	O13	38	100	T4	W4
VDDE		143	VDDE*	F2	O12	39	99	N6	U5
J14	10	142	E2	F4	O11		98	R5	V5
J15	11	141	F3	G3	O4	40	97	T6	T5
L0		140	F2	G2	O3	41	96	T5	W5
L1		139	G4	G1	O2	42	95	M7	R6
L2	12	138	G1	G4	GNDE		94	GND*	GND*
PORT_EN	13				O1	43	93	R6	U6
L3	14	137	H1	H1	O0	44	92	N7	V6
L4	15	136	H4	H3	M15	45	91	T7	T6
L11	16	135	G2	H2	M14		90	P6	W6
GNDE	17	134	GND*	GND*	M13	46	89	R7	U7
L12		133	J1	J2	M12	47	88	P7	V7
L13	18	132	J3	J3	M11	48	87	T8	W7
L14	19	131	H2	K2	M4	49	86	N8	T7
L15		130	J5	K3	VDDE	50	85	VDDE*	U8
N0/TMS[0]	20 (TMS)	129	J2	K4	M3		84	R8	T8
N1		128	J4	L1	VDDI	51	83	VDDI*	V9
N2/TMS[1]	21	127 (TMS)	K1 (TMS)	L2 (TMS)	GNDI	52	82	GND*	GND*
N3	22	126	K3	L3	M2	53	81	P8	U9
VDDE		125	VDDE*	L4	M1	54	80	T9	T9
N4	23	124	K2	M1	M0		79	P9	W10
VDDE	24		VDDE*	L4	F0		78	R9	U10
N11	25	123	L1	M3	F1	55	77	N9	T10
N12		122	K4	M4	F2	56	76	T10	W11
N13	26	121	L3	N1	GNDI	57	75	GND*	GND*
N14	27	120	K5	N2	VDDI	58	74	VDDI*	V11
N15	28	119	M1	N3	F3		73	P10	U11
P0		118	L2	P1	GNDE	59	72	GND*	GND*
P1		117	M2	P2	F4	60	71	R10	T11
PORT_EN		116	N1	P3	F11	61	70	T11	W12
P2	29	115	M3	P4	F12	62	69	N10	U12
P3	30	114	N2	R3	GNDE			GND*	GND*

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3256XL Programming Signal Definitions Continued

Function	TQ144 Pin No.	PQ208 Pin No.	FT256 Pin No.	CS280 Pin No.	Function	TQ144 Pin No.	PQ208 Pin No.	FT256 Pin No.	CS280 Pin No.
F13	63	68	P11	T12	VDDE		23	VDDE*	J19
GNDE	64		GND*	GND*	C11	92	22	H13	J18
F14		67	M10	V13	C4	93	21	G16	J17
F15	65	66	R11	U13	C3	94	20	G14	J16
H0	66	65	T12	T13	VDDE	95		VDDE*	J19
H1	67	64	R12	W14	C2	96	19	F16	H19
VDDE		63	VDDE*	U14	C1	97	18	G13	H18
H2	68	62	N11	T14	C0	98	17	G15	H17
H3	69	61	T13	R14	A15		16	G12	H16
H4		60	P12	W15	A14		15	F15	G19
H11	70	59	R13	U15	GNDE		14	GND*	GND*
H12		58	M11	V15	A13	99	13	F14	G17
H13	71	57	T14	T15	A12	100	12	E16	G16
H14		56	N12	V16	A11	101	11	F13	F19
H15	72	55	R14	W17	A4	102	10	E15	F18
VDDE	73		VDDE*	T18	A3	103	9	E14	F17
GNDE		50	GND*	GND*	A2/TDO[0]	104 (TDO)	8	D16	F15
G15		49	P15	U19	A1		7	F12	E19
G14	74	48	L12	T16	GNDE	105		GND*	GND*
G13	75	47	N16	T17	A0	106	6	C16	E18
VDDE	76		VDDE*	T18	VDDE		5	VDDE*	D17
G12		46	M14	R15	B0	107	4	E13	B19
G11	77	45	M16	R17	B1	108	3	D15	B18
G4	78	44	L13	R18	B2		206	C13	B17
G3	79	43	N15	R16	B3		205	A14	A18
G2	80	42	M15	R19	B4	109	204	E11	A17
VDDE		41	VDDE*	P15	B11	110	203	A13	C16
G1		40	L16	P18	B12	111	202	D12	A16
G0	81	39	K12	P16	B13		201	B13	E15
E15		38	L15	N17	GNDE		200	GND*	GND*
E14	82	37	K13	N18	B14	112	199	C12	D15
E13	83	36	K16	N19	B15	113	198	A12	A15
E12		35	K14	N16	D0	114	197	D11	E14
E11	84	34	K15	M17	VDDE	115		VDDE*	C14
GNDE	85		GND*	GND*	D1	116	196	A11	D14
E4	86	33	L14	M18	D2	117	195	E10	A14
GNDE		32	GND*	GND*	D3		194	B12	C13
E3	87	31	J16	M16	D4	118	193	C11	B13
E2/TCK[1]	88	30 (TCK)	J13 (TCK)	L19 (TCK)	D11	119	192	B11	A13
E1		29	J15	L18	VDDE		191	VDDE*	D13
E0/TCK[0]	89 (TCK)	28	J14	L17	D12	120	190	A10	A12
C15		27	H16	L16	D13/TDO[1]	121	189 (TDO)	C10 (TDO)	C12 (TDO)
C14	90	26	H14	K18	D14		188	A9	B12
C13	91	25	H15	K17	D15	122	187	D9	D12
C12		24	H12	K16	VDDI	123	186	VDDI*	A11

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3256XL Programming Signal Definitions Continued

Function	TQ144 Pin No.	PQ208 Pin No.	FT256 Pin No.	CS280 Pin No.	Function	TQ144 Pin No.	PQ208 Pin No.	FT256 Pin No.	CS280 Pin No.
GNDI	124	185	GND*	GND*	K3		171	D7	A7
CLK3 / IN3	125	184	B10	B11	K2	138	170	A6	B7
CLK2 / IN2	126	183	C9	C11	K1		169	E7	C7
CLK1 / IN1	127	182	A8	D11	K0		168	B6	D7
CLK0 / IN0	128	181	B9	A10	I15	139	167	C6	A6
GNDI	129	180	GND*	GND*	I14	140	166	A5	B6
VDDI	130	179	VDDI*	B10	VDDE		165	VDDE*	C6
K15	131	178	B8	C10	I13	141	164	D6	D6
K14	132	177	D8	D10	I12	142	163	B5	E6
K13 / TDI[1]	133	176 (TDI)	A7 (TDI)	B9 (TDI)	I11		162	C5	A5
K12	134	175	C8	C9	I4	143	161	A4	C5
GNDE	135	174	GND*	GND*	VDDE	144		VDDE*	C6
K11	136	173	C7	B8	I3		160	E6	B5
K4	137	172	B7	C8	I2		159	B4	A4

Notes:

PQ208

- No Connects: 1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, and 208.

FT256

- GNDE and GNDI pads are connected to the following package balls: E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, and L11.
- VDDE pads are connected to the following package balls: F7, F8, F9, F10, G6, G11, H6, H11, J6, J11, K6, K11, L7, L8, L9, and L10.
- VDDI pads are connected to the following package balls: E8, E9, H5, J12, M8, and M9.
- No Connects: A1, A2, A3, A15, A16, B1, B2, B3, B14, B15, B16, C2, C3, C4, C14, C15, D4, D5, D10, D13, D14, E12, F5, G3, H3, L4, M5, M6, M12, M13, N4, N5, N13, N14, P2, P3, P4, P13, P14, P16, R2, R3, R15, R16, T2, T3, T15, T16.

CS280

- GND* = Ground pads that are connected to the following External Package Balls: E5, E7, E8, E9, E10, E11, E12, E13, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, R7, R8, R9, R10, R11, R12 and R13.
- No Connects: A1, A2, A3, A8, A9, A19, B2, B3, B4, B14, B15, B16, C1, C2, C4, C15, C17, C18, C19, D3, D4, D5, D8, D9, D16, D18, D19, E16, E17, F1, F16, G18, H4, J1, J4, K1, K19, M2, M19, N4, P5, P17, P19, R1, R5, T1, T2, T4, T19, U3, U16, U17, U18, V3, V4, V8, V10, V12, V14, V17, V18, V19, W1, W2, W8, W9, W13, W16, W18, and W19.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3384XL Programming Signal Definitions

Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #
VDDE	144		VDDE	VDDE	FB_22_14				N4
FB_17_16	1	154	B2	D3	FB_22_15		124	K2	P1
FB_17_15	2	153	B1	B2	FB_22_16	25	123	L1	P2
FB_17_14				C2	FB_24_1	26	122	K4	P3
FB_17_13			C1	E3	GNDE	GND		GND	GNDE
GNDE	3	152	GND	GNDE	FB_24_2	27	121	L3	P4
FB_17_5	4	151	D3	D2	FB_24_3	28	120	K5	R1
VDDE			VDDE	VDDE	FB_24_4	29	119	M1	R2
FB_17_4	5	150	C2	D1	FB_24_5	30		L2	R3
FB_17_3	6	149	F5	F4	FB_24_13	31	118	M2	T2
FB_17_2		148	D1	F3	FB_24_14	32	117	L4	T3
FB_17_1		147	E4	E2	PORT_EN	33	116	N1	T4
FB_18_1	7	146	D2	E1	FB_24_15			M3	U2
FB_18_2	8	145	E3	F2	VDDE			VDDE	VDDE
FB_18_3	9	144	E1	G4	FB_24_16	34	115	N2	U3
FB_18_4	10		F4	G3	FB_23_16		114	L5	V2
VDDE		143	VDDE	VDDE	FB_23_15		113	P1	U4
FB_18_5			F1	G2	FB_23_14	35	112	M4	V3
GNDE	GND		GND	GNDE	FB_23_13			R1	W1
FB_18_13		142	G5	H3	FB_23_5			N3	W2
FB_18_14		141	E2	H2	GNDE	GND		GND	GNDE
FB_18_15	11	140	F3	H1	FB_23_4		111	T1	W3
FB_18_16	12	139	F2	J4	FB_23_3		110	P3	Y2
GNDE	13				FB_23_2		109	P2	Y3
FB_20_1	14	138	G4	J3	FB_23_1	36	108	M5	AA2
FB_20_2		137	G1	J2	VDDE		107	VDDE	VDDE
FB_20_3		136	G3	K4	FB_21_16	37	106	N4	AA3
FB_20_4	15	135	H1	K3	FB_21_15	38		R2	Y4
GNDE	GND	134	GND	GNDE	FB_21_14	39			AB3
FB_20_5			H4	K2	GNDE	GND		GND	GNDE
FB_20_13			G2	K1	FB_21_13	40	104	T2	AA4
GNDE	17				FB_21_5		103	P4	Y5
FB_20_14	16	133	H3	L4	FB_21_4	41	102	R3	AA5
FB_20_15		132	J1	L3	FB_21_3	42	101	N5	AB4
FB_20_16	18	131	J3	L2	FB_21_2		100	T3	W6
VDDI			VDDI	M1	FB_21_1		99	M6	AB5
GNDI			GND	GNDI	VDDE			VDDE	VDDE
FB_22_1	19		H2	M2	FB_14_16	43	98	R4	Y6
FB_22_2		130	J5	M3	FB_14_15		97	P5	AA6
FB_22_3	20	129	J2	M4	FB_14_14	44	96	T4	AB6
FB_22_4	21	128	J4	N1	FB_14_13	45	95	N6	W7
FB_22_5 / TMS	22	127	K1	N2	FB_14_5			R5	Y7
FB_22_13	23	126	K3	N3	GNDE	GND	94	GND	GNDE
VDDE	24	125	VDDE	VDDE	FB_14_4			T6	AA7

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3384XL Programming Signal Definitions Continued

Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #
FB_14_3	46	93	T5	AB7	FB_6_3		60	T14	W16
FB_14_2	47	92	M7	Y8	FB_6_4		59	N12	AB17
FB_14_1		91	R6	AA8	FB_6_5		58	R14	AA17
FB_16_1		90	N7	AB8	FB_6_13		57	P13	AB18
FB_16_2	48	89	T7	W9	FB_6_14		56	T15	AA18
FB_16_3		88	P6	Y9	FB_6_15	68		P14	W17
FB_16_4	49	87	R7	AA9	VDDE			VDDE	VDDE
FB_16_5		86	P7	AB9	FB_6_16	69		T16	AA19
VDDE	50	85	VDDE	VDDE	FB_8_1	70	55	M12	Y18
FB_16_13			T8	W10	FB_8_2	71	51	R15	AA20
FB_16_14			N8	Y10	FB_8_3	72		N13	Y19
FB_16_15		84	R8	AA10	FB_8_4				AA21
VDDI	51	83	VDDI	AB10	GNDE	GND	50	GND	GNDE
GNDI	52	82	GND	GNDI	FB_8_5		49	P16	Y20
FB_16_16	53	81	P8	AB11	FB_8_13		48	N14	Y21
FB_15_16	54	80	T9	W11	FB_8_14		47	R16	W20
FB_15_15		79	P9	AA11	FB_8_15		46	M13	W21
GNDE	GND		GND	GNDE	VDDE	73		VDDE	VDDE
VDDE			VDDE	VDDE	FB_8_16	74	45	P15	Y22
FB_15_14		78	R9	Y11	FB_7_16		44	L12	W22
FB_15_13	55	77	N9	AB12	FB_7_15	75	43	N16	V20
FB_15_5	56	76	T10	AA12	FB_7_14		42	M14	V21
GNDI	57	75	GND	GNDI	FB_7_13			M16	U19
VDDI	58	74	VDDI	Y12	GNDE	GND		GND	GNDE
FB_15_4		73	P10	W12	FB_7_5			L13	V22
GNDE	59	72	GND	GNDE	VDDE	76	41	VDDE	VDDE
FB_15_3	60	71	R10	AB13	FB_7_4	77	40	N15	U20
FB_15_2				AA13	FB_7_3	78	39	M15	U21
VDDE			VDDE	VDDE	FB_7_2	79	38	L16	U22
FB_15_1			T11	Y13	FB_7_1	80	37	K12	T19
FB_13_1	61	70	N10	W13	FB_5_16	81	36	L15	T20
FB_13_2		69	P11	AB14	FB_5_15	82	35	K13	T21
FB_13_3	62	68	M10	AA14	FB_5_14	83	34	K16	T22
FB_13_4	63	67	R11	Y14	FB_5_13		33	K14	R20
GNDE	64		GND	GNDE	VDDE			VDDE	VDDE
FB_13_5		66	T12	W14	FB_5_5	84		K15	R21
FB_13_13		65	R12	AB15	FB_5_4			L14	R22
FB_13_14	65	64	N11	AA15	GNDE	85	32	GND	GNDE
VDDE		63	VDDE	VDDE	FB_5_3		31	J16	P19
FB_13_15			T13	Y15	FB_5_2 / TCK	86	30	J13	P20
FB_13_16	66		P12	AB16	FB_5_1		29	J15	P22
FB_6_1	67	62	R13	AA16	FB_3_16	87	28	J14	N19
FB_6_2		61	M11	Y16	FB_3_15		27	H16	N21
GNDE	GND		GND	GNDE	GNDI			GND	GNDI

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3384XL Programming Signal Definitions Continued

Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #
VDDI			VDDI	N20	FB_4_16	116	203	C13	B18
FB_3_14	88	26	H14	N22	FB_11_1			A14	A19
FB_3_13		25	H15	M22	FB_11_2		202	E11	D17
FB_3_5	89	24	H12	M19	FB_11_3		201	A13	A18
VDDE		23	VDDE	VDDE	FB_11_4			D12	C17
FB_3_4	90			M20	GNDE	GND	200	GND	GNDE
FB_3_3			H13	L21	FB_11_5	117	199	B13	B17
FB_3_2		22	G16	L20	FB_11_13		198	C12	A17
GNDE	GND		GND	GNDE	FB_11_14		197	A12	D16
FB_3_1		21	G14	L19	FB_11_15	118	196	D11	C16
FB_1_16	91	20	F16	K22	VDDE			VDDE	VDDE
FB_1_15		19	G13	K21	FB_11_16	119	195	A11	B16
FB_1_14		18	G15	K19	FB_9_16		194	E10	A16
FB_1_13	92	17	G12	J22	FB_9_15		193	B12	C15
FB_1_5	93	16	F15	J21	FB_9_14		192	C11	B15
GNDE	GND		GND	GNDE	FB_9_13			B11	A15
FB_1_4		15	F14	J19	FB_9_5	120		D10	D14
GNDE	GND	14	GND	GNDE	VDDE		191	VDDE	VDDE
FB_1_3		13	E16	H21	FB_9_4		190	A10	C14
FB_1_2			F13	H20	GNDE	GND		GND	GNDE
FB_1_1	94		E15	G22	FB_9_3 / TDO	121	189	C10	B14
FB_2_1		12	E14	G21	FB_9_2		188	A9	D13
VDDE	95		VDDE	VDDE	FB_9_1	122	187	D9	C13
FB_2_2	96	11	D16	G19	VDDI	123	186	VDDI	A13
FB_2_3	97	10	F12	F22	GNDI	124	185	GND	GNDI
FB_2_4	98	9	C16	F21	IN3 / CLK3	125	184	B10	A12
GNDE	GND		GND	GNDE	IN2 / CLK2	126	183	C9	D12
FB_2_5	99	8	E13	F20	IN1 / CLK1	127	182	A8	B12
FB_2_13	100		D15	E22	IN0 / CLK0	128	181	B9	C12
FB_2_14	101	7	D14	E21	GNDI	129	180	GND	GNDI
FB_2_15	102	6	B16	F19	VDDI	130	179	VDDI	A11
VDDE		5	VDDE	VDDE	FB_10_1		178	B8	B11
FB_2_16	103		C15	E20	FB_10_2		177	D8	C11
FB_4_1	104	4	A16	D22	VDDE			VDDE	VDDE
GNDE	105				FB_10_3 / TDI	131	176	A7	D11
FB_4_2	106	3	E12	C22	FB_10_4	132	175	C8	A10
FB_4_3	107			B21	FB_10_5				B10
FB_4_4	110		C14	B20	FB_10_13			C7	C10
GNDE	GND		GND	GNDE	GNDE	GND	174	GND	GNDE
FB_4_5	111	207	D13	C19	FB_10_14		173	B7	D10
FB_4_13	112	206	A15	B19	FB_10_15	133	172	D7	A9
FB_4_14	113	205	B15	A20	VDDE			VDDE	VDDE
FB_4_15	114	204	B14	C18	FB_10_16	134	171	A6	B9
VDDE	115		VDDE	VDDE	FB_12_16		170	E7	C9

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3384XL Programming Signal Definitions Continued

Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	TQ144 Pin #	PQ208 Pin #	FT256 Pin #	FG324 Pin #
FB_12_15		169	B6	D9	FB_19_16		162	B4	B6
FB_12_14		168	C6	A8	FB_19_15	140	161	D5	C6
GNDE	135		GND	GNDE	FB_19_14		160	A3	A5
FB_12_13	136	167	A5	B8	GNDE	GND		GND	GNDE
FB_12_5		166	D6	C8	FB_19_13		159	C4	D6
VDDE		165	VDDE	VDDE	FB_19_5	141	158	B3	A4
FB_12_4	137		B5	A7	FB_19_4	142		A1	B5
FB_12_3	138		C5	B7	FB_19_3			A2	C5
FB_12_2		164	A4	C7	FB_19_2	143	156	D4	B4
FB_12_1	139	163	E6	D7	FB_19_1		155	C3	C4

Notes:

TQ144

- No Connect Pins: Pin # 108, 109

PQ208

- No Connect Package Pins: 1, 2, 52, 53, 54, 105, 157, 208.

FT256

- All GNDE and GNDI pads are connected to the following package balls: E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, and L11.
- All VDDE pads are connected to the following package balls: F7, F8, F9, F10, G6, G11, H6, H11, J6, J11, K6, K11, L7, L8, L9, and L10.
- All VDDI pads are connected to the following package balls: E8, E9, H5, J12, M8, and M9.

FG324

- All GNDE and GNDI pads are connected to the following package balls: D4, D5, D18, D19, E4, E19, J9, J14, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, P9, P14, V4, V19, W4, W5, W18, and W19.
- VDDE pads are connected to the following package balls: D8, D15, H4, H19, J10, J11, J12, J13, K9, K14, L9, L14, M9, M14, N9, N14, P10, P11, P12, P13, R4, R19, W8, AND W15.
- No Connect Balls: A1, A2, A3, A6, A14, A21, A22, B1, B3, B13, B22, C1, C3, C20, C21, D20, D21, F1, G1, G20, H22, J1, J20, K20, L1, L22, M21, P21, T1, U1, V1, Y1, Y17, AA1, AA22, AB1, AB2, AB19, AB20, AB21, and AB22.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3512XL Programming Signal Definitions

Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #
VDDE		VDDE	VDDE	GNDI		GNDI	GNDI
FB_18_1	156	C1	D3	FB_31_15	130	J5	M2
FB_18_2	155	D3	B2	FB_31_14	129	J2	M3
GNDE		GNDE	GNDE	FB_31_13			M4
FB_18_3	154	C2	B1	FB_31_4	128	J4	N1
FB_18_4	153	F5	C2	FB_31_3/ TMS	127	K1	N2
GNDE	152	GNDE	GNDE	GNDE		GNDE	GNDE
FB_18_13			C1	FB_31_2		K3	N3
VDDE		VDDE	VDDE	FB_31_1	126	K2	N4
FB_18_14	151	D1	E3	VDDE	125	VDDE	VDDE
FB_18_15			D2	FB_29_16	124	L1	P1
FB_18_16	150	E4	D1	FB_29_15			P2
FB_20_1	149	D2	F4	VDDE		VDDE	VDDE
GNDE		GNDE	GNDE	FB_29_14	123	K4	P3
FB_20_2	148	E3	F3	GNDE		GNDE	GNDE
FB_20_3			E2	FB_29_13	122	L3	P4
FB_20_4	147	E1	E1	FB_29_4	121	K5	R1
FB_20_13			F2	FB_29_3	120	M1	R2
FB_20_14	146	F4	F1	VDDE		VDDE	VDDE
FB_20_15	145	F1	G4	FB_29_2			R3
FB_20_16	144	G5	G3	FB_29_1	119	L2	T1
VDDE	143	VDDE	VDDE	FB_27_16	118	M2	T2
FB_22_1	142	E2	G2	FB_27_15	117	L4	T3
GNDE		GNDE	GNDE	PORT_EN	116	N1 (PE)	T4 (PE)
FB_22_2	141	F3	G1	FB_27_14	115	M3	U1
FB_22_3			H3	VDDE		VDDE	VDDE
FB_22_4	140	F2	H2	FB_27_13			U2
FB_22_13			H1	FB_27_4	114	N2	U3
FB_22_14	139	G4	J4	FB_27_3	113	L5	V1
VDDE		VDDE	VDDE	FB_27_2			V2
FB_22_15		G1	J3	FB_27_1	112	P1	U4
FB_22_16	138	G3	J2	FB_25_16	111	M4	V3
FB_24_1	137	H1	J1	FB_25_15	110	R1	W1
FB_24_2	136	H4	K4	GNDE		GNDE	GNDE
FB_24_3	135	G2	K3	FB_25_14	109	N3	W2
GNDE	134	GNDE	GNDE	FB_25_13			Y1
FB_24_4		H3	K2	GNDE		GNDE	GNDE
VDDE		VDDE	VDDE	FB_25_4	108	T1	W3
FB_24_13	133	J1	K1	FB_25_3			Y2
FB_24_14			L1	VDDE	107	VDDE	VDDE
FB_24_15			L4	FB_25_2	106	P3	Y3
FB_24_16	132	J3	L3	FB_25_1	105	P2	AA1
FB_31_16	131	H2	L2	VDDE		VDDE	VDDE
VDDI		VDDI	M1	FB_26_1	104	M5	AB1

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3512XL Programming Signal Definitions Continued

Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #
FB_26_2		N4	AA2	GNDI	75	GNDI	GNDI
GNDE		GNDE	GNDE	VDDI	74	VDDI	Y12
FB_26_3	103	R2	AB2	FB_16_13			W12
FB_26_4		T2	AA3	FB_16_4		T10	AB13
FB_26_13	102	P4	Y4	FB_16_3	73	P10	AA13
FB_26_14			AB3	GNDE	72	GNDE	GNDE
FB_26_15	101	R3	AA4	FB_16_2	71	R10	Y13
GNDE		GNDE	GNDE	VDDE		VDDE	VDDE
FB_26_16	100	N5	Y5	FB_16_1	70	T11	W13
FB_28_1	99	T3	AA5	FB_14_16	69	N10	AB14
VDDE		VDDE	VDDE	FB_14_15			AA14
FB_28_2	98	M6	AB4	FB_14_14	68	P11	Y14
FB_28_3		R4	W6	FB_14_13	67	M10	W14
FB_28_4	97	P5	AB5	GNDE		GNDE	GNDE
FB_28_13			Y6	FB_14_4	66	R11	AB15
FB_28_14	96	T4	AA6	FB_14_3	65	T12	AA15
FB_28_15	95	N6	AB6	FB_14_2		R12	Y15
GNDE	94	GNDE	GNDE	FB_14_1	64	N11	AB16
FB_28_16	93	R5	W7	VDDE	63	VDDE	VDDE
FB_30_1	92	T6	Y7	FB_12_16	62	T13	AA16
FB_30_2		T5	AA7	FB_12_15	61	P12	Y16
FB_30_3	91	M7	AB7	FB_12_14		R13	W16
FB_30_4			Y8	FB_12_13	60	M11	AB17
FB_30_13	90	R6	AA8	GNDE		GNDE	GNDE
FB_30_14	89	N7	AB8	FB_12_4			AA17
FB_30_15	88	T7	W9	FB_12_3	59	T14	AB18
GNDE		GNDE	GNDE	FB_12_2		N12	AA18
FB_30_16	87	P6	Y9	FB_12_1	58	R14	Y17
FB_32_1	86	R7	AA9	VDDE		VDDE	VDDE
VDDE	85	VDDE	VDDE	FB_10_16	57	P13	W17
FB_32_2		P7	AB9	FB_10_15		T15	AB19
FB_32_3	84	T8	W10	FB_10_14	56	P14	AA19
FB_32_4		N8	Y10	GNDE		GNDE	GNDE
FB_32_13			AA10	FB_10_13	55	T16	Y18
VDDI	83	VDDI	AB10	FB_10_4			AB20
GNDI	82	GNDI	GNDI	VDDE		VDDE	VDDE
FB_32_14	81	R8	AB11	FB_10_3	54	M12	AA20
FB_32_15	80	P8	W11	FB_10_2	53	R15	Y19
FB_32_16	79	T9	AA11	FB_10_1	52	N13	AB21
GNDE		GNDE	GNDE	GNDE		GNDE	GNDE
VDDE		VDDE	VDDE	FB_9_1	51	P16	AA21
FB_16_16	78	P9	Y11	FB_9_2		N14	AB22
FB_16_15	77	R9	AB12	GNDE	50	GNDE	GNDE
FB_16_14	76	N9	AA12	FB_9_3	49	R16	AA22

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3512XL Programming Signal Definitions Continued

Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #
FB_9_4			Y20	GNDE		GNDE	GNDE
FB_9_13	48	M13	Y21	FB_8_13	20	G14	L21
VDDE		VDDE	VDDE	FB_8_4			L20
FB_9_14	47	P15	W20	FB_8_3	19	F16	L19
FB_9_15	46	L12	W21	FB_8_2			K22
FB_9_16	45	N16	Y22	FB_8_1	18	G13	K21
GNDE		GNDE	GNDE	VDDE		VDDE	VDDE
FB_11_1	44	M14	W22	FB_6_16	17	G15	K20
VDDE		VDDE	VDDE	FB_6_15		F14	K19
FB_11_2	43	M16	V20	FB_6_14	16	G12	J22
GNDE		GNDE	GNDE	GNDE		GNDE	GNDE
FB_11_3	42	L13	V21	FB_6_13	15	F15	J21
FB_11_4		N15	U19	GNDE	14	GNDE	GNDE
VDDE	41	VDDE	VDDE	FB_6_4			J20
FB_11_13			V22	FB_6_3	13	E16	J19
FB_11_14	40	M15	U20	FB_6_2			H22
FB_11_15	39	L16	U21	FB_6_1	12	F13	H21
FB_11_16	38	K12	U22	FB_4_16	11	E15	H20
VDDE		VDDE	VDDE	FB_4_15		E14	G22
FB_13_1	37	L15	T19	VDDE		VDDE	VDDE
FB_13_2			T20	FB_4_14	10	D16	G21
FB_13_3	36	K13	T21	FB_4_13			G20
GNDE		GNDE	GNDE	FB_4_4	9	F12	G19
FB_13_4	35	K16	T22	GNDE		GNDE	GNDE
FB_13_13		K14	R20	FB_4_3	8	C16	F22
VDDE		VDDE	VDDE	FB_4_2			F21
FB_13_14	34	K15	R21	FB_4_1	7	E13	F20
FB_13_15	33	L14	R22	FB_2_16	6	D15	E22
GNDE	32	GNDE	GNDE	VDDE	5	VDDE	VDDE
FB_13_16	31	J16	P19	FB_2_15			E21
FB_15_1 / TCK	30	J13	P20	FB_2_14	4	D14	F19
FB_15_2	29	J15	P21	VDDE		VDDE	VDDE
FB_15_3	28	J14	P22	FB_2_13	3	B16	E20
FB_15_4			N19	FB_2_4		C15	D22
GNDI		GNDI	GNDI	FB_2_3	2	A16	D21
VDDI		VDDI	N20	FB_2_2			C22
FB_15_13	27	H16	N21	FB_2_1	1	E12	D20
FB_15_14			N22	VDDE		VDDE	VDDE
FB_15_15	26	H14	M22	FB_1_1	208	C14	C21
FB_15_16	25	H15	M19	FB_1_2		D13	C20
FB_8_16	24	H12	M20	GNDE		GNDE	GNDE
VDDE	23	VDDE	VDDE	FB_1_3	207		B22
FB_8_15	22	H13	M21	FB_1_4	206	A15	B21
FB_8_14	21	G16	L22	FB_1_13			A22

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3512XL Programming Signal Definitions Continued

Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #	Pin Function	PQ208 Pin #	FT256 Pin #	FG324 Pin #
FB_1_14	205	B15	A21	FB_23_16	178	B8	B11
VDDE		VDDE	VDDE	FB_23_15	177	D8	C11
FB_1_15		B14	B20	VDDE		VDDE	VDDE
FB_1_16	204	C13	C19	FB_23_14 / TDI	176	A7	D11
FB_3_1	203	A14	B19	FB_23_13			A10
FB_3_2		E11	A20	FB_23_4		C8	B10
FB_3_3	202		C18	FB_23_3	175	C7	C10
FB_3_4	201	A13	B18	GNDE	174	GNDE	GNDE
GNDE	200	GNDE	GNDE	FB_23_2		B7	D10
FB_3_13		D12	A19	FB_23_1	173	D7	A9
FB_3_14			D17	FB_21_16	172	A6	B9
FB_3_15	199	B13	A18	VDDE		VDDE	VDDE
FB_3_16	198	C12	C17	FB_21_15		E7	C9
FB_5_1	197	A12	B17	FB_21_14	171	B6	D9
FB_5_2			A17	FB_21_13	170	C6	A8
VDDE		VDDE	VDDE	FB_21_4			B8
FB_5_3	196	D11	D16	FB_21_3	169	A5	C8
FB_5_4			C16	FB_21_2		D6	A7
FB_5_13	195	A11	B16	GNDE		GNDE	GNDE
FB_5_14		E10	A16	FB_21_1	168	B5	B7
FB_5_15	194	B12	C15	FB_19_16	167	C5	C7
FB_5_16	193	C11	B15	FB_19_15	166	A4	D7
FB_7_1	192	B11	A15	VDDE	165	VDDE	VDDE
FB_7_2		D10	D14	FB_19_14		E6	A6
VDDE	191	VDDE	VDDE	FB_19_13	164	B4	B6
FB_7_3	190	A10	C14	FB_19_4		D5	C6
GNDE		GNDE	GNDE	VDDE		VDDE	VDDE
FB_7_4 / TDO	189	C10	B14	FB_19_3	163	A3	A5
FB_7_13	188		A14	FB_19_2			D6
FB_7_14			D13	FB_19_1	162	C4	A4
FB_7_15		A9	C13	FB_17_16	161	B3	A3
FB_7_16	187	D9	B13	FB_17_15	160	A1	B5
VDDI	186	VDDI	A13	GNDE		GNDE	GNDE
GNDI	185	GNDI	GNDI	FB_17_14		A2	C5
IN3 / GCLK3	184	B10	A12	FB_17_13	159	D4	B4
IN2 / GCLK2	183	C9	D12	FB_17_4			C4
IN1 / GCLK1	182	A8	B12	FB_17_3	158	C3	B3
IN0 / GCLK0	181	B9	C12	FB_17_2		B2	A2
GNDI	180	GNDI	GNDI	FB_17_1	157	B1	C3
VDDI	179	VDDI	A11				

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

3512XL Programming Signal Definitions Continued

Notes:

FT256

- GNDE and GNDI pads are connected to the following package balls: E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, and L11
- VDDE pads as shown above are connected to the following package balls: F7, F8, F9, F10, G6, G11, H6, H11, J6, J11, K6, K11, L7, L8, L9, and L10.
- VDDI pads are connected to the following package balls: E8, E9, H5, J12, M8, and M9.

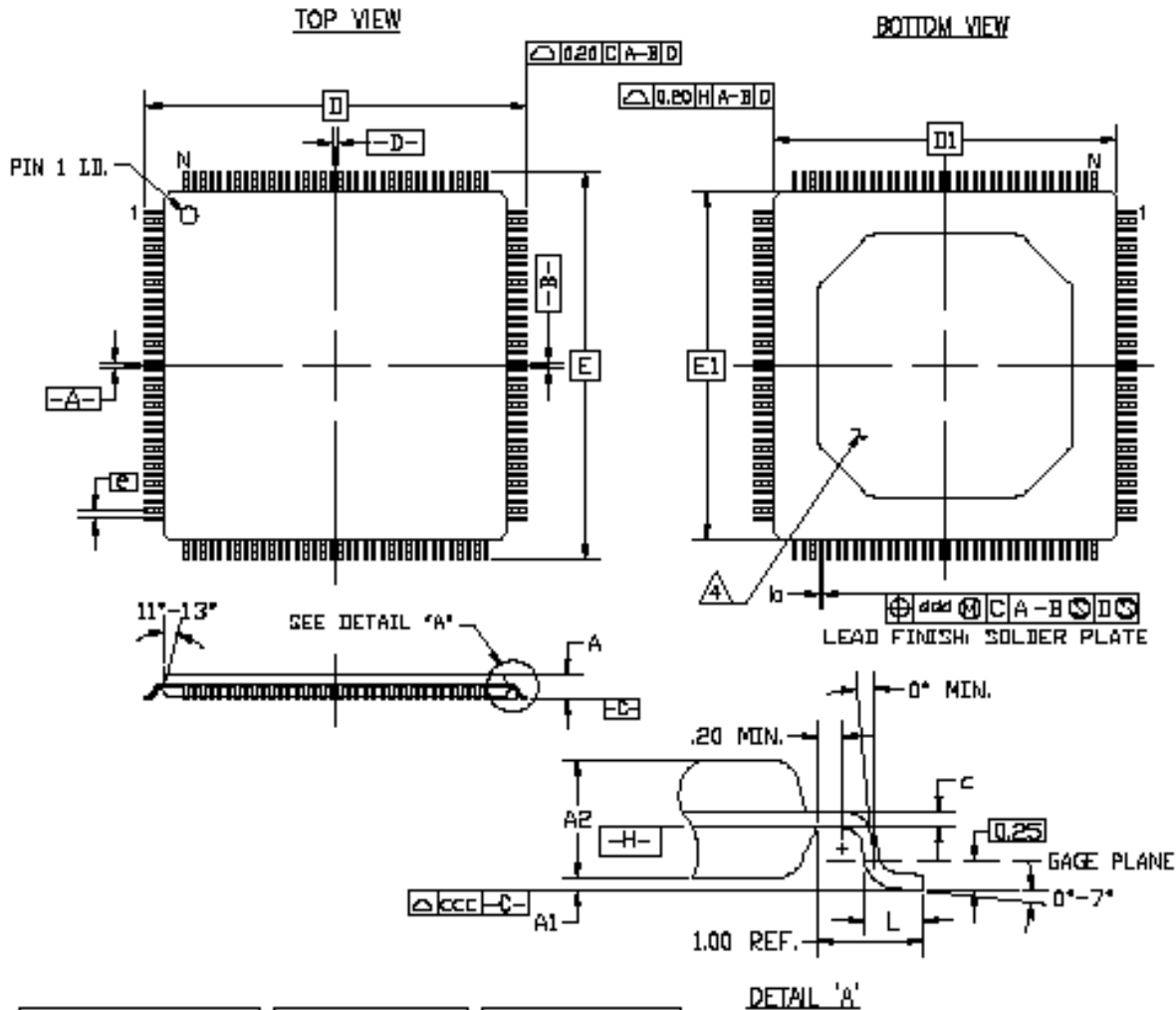
FG324

- GNDE and GNDI pads are connected to the following package balls: D4, D5, D18, D19, E4, E19, J9, J14, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, P9, P14, V9, V14, W4, W5, W18, and W19.
- VDDE pads are connected to the following package balls: D8, D15, H4, H19, J10, J11, J12, J13, K9, K14, L9, L14, M9, M14, N9, N14, P10, P11, P12, P13, R4, R19, W8, AND W15.
- Ball A1 is a package No Connect.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

TQFP/HTQFP Packages - TQ100, TQ144, TQ176, HT100, HT144, HT176



Package	TQ/HT100			TQ/HT144			TQ/HT176		
	MILLIMETERS			MILLIMETERS			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~	~	1.60	~	~	1.60	~	~	1.60
A1	0.05	~	0.15	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45
D/E	16.00 BSC			22.00 BSC			26.00 BSC		
D1/E1	14.00 BSC			20.00 BSC			24.00 BSC		
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
e	0.50 BSC			0.50 BSC			0.50 BSC		
b	0.17	0.22	0.27	0.17	0.22	0.27	0.17	0.22	0.27
c	0.09	~	0.20	0.09	~	0.20	0.09	~	0.20
ccc	~	~	0.08	~	~	0.08	~	~	0.08
ddd	~	~	0.08	~	~	0.08	~	~	0.08
N	100			144			176		
REF.	JEDEC MS-026-BFD			JEDEC MS-026-BFB			JEDEC MS-026-BGA		

NOTE:

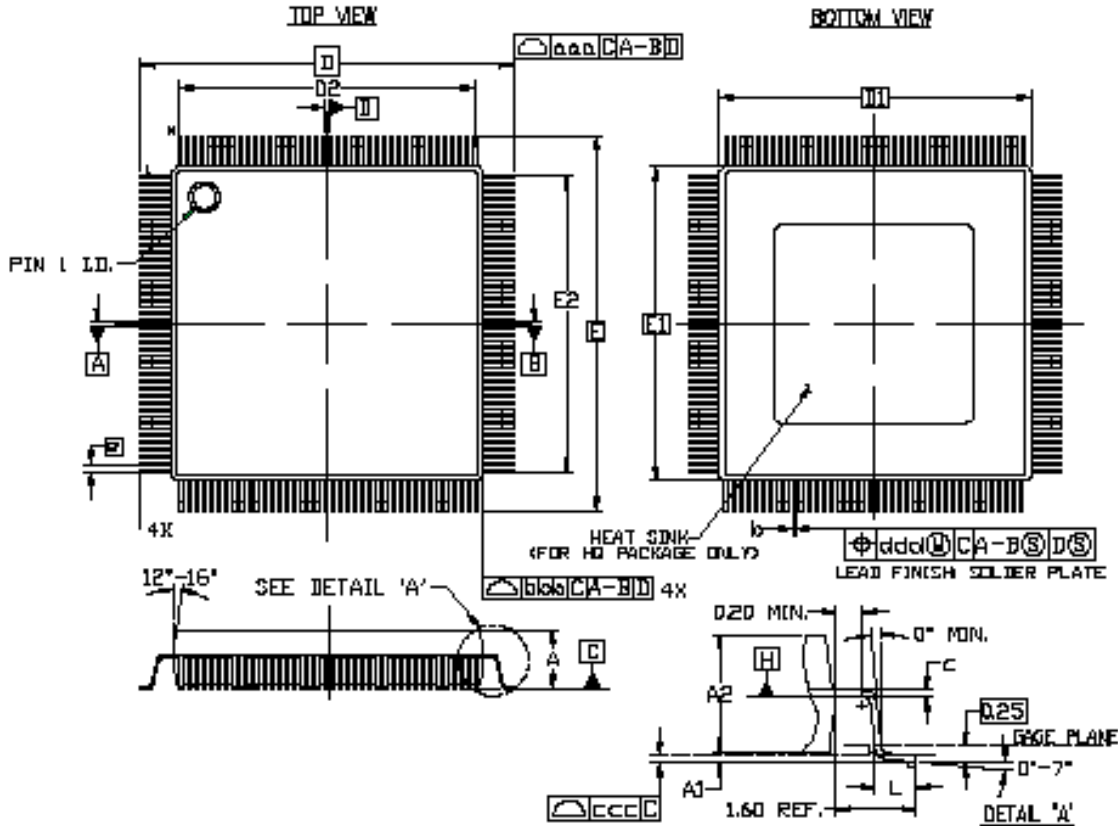
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5-1982
 2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
 3. PACKAGE TOP DIMENSION MAY BE SMALLER THAN THE BOTTOM DIMENSION BY 0.15mm.
- ⚠ THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS 'HT'.

100, 144, 176-PIN TQFP/HEAT SINK TQFP (TQ/HT100, 144, 176)

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

PQ/HQFP Packages - PQ44, PQ160, PQ208, PQ240, HQ160, HQ208, HQ240



	PQ44			PQ/HQ160			PQ/HQ208			PQ/HQ240		
	MILLIMETERS			MILLIMETERS			MILLIMETERS			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~	2.15	2.35	~	3.70	4.10	~	3.70	4.10	~	3.70	4.10
A1	0.05	~	0.25	0.25	0.33	0.50	0.25	0.33	0.50	0.25	0.30	0.50
Ae	1.95	2.00	2.10	3.20	3.40	3.60	3.20	3.40	3.60	3.20	3.40	3.60
D/E	13.20 BSC			31.20 BSC			30.60 BSC			34.60 BSC		
Dy/E1	10.00 BSC			28.00 BSC			28.00 BSC			32.00 BSC		
De/Ee	8.00 REF.			25.35 REF.			25.50 REF.			29.50 REF.		
L	0.73	0.80	1.03	0.73	0.80	1.03	0.50	0.60	0.75	0.50	0.60	0.75
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
b	0.30	~	0.45	0.22	~	0.40	0.17	0.22	0.27	0.17	~	0.27
C	0.13	~	0.23	0.13	~	0.23	0.09	~	0.20	0.09	~	0.20
aaa	~	~	0.25	~	~	0.25	~	~	0.25	~	~	0.25
kkk	~	~	0.20	~	~	0.20	~	~	0.20	~	~	0.20
ccc	~	~	0.10	~	~	0.10	~	~	0.08	~	~	0.08
kkk	~	~	0.20	~	~	0.13	~	~	0.08	~	~	0.08
N	44			160			208			240		
REF.	JEDEC MS-022-AB			JEDEC MS-022-DDI			JEDEC MO-143-FA-L			JEDEC MO-143-GA		

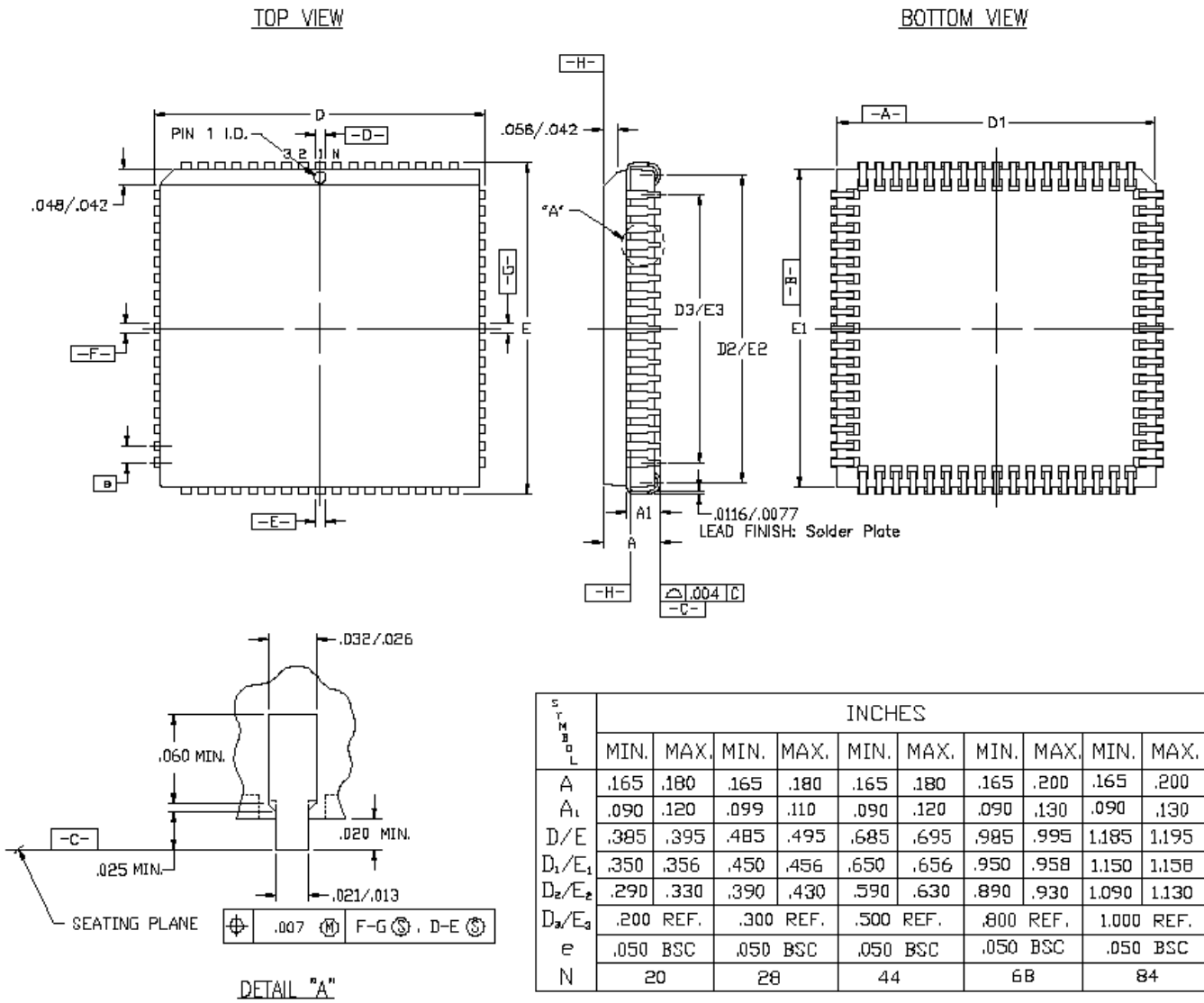
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE WELD PROTRUSION. ALLOWABLE WELD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
3. PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN THE BOTTOM DIMENSIONS BY 0.20mm.
4. THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

44, 160, 208, 240-PIN PQFP/HEAT SINK PQFP (PQ44, PQ/HQ160, 208, 240)

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY



NOTES:

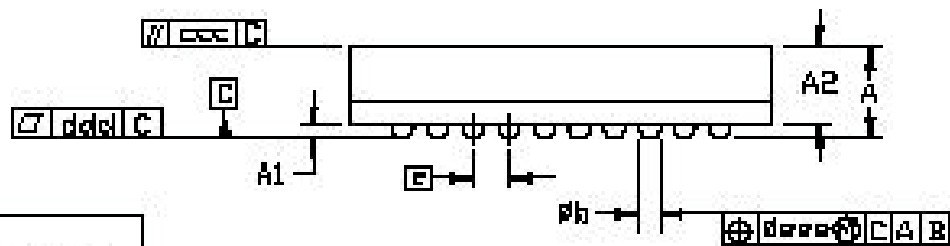
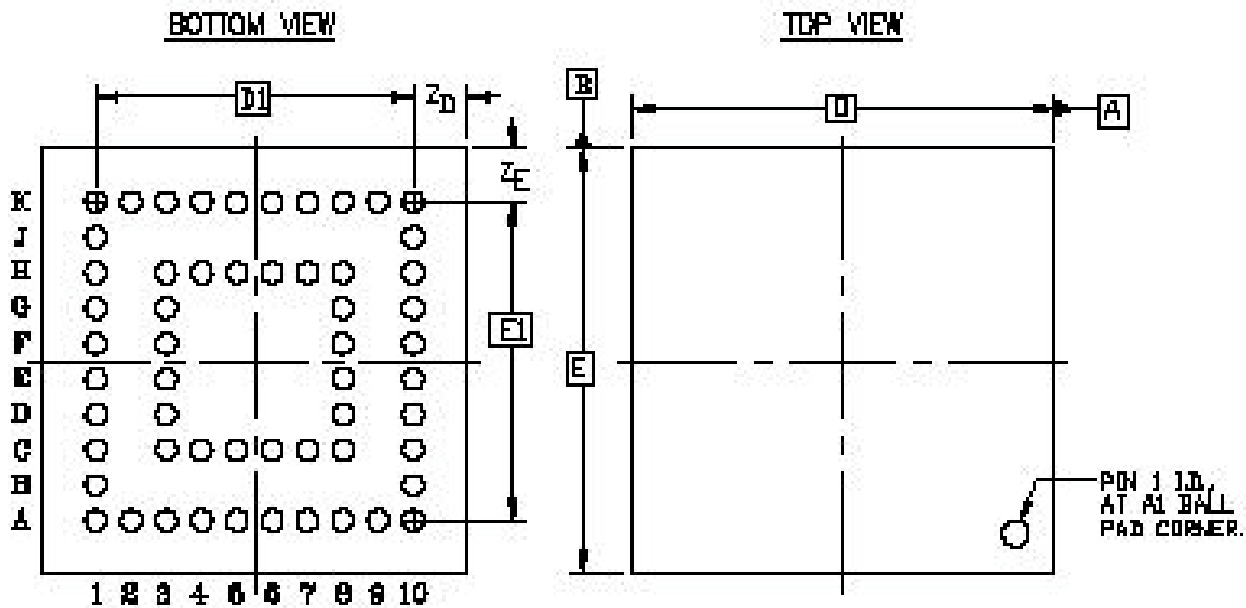
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE.
3. 'N' IS NUMBER OF TERMINALS.
4. CONFORM TO JEDEC MO-047
5. TOP OF PACKAGE MAY BE SMALLER THAN BOTTOM BY .010".

20, 28, 44, 68 and 84-PIN PLCC (PC20 THRU PC84)

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

CP56



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	\varnothing	\varnothing	1.35
A1	0.15	0.20	0.25
D/E	5.90	6.00	6.10
D ₁ /E ₁	4.50 BSC		
a	0.50 BSC		
#b	0.25	0.30	0.35
ccc	\varnothing	\varnothing	0.20
ddd	\varnothing	\varnothing	0.10
eee	\varnothing	\varnothing	0.15
Z _D /Z _E	0.58	0.76	0.93
N	10		

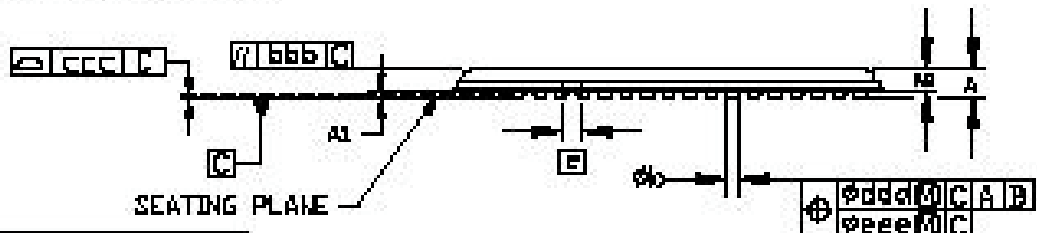
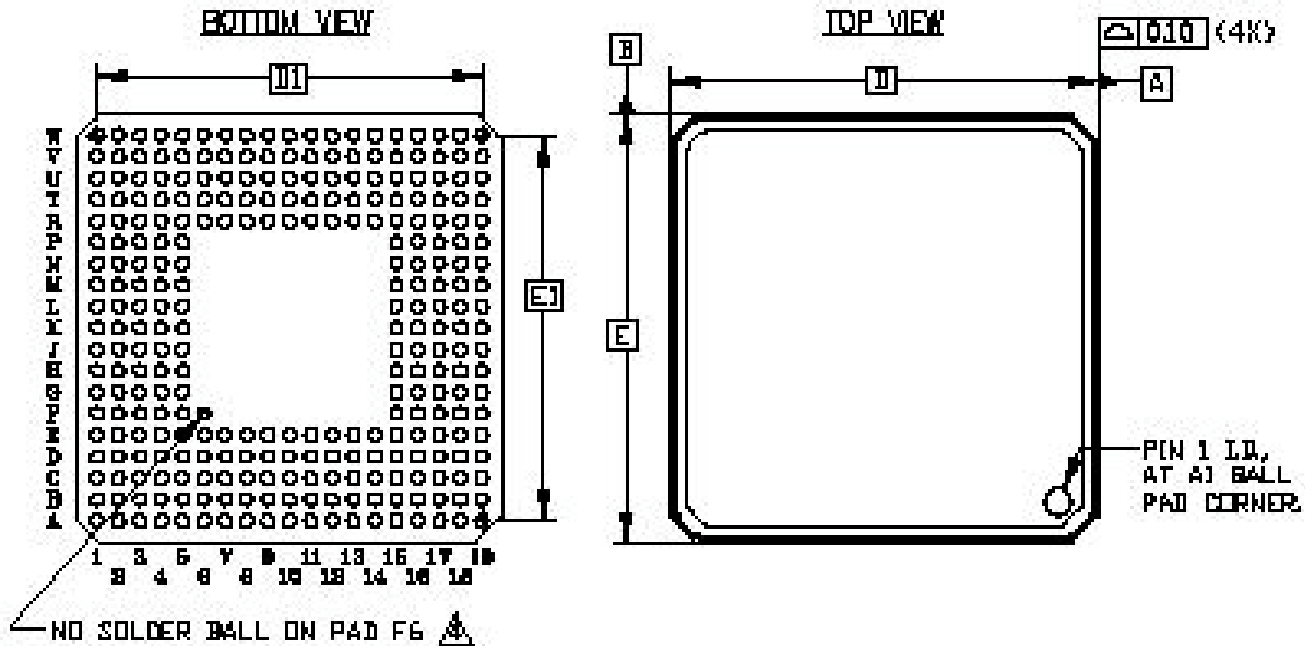
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. SYMBOL "W" IS THE PIN MATRIX SIZE.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

CS280



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	\approx	\approx	1.20
A ₁	0.20	\approx	\approx
A ₂	0.65	\approx	\approx
D/E	16.00 BSC		
D/E ₁	14.40 BSC		
D	0.80 BSC		
H	0.40	0.45	0.50
H ₁	\approx	\approx	0.10
H ₂	\approx	\approx	0.12
H ₃	\approx	\approx	0.13
H ₄	\approx	\approx	0.08
H	19		

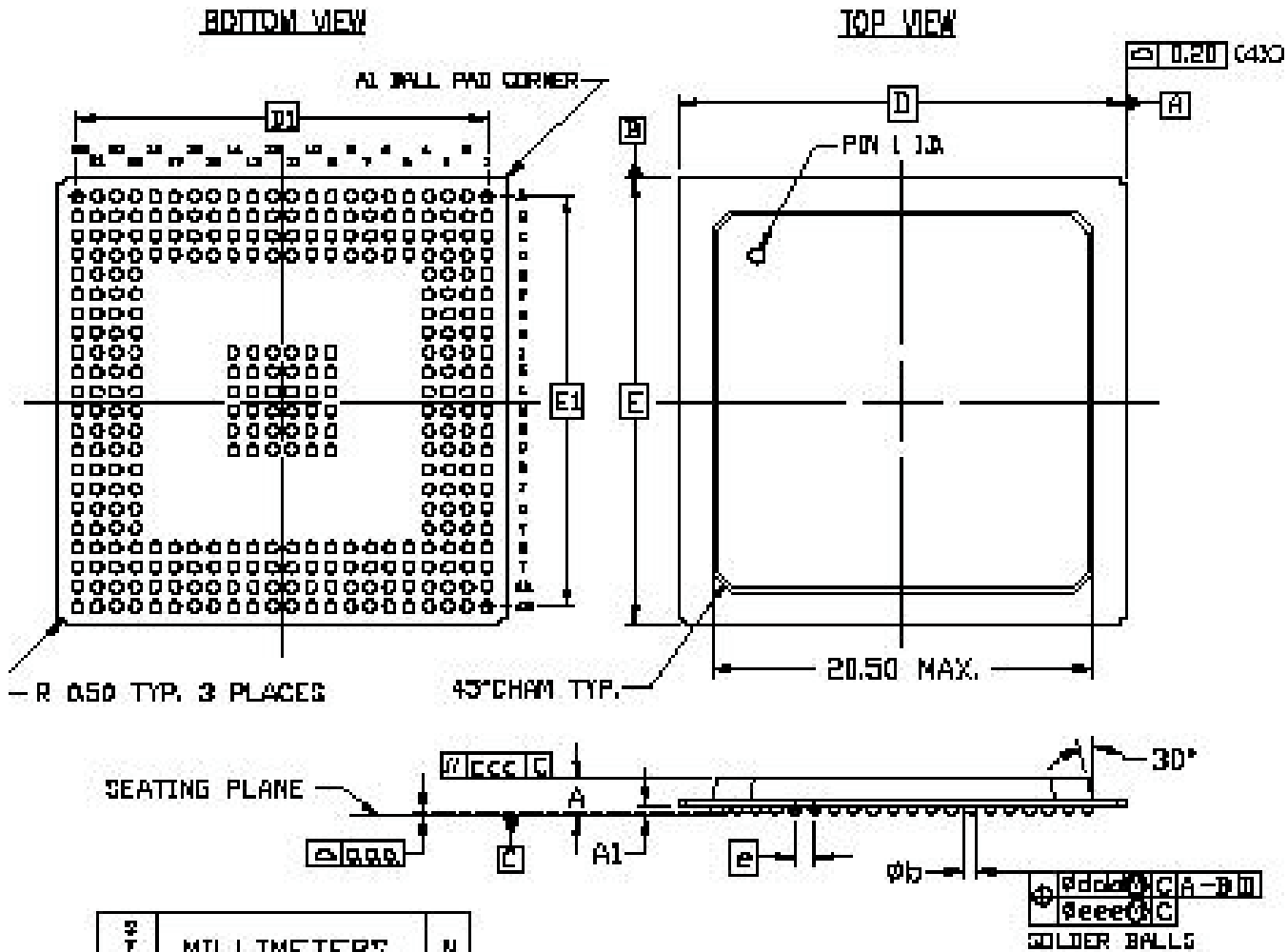
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
 2. SYMBOL "N" IS THE PIN MATRIX SIZE.
 3. CONFORMS TO JEDEC WD-218-BAL-1 (DEPOPULATED).
- \triangle PAD 'F6' IS FOR PAD 'A1' CORNER INDICATION.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

FG324



SYMBOL	MILLIMETERS			NOTES
	MIN.	NOM.	MAX.	
A	<i>typ</i>	<i>typ</i>	2.50	
A1	0.40	0.50	0.60	
D1/E	23.00 BSC			
Dy/E1	21.00 REF			
e	1.00 BSC			
Phi b	0.50	0.60	0.70	
phi b	<i>typ</i>	<i>typ</i>	0.20	
phi c	<i>typ</i>	<i>typ</i>	0.35	
phi d	<i>typ</i>	<i>typ</i>	0.30	
phi e	<i>typ</i>	<i>typ</i>	0.10	
N	22			

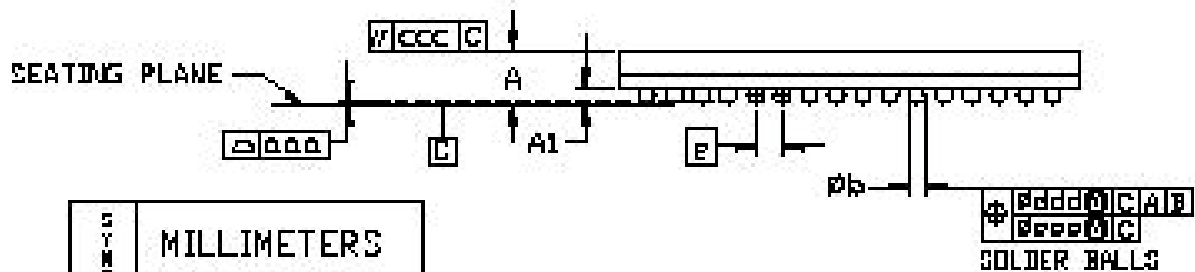
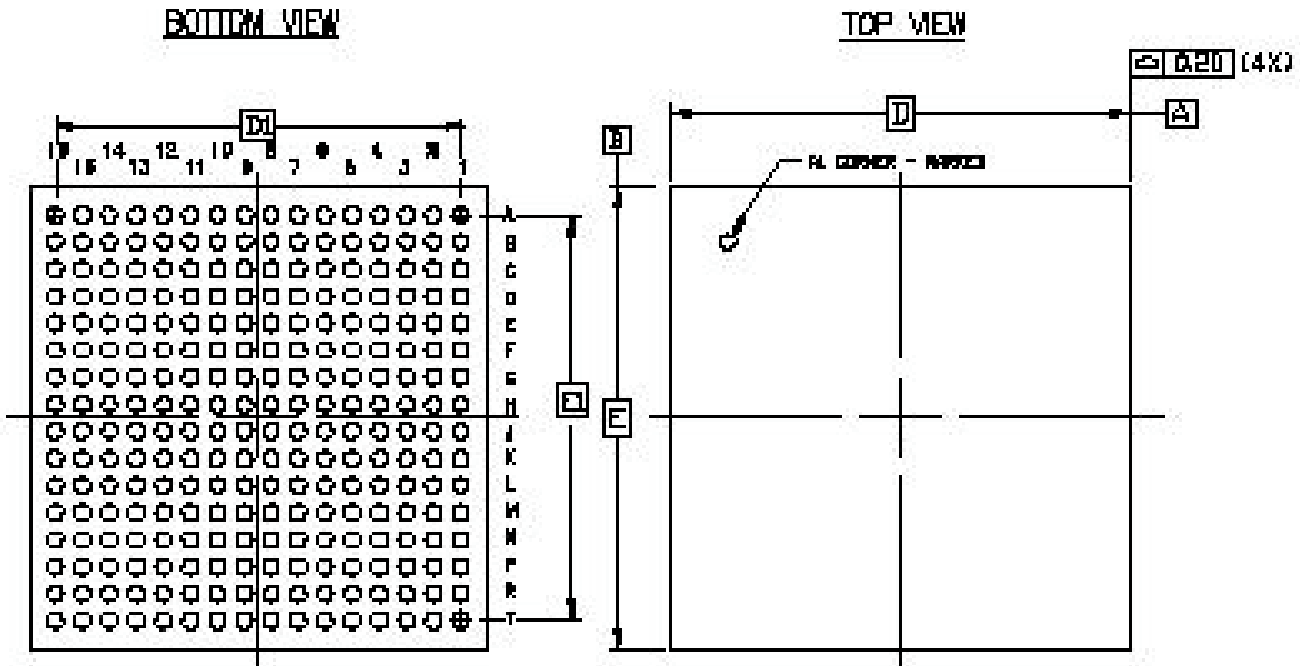
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'W' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC NS-034-AA-1

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

FT256



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	φ	1.40	1.55
A ₁	0.35	0.40	0.50
D ₁ /E	17.00 BSC		
D ₂ /E	15.00 REF		
e	1.00 BSC		
φb	0.40	0.50	0.60
ccc	φ	φ	0.15
ddd	φ	φ	0.15
eee	φ	φ	0.25
fff	φ	φ	0.10
H	16		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL 'W' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAF-1 EXCEPT FOR THE SIZE OF BALL

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

THE ATTACHED FILE CONTAINS ALL ABSOLUTE ADDRESSES A6 TO A0 IN BINARY FOR THE XILINX **XCR3032XL** DEVICE. ADDRESS BITS A5-A0 ARE A GRAY CODE COUNT OF ADDRESSES AND A6 SELECTS UPPER (1) OR LOWER (0) ROW AT THE GIVEN ADDRESS.

DEVICE PACKAGES AND PIN COUNTS

- VQ44
- PC44
- CS48

DEVICE FUSE COUNT

- VQ44 11529 (0-11528)
- PC44 11529 (0-11528)
- CS48 11529 (0-11528)

ERASE ADDRESSES (FOR BULK ERASE)

No address required for bulk erase; erase is performed with ISP command.

Note: When reading an erased device, logical one ('1') is the correct logical value. Logical zero ('0') is the correct logical value for a programmed bit.

OPERATING MODES

Programming and erasing is possible via ISP only.

READ SECURITY ADDRESS

A security feature is available which when programmed, disables access to the information contained in the Non-volatile Eprom array. Any operation reading the user array should not be allowed. A 'read secured' device can still be erased and only then, reprogrammed.

While checking the device for read security before an operation, if the following address is programmed, consider the device read secured. A logical one ('1') if read permitted or a logical zero ('0') if read secured.

Note: The jedec file DOES NOT contain a fuse for this security bit. The security bit must be set with an independent operation to the address shown below.

1. Upper address: 1101110 bit: D0

PORTEN ADDRESS

A feature is available which when programmed, disables the JTAG port and converts the port pins to fully-functional I/Os. This occurs upon subsequent power-cycling or execution of a "reinit" ISP command. See datasheet for discussion of reclaiming JTAG port on a device programmed with port pins as I/Os.

While checking the device for configuration of the JTAG port pins before an operation, if the following address is programmed, consider the device to have the JTAG port disabled and fully-functional I/Os enabled. A logical one ('1') if JTAG port is enabled or a logical zero ('0') if JTAG port is disabled and fully-functional I/Os are enabled.

Note: The jedec file DOES contain a fuse for this porten bit. The porten bit must be set to zero with an independent operation to the address shown below.

1. Upper address: 1101110 bit: D1

MANUFACTURER'S CODE

Available via ISP only

SPD0010 E10

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

PRODUCT AND VERSION CODE

Available via ISP only

SIGNATURE STRING ADDRESSES

The signature string is a user definable code which can be loaded at anytime with appropriate programming equipment. The programmer should allow reading and displaying of the string. These data are erased with ISP erase operation and programmed with the same procedure used for ordinary configuration bits. The user should be able to define the string during a programming session.

These signature string addresses and bit locations are as follows:

1. Lower address: 0101111 bits: D5-9, D66-113
2. Upper address: 1101111 bits: D5-9, D66-113

THE ATTACHED FILE CONTAINS ALL ABSOLUTE ADDRESSES A7 TO A0 IN BINARY FOR THE XILINX **XCR3064XL** DEVICE. ADDRESS BITS A6-A0 ARE A GRAY CODE COUNT OF ADDRESSES AND A7 SELECTS UPPER (1) OR LOWER (0) ROW AT THE GIVEN ADDRESS.

DEVICE PACKAGES AND PIN COUNTS

- VQ44
- VQ100
- PC44
- CP56
- CS48

DEVICE FUSE COUNT

- VQ44 24481 (0-24480)
- VQ100 24481 (0-24480)
- PC44 24481 (0-24480)
- CP56 24481 (0-24480)
- CS48 24481 (0-24480)

ERASE ADDRESSES (FOR BULK ERASE)

No address required for bulk erase; erase is performed with ISP command.

Note: When reading an erased device, logical one ('1') is the correct logical value. Logical zero ('0') is the correct logical value for a programmed bit.

OPERATING MODES

Programming and erasing is possible via ISP only.

READ SECURITY ADDRESS

A security feature is available which when programmed, disables access to the information contained in the Non-volatile Eprom array. Any operation reading the user array should not be allowed. A 'read secured' device can still be erased and only then, reprogrammed.

While checking the device for read security before an operation, if the following address is programmed, consider the device read secured. A logical one ('1') if read permitted or a logical zero ('0') if read secured.

Note: The jedec file DOES NOT contain a fuse for this security bit. The security bit must be set with an independent operation to the address shown below.

- 1) Upper address: 11011100 bit: D0
SPD0010 E10

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

PORTEN ADDRESS

A feature is available which when programmed, disables the JTAG port and converts the port pins to fully-functional I/Os. This occurs upon subsequent power-cycling or execution of a "reinit" ISP command. See datasheet for discussion of reclaiming JTAG port on a device programmed with port pins as I/Os.

While checking the device for configuration of the JTAG port pins before an operation, if the following address is programmed, consider the device to have the JTAG port disabled and fully-functional I/Os enabled. A logical one ('1') if JTAG port is enabled or a logical zero ('0') if JTAG port is disabled and fully-functional I/Os are enabled.

Note: The jedec file DOES contain a fuse for this porten bit. The porten bit must be set to zero with an independent operation to the address shown below.

1. Upper address: 11011100 bit: D1

MANUFACTURER'S CODE

Available via ISP only

PRODUCT AND VERSION CODE

Available via ISP only

SIGNATURE STRING ADDRESSES

The signature string is a user definable code which can be loaded at anytime with appropriate programming equipment. The programmer should allow reading and displaying of the string. These data are erased with ISP erase operation and programmed with the same procedure used for ordinary configuration bits. The user should be able to define the string during a programming session.

These signature string addresses and bit locations are as follows:

1. Lower address: 01011101 bits: D5-9, D75-122
2. Upper address: 11011101 bits: D5-9, D75-122

THE ATTACHED FILE CONTAINS ALL ABSOLUTE ADDRESSES A7 TO A0 IN BINARY FOR THE XILINX **XCR3128XL** DEVICE. ADDRESS BITS A6-A0 ARE A GRAY CODE COUNT OF ADDRESSES AND A7 SELECTS UPPER (1) OR LOWER (0) ROW AT THE GIVEN ADDRESS.

DEVICE PACKAGES AND PIN COUNTS

- VQ100
- TQ144
- CS144

DEVICE FUSE COUNT

- VQ100 52009 (0-52008)
- TQ144 52009 (0-52008)
- CS144 52009 (0-52008)

ERASE ADDRESSES (FOR BULK ERASE)

No address required for bulk erase; erase is performed with ISP command.

Note: When reading an erased device, logical one ('1') is the correct logical value. Logical zero ('0') is the correct logical value for a programmed bit.

OPERATING MODES

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Programming and erasing is possible via ISP only.

READ SECURITY ADDRESS

A security feature is available which when programmed, disables access to the information contained in the Non-volatile Eprom array. Any operation reading the user array should not be allowed. A 'read secured' device can still be erased and only then, reprogrammed. While checking the device for read security before an operation, if the following address is programmed, consider the device read secured. A logical one ('1') if read permitted or a logical zero ('0') if read secured.

Note: The jedec file DOES NOT contain a fuse for this security bit. The security bit must be set with an independent operation to the address shown below.

1. Upper address: 11011100 bit: D0

PORTEN ADDRESS

A feature is available which when programmed, disables the JTAG port and converts the port pins to fully-functional I/Os. This occurs upon subsequent power-cycling or execution of a "reinit" ISP command. See datasheet for discussion of reclaiming JTAG port on a device programmed with port pins as I/Os.

While checking the device for configuration of the JTAG port pins before an operation, if the following address is programmed, consider the device to have the JTAG port disabled and fully-functional I/Os enabled. A logical one ('1') if JTAG port is enabled or a logical zero ('0') if JTAG port is disabled and fully-functional I/Os are enabled.

Note: The jedec file DOES contain a fuse for this porten bit. The porten bit must be set to zero with an independent operation to the address shown below.

1. Upper address: 11011100 bit: D1

MANUFACTURER'S CODE

Available via ISP only

PRODUCT AND VERSION CODE

Available via ISP only

SIGNATURE STRING ADDRESSES

The signature string is a user definable code which can be loaded at anytime with appropriate programming equipment. The programmer should allow reading and displaying of the string. These data are erased with ISP erase operation and programmed with the same procedure used for ordinary configuration bits. The user should be able to define the string during a programming session.

These signature string addresses and bit locations are as follows:

1. Lower address: 01011101 bits: D5-19, D47-73, D170-265
2. Upper address: 11011101 bits: D5-19, D47-73, D170-265

THE ATTACHED FILE CONTAINS ALL ABSOLUTE ADDRESSES A8 TO A0 IN BINARY FOR THE XILINX **XCR3256XL** DEVICE. ADDRESS BITS A7-A0 ARE A GRAY CODE COUNT OF ADDRESSES AND A8 SELECTS UPPER (1) OR LOWER (0) ROW AT THE GIVEN ADDRESS.

DEVICE PACKAGES AND PIN COUNTS

- TQ144
- PQ208
- CS280
- FT256

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

DEVICE FUSE COUNT

- TQ144 115868
- PQ208 115868
- CS280 115868
- FT256 115868

ERASE ADDRESSES (FOR BULK ERASE)

No address required for bulk erase; erase is performed with ISP command.

Note: When reading an erased device, logical one ('1') is the correct logical value. Logical zero ('0') is the correct logical value for a programmed bit.

OPERATING MODES

Programming and erasing is possible via ISP only.

READ SECURITY ADDRESS

A security feature is available which when programmed, disables access to the information contained in the Non-volatile Eprom array. Any operation reading the user array should not be allowed. A 'read secured' device can still be erased and only then, reprogrammed.

While checking the device for read security before an operation, if the following address is programmed, consider the device read secured. A logical one ('1') if read permitted or a logical zero ('0') if read secured.

Note: The jedec file DOES NOT contain a fuse for this security bit. The security bit must be set with an independent operation to the address shown below.

1. Upper address: 110111000 bit: D0

PORTEN ADDRESS

A feature is available which when programmed, disables the JTAG port and converts the port pins to fully-functional I/Os. This occurs upon subsequent power-cycling or execution of a "reinit" ISP command. See datasheet for discussion of reclaiming JTAG port on a device programmed with port pins as I/Os.

While checking the device for configuration of the JTAG port pins before an operation, if the following address is programmed, consider the device to have the JTAG port disabled and fully-functional I/Os enabled. A logical one ('1') if JTAG port is enabled or a logical zero ('0') if JTAG port is disabled and fully-functional I/Os are enabled.

Note: The jedec file DOES contain a fuse for this porten bit. The porten bit must be set to zero with an independent operation to the address shown below.

1. Upper address: 110111000 bit: D1

MANUFACTURER'S CODE

Available via ISP only

PRODUCT AND VERSION CODE

Available via ISP only

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

SIGNATURE STRING ADDRESSES

The signature string is a user definable code which can be loaded at anytime with appropriate programming equipment. The programmer should allow reading and displaying of the string. These data are erased with ISP erase operation and programmed with the same procedure used for ordinary configuration bits. The user should be able to define the string during a programming session.

These signature string addresses and bit locations are as follows:

1. Lower address: 010111001 bits: D5-19, D66-111, D208-D303
2. Upper address: 110111001 bits: D5-19, D66-111, D208-D303

THE ATTACHED FILE CONTAINS ALL ABSOLUTE ADDRESSES A8 TO A0 IN BINARY FOR THE XILINX **XCR3384XL** DEVICE. ADDRESS BITS A7-A0 ARE A GRAY CODE COUNT OF ADDRESSES AND A8 SELECTS UPPER (1) OR LOWER (0) ROW AT THE GIVEN ADDRESS.

DEVICE PACKAGES AND PIN COUNTS

- TQ144
- PQ208
- FT256
- FG324

DEVICE FUSE COUNT

- TQ144 189968
- PQ208 189968
- FT256 189968
- FG324 189968

ERASE ADDRESSES (FOR BULK ERASE)

No address required for bulk erase; erase is performed with ISP command.

Note: When reading an erased device, logical one ('1') is the correct logical value. Logical zero ('0') is the correct logical value for a programmed bit.

OPERATING MODES

Programming and erasing is possible via ISP only.

READ SECURITY ADDRESS

A security feature is available which when programmed, disables access to the information contained in the Non-volatile Eprom array. Any operation reading the user array should not be allowed. A 'read secured' device can still be erased and only then, reprogrammed.

While checking the device for read security before an operation, if the following address is programmed, consider the device read secured. A logical one ('1') if read permitted or a logical zero ('0') if read secured.

Note: The jedec file DOES NOT contain a fuse for this security bit. The security bit must be set with an independent operation to the address shown below.

1. Upper address: 110111000 bit: D0

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

PORTEN ADDRESS

A feature is available which when programmed, disables the JTAG port and converts the port pins to fully-functional I/Os. This occurs upon subsequent power-cycling or execution of a "reinit" ISP command. See datasheet for discussion of reclaiming JTAG port on a device programmed with port pins as I/Os.

While checking the device for configuration of the JTAG port pins before an operation, if the following address is programmed, consider the device to have the JTAG port disabled and fully-functional I/Os enabled. A logical one ('1') if JTAG port is enabled or a logical zero ('0') if JTAG port is disabled and fully-functional I/Os are enabled.

Note: The jedec file DOES contain a fuse for this porten bit. The porten bit must be set to zero with an independent operation to the address shown below.

1. Upper address: 110111000 bit: D1

MANUFACTURER'S CODE

Available via ISP only

PRODUCT AND VERSION CODE

Available via ISP only

SIGNATURE STRING ADDRESSES

The signature string is a user definable code which can be loaded at anytime with appropriate programming equipment. The programmer should allow reading and displaying of the string. These data are erased with ISP erase operation and programmed with the same procedure used for ordinary configuration bits. The user should be able to define the string during a programming session.

These signature string addresses and bit locations are as follows:

1. Lower address: 010111001 bits: D15-29, D156-218, D363-D506
2. Upper address: 110111001 bits: D15-29, D156-218, D363-D506

THE ATTACHED FILE CONTAINS ALL ABSOLUTE ADDRESSES A8 TO A0 IN BINARY FOR THE XILINX **XCR3512XL** DEVICE. ADDRESS BITS A7-A0 ARE A GRAY CODE COUNT OF ADDRESSES AND A8 SELECTS UPPER (1) OR LOWER (0) ROW AT THE GIVEN ADDRESS.

DEVICE PACKAGES AND PIN COUNTS

- PQ208
- FT256
- FG324

DEVICE FUSE COUNT

- PQ208 278720
- FT256 278720
- FG324 278720

ERASE ADDRESSES (FOR BULK ERASE)

No address required for bulk erase; erase is performed with ISP command.

Note: When reading an erased device, logical one ('1') is the correct logical value. Logical zero ('0') is the correct logical value for a programmed bit.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

OPERATING MODES

Programming and erasing is possible via ISP only.

READ SECURITY ADDRESS

A security feature is available which when programmed, disables access to the information contained in the Non-volatile Eprom array. Any operation reading the user array should not be allowed. A 'read secured' device can still be erased and only then, reprogrammed.

While checking the device for read security before an operation, if the following address is programmed, consider the device read secured. A logical one ('1') if read permitted or a logical zero ('0') if read secured.

Note: The jedec file DOES NOT contain a fuse for this security bit. The security bit must be set with an independent operation to the address shown below.

1. Upper address: 110111000 bit: D0

PORTEN ADDRESS

A feature is available which when programmed, disables the JTAG port and converts the port pins to fully-functional I/Os. This occurs upon subsequent power-cycling or execution of a "reinit" ISP command. See datasheet for discussion of reclaiming JTAG port on a device programmed with port pins as I/Os.

While checking the device for configuration of the JTAG port pins before an operation, if the following address is programmed, consider the device to have the JTAG port disabled and fully-functional I/Os enabled. A logical one ('1') if JTAG port is enabled or a logical zero ('0') if JTAG port is disabled and fully-functional I/Os are enabled.

Note: The jedec file DOES contain a fuse for this porten bit. The porten bit must be set to zero with an independent operation to the address shown below.

1. Upper address: 110111000 bit: D1

MANUFACTURER'S CODE

Available via ISP only

PRODUCT AND VERSION CODE

Available via ISP only

SIGNATURE STRING ADDRESSES

The signature string is a user definable code which can be loaded at anytime with appropriate programming equipment. The programmer should allow reading and displaying of the string. These data are erased with ISP erase operation and programmed with the same procedure used for ordinary configuration bits. The user should be able to define the string during a programming session.

These signature string addresses and bit locations are as follows:

1. Lower address: 010111001 bits: D5-19, D108-185, D282-377, D383-397, D481-563, D660-755
2. Upper address: 110111001 bits: D5-19, D108-185, D282-377, D383-397, D481-563, D660-755

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

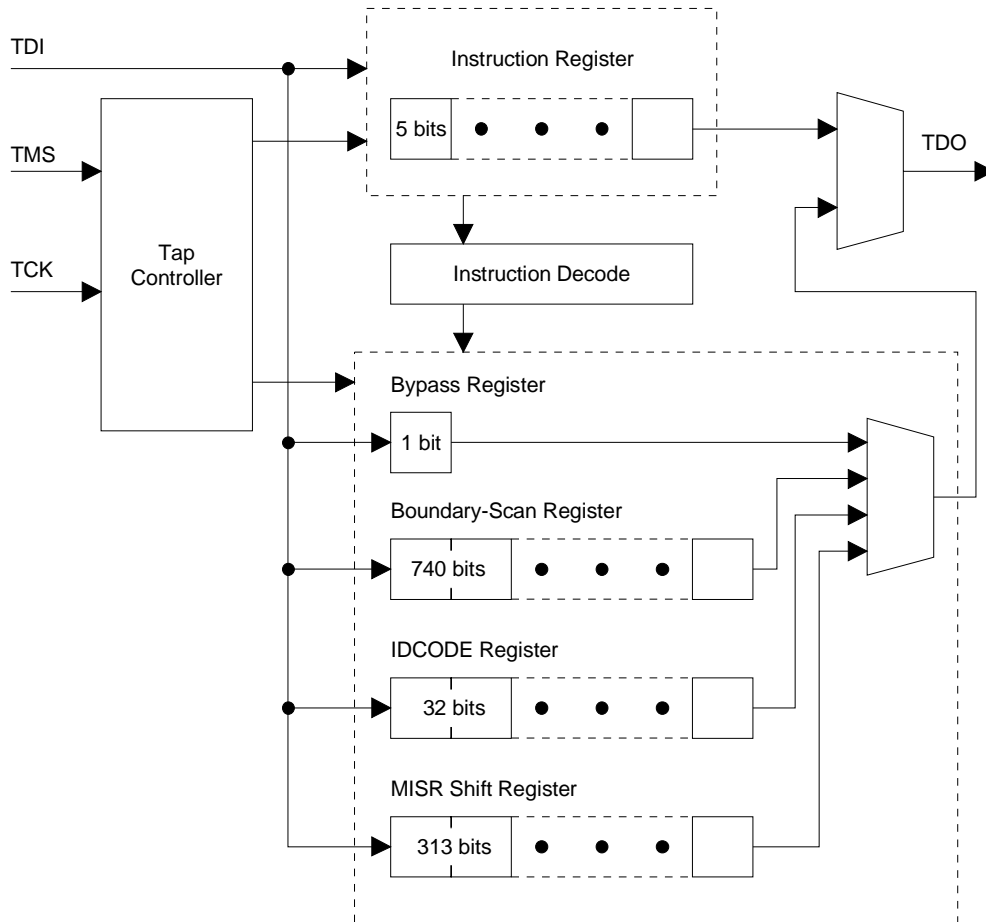
CoolRunner XPLA3 FAMILY

<i>Code</i>	<i>Instruction</i>	<i>Register used</i>
00000	Extest	Boundary-Scan
00001	Idcode	Ident
00010	Sample	Boundary-Scan
00011	Intest	Boundary-Scan
00100	Stctest	Boundary-Scan
00101	High-Z	Bypass
00110	Clamp	Bypass
00111	Write	ISP Shift
01000	EOTF	ISP Shift
01001	Enable	ISP Shift
01010	Erase	ISP Shift
01011	Program	ISP Shift
01100	Verify	ISP Shift
01101	Init	Bypass
01110	Read	ISP Shift
10000	Disable	ISP Shift
10001	Testmode	Bypass
11111	Bypass	Bypass

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

J-TAG Registers – Example XCR3256XL



XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

JTAG Register Description

Register	# of bits	Register Description										
Instruction Register	5	The Instruction Register is a shift-register-based design which allows an instruction to be shifted into a device. The instruction shifted into the register is latched at the completion of the shifting process. The instruction is used to select the BST or ISP operation and/or the data register to be accessed. The parallel output from the Instruction Register is latched to ensure that the BST and ISP logic is protected from the transient data patterns that will occur in its shift-register stages as new instruction data is entered.										
Bypass Register	1	The Bypass Register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of a component when no test or program operation of that component is required. This allows more rapid movement of test/program data to and from other components on a circuit pack that are required to perform test/program operations.										
Boundary Scan Register	740	The Boundary-Scan Register allows testing of circuitry external to the CPLD and also permits the system signals flowing into and out of the CPLD logic to be sampled and examined without causing interference with the normal operation of the CPLD logic. The Boundary-Scan Register is a long shift register composed of all the Boundary-Scan cells at the pins of the device.										
IDCODE Register	32	This register must consist of a 32 bit shift-register, parallel-in and serial out. The register contains the following information: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit(s)</th> <th>Usage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1 - pre-defined</td> </tr> <tr> <td>1-11</td> <td>Manufacturing Identity</td> </tr> <tr> <td>12-27</td> <td>Part Number</td> </tr> <tr> <td>28-31</td> <td>Version</td> </tr> </tbody> </table>	Bit(s)	Usage	0	1 - pre-defined	1-11	Manufacturing Identity	12-27	Part Number	28-31	Version
Bit(s)	Usage											
0	1 - pre-defined											
1-11	Manufacturing Identity											
12-27	Part Number											
28-31	Version											
ISP Shift Register	9 address bits 304 data bits 313 bits total	Used to address the EEPROM row and contains the data that is being written into or read from the EEPROM array.										

JTAG Pin Description

Pins	Name	Description
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively. TCK is also used to clock the TAP Controller state machine.
TMS	Test Mode Select	Test mode select pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Supported Low Level JTAG Boundary-Scan Commands

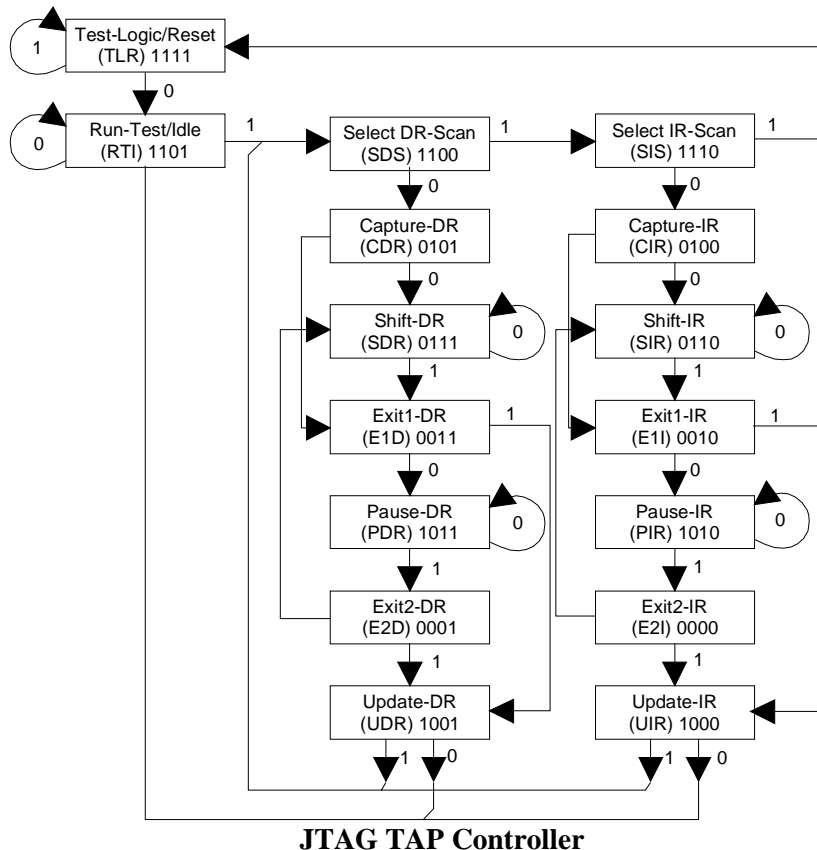
Instruction (Instr. Code) Register Used	Description
BYPASS (11111) <i>Bypass Register</i>	Required. Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation without affecting the operation of the IC.
EXTEST (00000) <i>Boundary-Scan Register</i>	Required. Puts the IC into external mode. Forces data externally from the boundary scan outputs and receives data externally to the boundary scan inputs.
IDCODE (00001) <i>Boundary-Scan Register</i>	Optional. Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a circuit pack. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
Sample /Preload (00010) <i>Boundary-Scan Register</i>	Required. Allows IC to remain in normal mode and selects the boundary scan register to be connected between TDI and TDO. Allows sampling data entering and leaving the device. It allows preload data into the boundary scan register before executing the EXTEST instruction.
INTEST (00011) <i>Boundary-Scan Register</i>	Optional. Puts the IC in internal mode and selects the boundary scan register to be connected between TDI and TDO. It allows to drive data into the CORE logic of the IC from the boundary scan inputs and to receive CORE logic output data into the boundary scan outputs.
STCTEST (00100) <i>Boundary-Scan Register</i>	Optional. The STCTEST instruction is used by the Philips design community to check the integrity of the JTAG Boundary-Scan structure. This command will be for internal Philips use only and will not be advertised to customers.
HIGHZ (00101) <i>Bypass Register</i>	Optional. The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HIGHZ instruction also forces the Bypass Register between TDI and TDO.
CLAMP (00110) <i>Bypass Register</i>	Optional. Forces data externally from the boundary scan outputs and selects the one bit bypass register to be connected between TDI and TDO. The data into the boundary scan register can be preloaded using sample/preload.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Supported Low Level ISP Commands

WRITE (00111) <i>ISP Shift Register</i>	To configure a specified address of the SRAM. Selects ISP register to be connected between TDI and TDO. (PRIVATE INSTRUCTION)
EOTF (01000) <i>ISP Shift Register</i>	Enters ISP mode in on-the-fly mode, which allows the IC to be in normal mode while the IC EEPROM is re-programmed. (PRIVATE INSTRUCTION)
ENABLE (01001) <i>ISP Shift Register</i>	Enters normal ISP mode, puts IC in disable mode.
ERASE (01010) <i>ISP Shift Register</i>	Bulk erases the IC EEPROM.
VERIFY (01100) <i>ISP Shift Register</i>	Reads the contents of a specified address of the IC EEPROM.
INIT (01101) <i>Bypass Register</i>	Starts initialization process, moves data from the EEPROM to SRAM.
READ (01110) <i>ISP Shift Register</i>	Reads a specific address from the SRAM. If security bit is programmed, SRAM access is blocked. (PRIVATE INSTRUCTION)
DISABLE (10000) <i>ISP Shift Register</i>	Leaves the ISP mode.
TESTMODE (10001) <i>Bypass Register</i>	Puts the IC into test mode. (PRIVATE INSTRUCTION)
PROGRAM (01011)	Program the data in the ISP shift register into the addressed EEPROM row.
ISP	



3.1.2 JTAG TAP Controller

The TAP Controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by the 1149.1 IEEE Standard. This TAP Controller is implemented in the Philips CPLDs.

Test-Logic/Reset: The BST and ISP logic is disabled so that normal operation of the on-chip system logic (i.e. in response to stimuli received through the system pins only) can continue unimpeded. This is achieved by initializing the instruction register to contain the IDCODE instruction. No matter what the original state of the controller, it will enter *Test-Logic-Reset* when TMS is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. Note that the TAP controller will be forced to the *Test-Logic-Reset* controller state at power-up.

Run-Test/Idle: All of the instructions supported by Philips CPLDs do not cause functions to execute in the *Run-Test/Idle* controller state. Thus, all BST and ISP data registers selected by the current instruction shall retain their previous state (i.e. Idle). The instruction does not change while the TAP controller is in this state.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Select-DR-Scan: This is a temporary controller state in which all BST and ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

Select-IR-Scan: This is a temporary controller state in which all BST and ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

Capture-DR: In this controller state, data may be parallel loaded into the BST data registers selected by the current instruction on the rising edge of TCK. If a BST data register selected by the current instruction does not have parallel input, or if capturing is not required for the selected test, then the register retains its previous state. The instruction does not change while the TAP controller is in this state.

Shift-DR: In this controller state, the BST or ISP data register connected between TDI and TDO as a result of the current instruction shifts data one stage towards its serial output on each rising edge of TCK. BST or ISP data registers that are selected by the current instruction, but are not placed in the serial path, retain their previous state. The instruction does not change while the TAP controller is in this state.

Exit1-DR: This is a temporary state. All BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

Pause-DR: This controller state allows shifting of the BST or ISP data register in the serial path between TDI and TDO to be temporarily halted. All BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

Exit2-DR: This is a temporary state. All BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

Update-DR: Some BST data registers may be provided with a latched parallel output to prevent changes at the parallel output while data is shifted in the associated shift-register path in response to certain instructions (e.g. EXTEST). Data is latched onto the parallel output of these BST data registers from the shift-register path on the falling edge of TCK in the *Update-DR* controller state. The data held at the latched parallel outputs should not change. The instruction does not change while the TAP controller is in this state.

Capture-IR: In this controller state, the shift-register contained in the instruction register loads a pattern of fixed logic values on the rising edge of TCK. In addition, design-specific data may be loaded into shift-register stages that are not required to be set to fixed values. BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

Shift-IR: In this controller state, the shift-register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. BST or ISP data registers that are selected by the current instruction, but are not placed in the serial path, retain their previous state. The instruction does not change while the TAP controller is in this state.

Exit1-IR: This is a temporary state. BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state and the instruction register retains its state.

Pause-IR: This controller state allows shifting of the instruction register to be temporarily halted. BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state and the instruction register retains its state.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Exit2-IR: This is a temporary state. BST or ISP data registers selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state and the instruction register retains its state.

Update-IR: The instruction shifted into the instruction register is latched onto the parallel output from the shift-register path on the falling edge of TCK in the *Update-IR* controller state. Once the new instruction has been latched, it becomes the current instruction. BST or ISP data registers selected by the current instruction retain their previous state.

Support the following High Level ISP and JTAG Boundary-Scan Instructions:

ISP Commands (ENABLE):

Bulk_Erase	Erase the EEPROM array.
Blank_Check	Verify that the EEPROM array has been erased.
Program	Program the EEPROM array.
Verify	Verify the EEPROM array.
Pr_Security	Program the Security Bit.
Rd_Security	Read the Security Bit.
Pr_UES	Program the UES.
Usercode	Read the UES.
Program_Verify	Simultaneously Program/Verify the EEPROM.

JTAG Commands:

Bypass	Connect TDO to TDO.
Idcode	Read the devices ID code.
Precondition Outputs	Allows the user to specify outputs

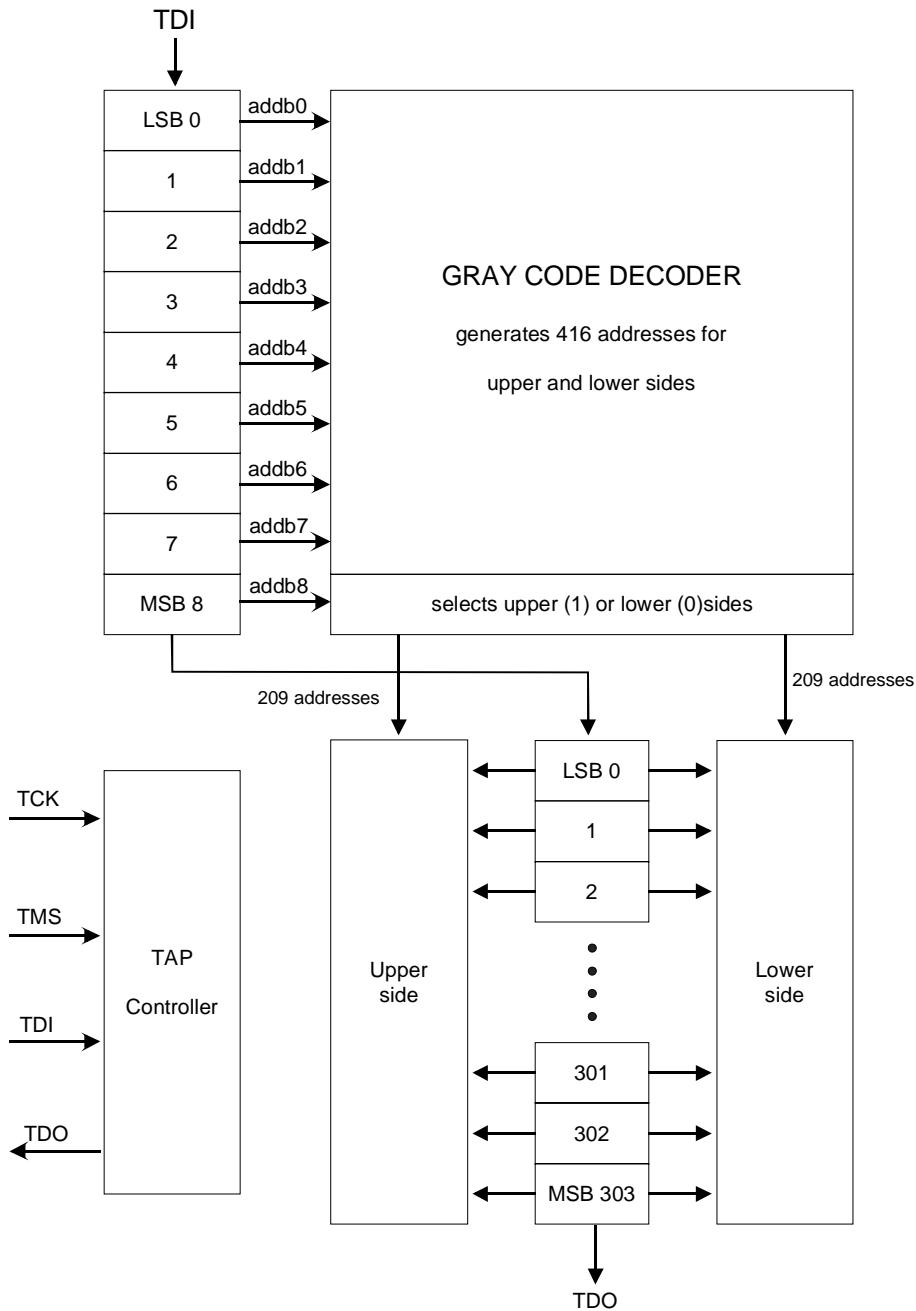
High Level ISP and JTAG Boundary-Scan Instructions:

- ISP Commands (ENABLE):
 - Bulk_Erase - Erase the EEPROM array.
 - Blank_Check - Verify that the EEPROM array has been erased.
 - Program - Program the EEPROM array.
 - Verify - Verify the EEPROM array.
 - Pr_Security - Program the Security Bit.
 - Rd_Security - Read the Security Bit.
 - Pr_UES - Program the UES.
 - Usercode - Read the UES.
 - Program_Verify - Simultaneously Program/Verify the EEPROM.
- JTAG Commands:
 - Bypass - Connect TDI to TDO.
 - Idcode - Read the devices ID code.
 - Precondition Outputs - User specified outputs

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

XPLA3 256 MACROCELL SHIFT REGISTER ARCHITECTURE



XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

XPLA3 256 MACROCELL DEVICE PROGRAMMING EXAMPLE

Bulk_Erase

The Bulk_Erase command erases the entire EEPROM array.

Bulk_Erase Command Flow

Command	Sequence
Bulk_Erase	<ol style="list-style-type: none"> 1. Ensure device is in test-logic/reset state 2. shift in the ENABLE instruction 3. shift in the ERASE instruction 4. pause to allow voltages to settle 5. execute the instruction (erase the contents of the EEPROM array) 6. pause to allow voltages to discharge 7. shift in the INIT instruction 8. execute the instruction (activate the contents of the EEPROM array) 9. shift in the DISABLE instruction 10. execute the instruction (activate the contents of the EEPROM array)

Bulk_Erase Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
Loop0	TMS = 1, TCK = ↑	Test-Logic/Reset	Ensure device in Test-Logic/Reset State	Loop 5 times
1	TMS = 0, TCK = ↑	Run-Test/Idle		
2	TMS = 1, TCK = ↑	Select DR-Scan		
3	TMS = 1, TCK = ↑	Select IR-Scan		
4	TMS = 0, TCK = ↑	Capture-IR		
5	TMS = 0, TCK = ↑	Shift-IR		
Loop1	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1001 (Enable)
6	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Enable MSB)
7	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register ; Set enable flip-flop	
8	TMS = 1, TCK = ↑	Select DR-Scan		
9	TMS = 1, TCK = ↑	Select IR-Scan		
10	TMS = 0, TCK = ↑	Capture-IR		
11	TMS = 0, TCK = ↑	Shift-IR		
Loop2	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bit (0-3)	TDI = 0101 (Erase)
12	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Erase MSB)
13	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
14	TMS = 1, TCK = ↑	Select DR-Scan		
15	TMS = 0, TCK = ↑	Capture-DR		
16	TMS = 1, TCK = ↑	Exit1-DR		
17	TMS = 0, TCK = ↑	Pause-DR		Loop 20 us
18	TMS = 1, TCK = ↑	Exit2-DR		
19	TMS = 1, TCK = ↑	Update-DR		
20	TMS = 0, TCK = ↑	Run-Test/Idle	Execute: Erase the device	Loop for 100 ms
21	TMS = 1, TCK = ↑	Select DR-Scan		
22	TMS = 0, TCK = ↑	Capture-DR		
23	TMS = 1, TCK = ↑	Exit1-DR		
Loop 3	TMS = 0, TCK = ↑	Pause-DR	Discharge hgh voltages	Loop 5ms
24	TMS = 1, TCK = ↑	Exit2-DR		

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

25	TMS = 1, TCK = ↑	Update-DR		
26	TMS = 1, TCK = ↑	Select DR-Scan		

Bulk Erase Detailed Algorithm Continued

27	TMS = 1, TCK = ↑	Select IR-Scan		
28	TMS = 0, TCK = ↑	Capture-IR		
29	TMS = 0, TCK = ↑	Shift-IR		
Loop4	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1011 (Init)
30	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Init MSB)
31	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
32	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	Loop for 200us
33	TMS = 1, TCK = ↑	Select DR-Scan		
34	TMS = 1, TCK = ↑	Select IR-Scan		
35	TMS = 0, TCK = ↑	Capture-IR		
36	TMS = 0, TCK = ↑	Shift-IR		
Loop5	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 0000 (Disable)
37	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 1 (Disable MSB)
38	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
39	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	
40	TMS = 1, TCK = ↑	Select DR-Scan		
41	TMS = 1, TCK = ↑	Select IR-Scan		
42	TMS = 1, TCK = ↑	Test-Logic/Reset	One negative edge clock	
43	TMS = 1,	Test-Logic/Reset	In user mode	DONE

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

XPLA3 256 MACROCELL DEVICE PROGRAMMING EXAMPLE

Blank_Check

The Blank_Check command verifies that the entire EEPROM array has been erased.

Blank_Check Command Flow

Command	Sequence
Blank_Check	<ol style="list-style-type: none"> 1. ensure device is in Test-Logic/Reset state 2. shift in the ENABLE instruction 3. 3. shift in the VERIFY instructions in the address of the EEPROM row being verified. 4. Pause 20us to allow voltages to settle 5. execute the command (this transfers the row data into the ISP Shift Register) 6. shift out the data from the ISP Shift Register 7. compare the shifted-out data to the expected data 8. Repeat step 3 though 7 until all EEPROM rows have been checked 9. shift in the INIT instruction 10. execute the instruction (activate the contents of the EEPROM array) 11. shift in the DISABLE instruction 12. execute the instruction (activate the contents of the EEPROM array)

Blank_Check Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
Loop0	TMS = 1, TCK = \uparrow	Test-Logic/Reset	Ensure device in Test-Logic/Reset	Loop 5 times
1	TMS = 0, TCK = \uparrow	Run-Test/Idle		
2	TMS = 1, TCK = \uparrow	Select DR-Scan		
3	TMS = 1, TCK = \uparrow	Select IR-Scan		
4	TMS = 0, TCK = \uparrow	Capture-IR		
5	TMS = 0, TCK = \uparrow	Shift-IR		
Loop1	TMS = 0, TCK = \uparrow	Shift-IR	Shift in instruction bits (0-3)	TDI = 1001 (Enable)
6	TMS = 1, TCK = \uparrow	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Enable MSB)
7	TMS = 1, TCK = \uparrow	Update-IR	Load the Instruction Register ;	
8	TMS = 1, TCK = \uparrow	Select DR-Scan		
9	TMS = 1, TCK = \uparrow	Select IR-Scan		
10	TMS = 0, TCK = \uparrow	Capture-IR		
11	TMS = 0, TCK = \uparrow	Shift-IR		
Loop2	TMS = 0, TCK = \uparrow	Shift-IR	Shift in instruction bit (0-3)	TDI = 0011 (Verify)
12	TMS = 1, TCK = \uparrow	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Verify MSB)
13	TMS = 1, TCK = \uparrow	Update-IR	Load the Instruction Register	
14	TMS = 1, TCK = \uparrow	Select DR-Scan		
15	TMS = 0, TCK = \uparrow	Capture-DR		
16	TMS = 0, TCK = \uparrow	Shift-DR		
Loop4	TMS = 0, TCK = \uparrow	Shift-DR	Shift first address bits (8-1)	TDI = address (MSB, ...)
17	TMS = 1, TCK = \uparrow	Exit1-DR	Shift first address bit 0	TDI = address (LSB)
Loop3	TMS = 0, TCK = \uparrow	Pause-DR	Pause to allow voltages to settle	Loop for 20us
Loop3	TMS = 1, TCK = \uparrow	Exit2-DR	Load address in Address Latch	
Loop3	TMS = 1, TCK = \uparrow	Update-DR	Load the Shift Register.	
Loop3	TMS = 0, TCK = \uparrow	Run-Test/Idle		
Loop3	TMS = 1, TCK = \uparrow	Select DR-Scan		
Loop3	TMS = 0, TCK = \uparrow	Capture-DR		
Loop3	TMS = 0, TCK = \uparrow	Shift-DR	Shift out data bit 303	TD0 = data bit 303; TDI=1
Loop5	TMS = 0, TCK = \uparrow	Shift-DR	Shift out data bits (302 - 0)	TD0 = data bits (302-0);TDI=1

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Blank_Check Detailed Algorithm

Loop5	TMS = 0, TCK = ↑	Shift-DR	Shift in next address bits (8-1)	
Loop3	TMS = 1, TCK = ↑	Exit1-DR	Shift in next address bit 0	Compare Data
18	Execute loop3 until all addresses have been loaded. Load dummy address after last data read.			
19	TMS = 0, TCK = ↑	Pause-DR		
20	TMS = 1, TCK = ↑	Exit2-DR		
21	TMS = 1, TCK = ↑	Update-DR		
22	TMS = 0, TCK = ↑	Run-Test/Idle		
23	TMS = 1, TCK = ↑	Select DR-Scan		
24	TMS = 1, TCK = ↑	Select IR-Scan		
25	TMS = 0, TCK = ↑	Capture-IR		
26	TMS = 0, TCK = ↑	Shift-IR		
Loop4	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1011 (Init)
27	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Init MSB)
28	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
29	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	Loop for 200us
30	TMS = 1, TCK = ↑	Select DR-Scan		
31	TMS = 1, TCK = ↑	Select IR-Scan		
32	TMS = 0, TCK = ↑	Capture-IR		
33	TMS = 0, TCK = ↑	Shift-IR		
Loop5	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 0000 (Disable)
34	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 1 (Disable MSB)
35	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
36	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	
37	TMS = 1, TCK = ↑	Select DR-Scan		
38	TMS = 1, TCK = ↑	Select IR-Scan		
39	TMS = 1, TCK = ↑	Test-Logic/Reset	One negative edge clock	
40	TMS = 1,	Test-Logic/Reset	In user mode	DONE

XPLA3 256 MACROCELL DEVICE PROGRAMMING EXAMPLE

Program

The Program command programs the user's data into the EEPROM array.

Program Command Sequence

Command	Sequence
Program	<ol style="list-style-type: none"> 1. Ensure device is in Test-Logic/Reset state 2. shift in the ENABLE instruction 3. shift in the PROGRAM instruction 4. shift in the address and data for the EEPROM row being programmed. 5. execute the command (Program the data into the selected EEPROM row) 6. Repeat steps 4 and 6 until all EEPROM rows have been programmed 7. shift in the INIT instruction 8. execute the instruction (activate the contents of the EEPROM array) 9. shift in the DISABLE instruction 10. execute the instruction (activate the contents of the EEPROM array)

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Program Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
Loop0	TMS = 1, TCK = ↑	Test-Logic/Reset	Ensure device in Test-Logic/Reset State	Loop 5 times
1	TMS = 0, TCK = ↑	Run-Test/Idle		
2	TMS = 1, TCK = ↑	Select DR-Scan		
3	TMS = 1, TCK = ↑	Select IR-Scan		
4	TMS = 0, TCK = ↑	Capture-IR		
5	TMS = 0, TCK = ↑	Shift-IR		
Loop1	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1001 (Enable)
6	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Enable MSB)
7	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register; Set Enable Flip-flop	
8	TMS = 1, TCK = ↑	Select DR-Scan		
9	TMS = 1, TCK = ↑	Select IR-Scan		
10	TMS = 0, TCK = ↑	Capture-IR		
11	TMS = 0, TCK = ↑	Shift-IR		
Loop2	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1101 (Program)
12	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Program MSB)
13	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
Loop3	TMS = 1, TCK = ↑	Select DR-Scan		
Loop3	TMS = 0, TCK = ↑	Capture-DR		
Loop3	TMS = 0, TCK = ↑	Shift-DR		
Loop4	TMS = 0, TCK = ↑	Shift-DR	Shift in Data bits 303-0	TDI = data bits (303 - 0)
Loop5	TMS = 0, TCK = ↑	Shift-DR	Shift in Address bit 8-1	TDI = address bits (8-1)
Loop3	TMS = 1, TCK = ↑	Exit1-DR	Shift in Address bit 0	TDI = address bit 0 (LSB)
Loop3	TMS = 0, TCK = ↑	Pause-DR	Wait for voltages to settle	Loop for 20 us
Loop3	TMS = 1, TCK = ↑	Exit2-DR		
Loop3	TMS = 1, TCK = ↑	Update-DR		
Loop3	TMS = 0, TCK = ↑	Run-Test/Idle	Program data in EEPROM	Wait 10 ms.
Execute loop3 418 times to PROGRAM the entire device.				
14	TMS = 1, TCK = ↑	Select DR-Scan		
15	TMS = 1, TCK = ↑	Select IR-Scan		
16	TMS = 0, TCK = ↑	Capture-IR		
17	TMS = 0, TCK = ↑	Shift-IR		
Loop4	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1011 (Init)
18	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Init MSB)
19	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
20	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	Loop for 200 us
21	TMS = 1, TCK = ↑	Select DR-Scan		
22	TMS = 1, TCK = ↑	Select IR-Scan		
23	TMS = 0, TCK = ↑	Capture-IR		
24	TMS = 0, TCK = ↑	Shift-IR		
Loop5	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 0000 (Disable)
25	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 1 (Disable MSB)
26	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
27	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	
28	TMS = 1, TCK = ↑	Select DR-Scan		
29	TMS = 1, TCK = ↑	Select IR-Scan		
30	TMS = 1, TCK = ↑	Test-Logic/Reset	One negative edge clock	
31	TMS = 1,	Test-Logic/Reset	In user mode	DONE

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

XPLA3 256 MACROCELL DEVICE PROGRAMMING EXAMPLE

Verify

The Verify command verifies that the user's data in the EEPROM array matches the data contained in the JEDEC file.

Verify Command Sequence

Command	Sequence
Verify	<ol style="list-style-type: none"> 1. ensure device is in Test-Logic/Reset state 2. shift in the ENABLE instruction 3. shift in the VERIFY instruction 4. shift in the address of the EEPROM row being verified. 5. Pause 20us for voltages to settle 6. execute the command (this transfers the row data into the ISP Shift Register) 7. shift out the data from the ISP Shift Register 8. compare the shifted-out data to the expected data 9. Repeat step 4 though 8 until all EEPROM rows have been verified 10. shift in the INIT instruction 11. execute the instruction (activate the contents of the EEPROM array) 12. shift in the DISABLE instruction 13. execute the instruction (activate the contents of the EEPROM array)

Verify Command Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
Loop0	TMS = 1, TCK = ↑	Test-Logic/Reset	Ensure device in Test-Logic/Reset	Loop 5 times
1	TMS = 0, TCK = ↑	Run-Test/Idle		
2	TMS = 1, TCK = ↑	Select DR-Scan		
3	TMS = 1, TCK = ↑	Select IR-Scan		
4	TMS = 0, TCK = ↑	Capture-IR		
5	TMS = 0, TCK = ↑	Shift-IR		
Loop1	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1001 (Enable)
6	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Enable MSB)
7	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register ; Set enable flip-flop	
8	TMS = 1, TCK = ↑	Select DR-Scan		
9	TMS = 1, TCK = ↑	Select IR-Scan		
10	TMS = 0, TCK = ↑	Capture-IR		
11	TMS = 0, TCK = ↑	Shift-IR		
Loop2	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bit (0-3)	TDI = 0011 (Verify)
12	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Verify MSB)
13	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
14	TMS = 1, TCK = ↑	Select DR-Scan		
15	TMS = 0, TCK = ↑	Capture-DR		
16	TMS = 0, TCK = ↑	Shift-DR		
Loop4	TMS = 0, TCK = ↑	Shift-DR	Shift first address bits (8-1)	TDI = address (MSB, ...)
17	TMS = 1, TCK = ↑	Exit1-DR	Shift first address bit 0	TDI = address (LSB)
Loop3	TMS = 0, TCK = ↑	Pause-DR	Pause to allow voltages to settle	Loop for 20us
Loop3	TMS = 1, TCK = ↑	Exit2-DR	Load address in Address Latch	
Loop3	TMS = 1, TCK = ↑	Update-DR	Load the Shift Register.	

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Loop3	TMS = 0, TCK = ↑	Run-Test/Idle	
Loop3	TMS = 1, TCK = ↑	Select DR-Scan	
Loop3	TMS = 0, TCK = ↑	Capture-DR	

Verify Command Detailed Algorithm

Loop3	TMS = 0, TCK = ↑	Shift-DR	Shift out data bit 303	TD0 = data bit 303; TDI=1
Loop5	TMS = 0, TCK = ↑	Shift-DR	Shift out data bits (302 - 0)	TD0 = data bits (302-0);TDI=1
Loop5	TMS = 0, TCK = ↑	Shift-DR	Shift in next address bits (8-1)	
Loop3	TMS = 1, TCK = ↑	Exit1-DR	Shift in next address bit 0	Compare Data
17	Execute loop3 until all addresses have been loaded. Load dummy address after last data read.			
18	TMS = 0, TCK = ↑	Pause-DR		
20	TMS = 1, TCK = ↑	Exit2-DR		
21	TMS = 1, TCK = ↑	Update-DR		
22	TMS = 0, TCK = ↑	Run-Test/Idle		
23	TMS = 1, TCK = ↑	Select DR-Scan		
24	TMS = 1, TCK = ↑	Select IR-Scan		
25	TMS = 0, TCK = ↑	Capture-IR		
26	TMS = 0, TCK = ↑	Shift-IR		
Loop4	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1011 (Init)
27	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Init MSB)
28	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
29	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	Loop for 200 us
30	TMS = 1, TCK = ↑	Select DR-Scan		
31	TMS = 1, TCK = ↑	Select IR-Scan		
32	TMS = 0, TCK = ↑	Capture-IR		
33	TMS = 0, TCK = ↑	Shift-IR		
Loop5	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 0000 (Disable)
34	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 1 (Disable MSB)
35	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
36	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	
37	TMS = 1, TCK = ↑	Select DR-Scan		
38	TMS = 1, TCK = ↑	Select IR-Scan		
39	TMS = 1, TCK = ↑	Test-Logic/Reset	One negative edge clock	
40	TMS = 1,	Test-Logic/Reset	In user mode	DONE

XPLA3 256 MACROCELL DEVICE PROGRAMMING EXAMPLE

Pr_Security

The Pr_Security command programs the security cell of the device.

Pr_Security Command Sequence

Command	Sequence
Pr_Security	<ol style="list-style-type: none"> 1. Ensure device is in the Test-Logic/Reset state 2. shift in the ENABLE instruction 3. shift in the PROGRAM instruction 4. shift in the address of the EEPROM row containing the security bit and shift in the data with the corresponding security bit set to the programming state and the other bits set to the non-programming state. 5. execute the command (Program the data into the selected EEPROM row) 6. shift in the INIT instruction 7. execute the command (Activate the security bit) 8. shift in the DISABLE instruction

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

9. execute the instruction

Program Security Bit Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
Loop0	TMS = 1, TCK = ↑	Test-Logic/Reset	Ensure device in Test-Logic/Reset State	Loop 5 times
1	TMS = 0, TCK = ↑	Run-Test/Idle		
2	TMS = 1, TCK = ↑	Select DR-Scan		
3	TMS = 1, TCK = ↑	Select IR-Scan		
4	TMS = 0, TCK = ↑	Capture-IR		
5	TMS = 0, TCK = ↑	Shift-IR		
Loop1	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1001 (Enable)
6	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Enable MSB)
7	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register; Set Enable Flip-flop	
8	TMS = 1, TCK = ↑	Select DR-Scan		
9	TMS = 1, TCK = ↑	Select IR-Scan		
10	TMS = 0, TCK = ↑	Capture-IR		
11	TMS = 0, TCK = ↑	Shift-IR		
Loop2	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1101 (Program)
12	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Program MSB)
13	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
14	TMS = 1, TCK = ↑	Select DR-Scan		
15	TMS = 0, TCK = ↑	Capture-DR		
16	TMS = 0, TCK = ↑	Shift-DR		
Loop3	TMS = 0, TCK = ↑	Shift-DR	Shift in Data bits 303-0	TDI = data bits (303 - 0)
Loop4	TMS = 0, TCK = ↑	Shift-DR	Shift in Address bit 8-1	TDI = address bits (8-1)
17	TMS = 1, TCK = ↑	Exit1-DR	Shift in Address bit 0	TDI = address bit 0 (LSB)
18	TMS = 0, TCK = ↑	Pause-DR	Wait for voltages to settle	Loop for 20 us
19	TMS = 1, TCK = ↑	Exit2-DR		
20	TMS = 1, TCK = ↑	Update-DR		
21	TMS = 0, TCK = ↑	Run-Test/Idle	Program data in EEPROM	Wait 10 ms.
22	TMS = 1, TCK = ↑	Select DR-Scan		
23	TMS = 1, TCK = ↑	Select IR-Scan		
24	TMS = 0, TCK = ↑	Capture-IR		
25	TMS = 0, TCK = ↑	Shift-IR		
Loop5	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1011 (Init)
26	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Init MSB)
27	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
28	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	Loop for 200 us
29	TMS = 1, TCK = ↑	Select DR-Scan		
30	TMS = 1, TCK = ↑	Select IR-Scan		
31	TMS = 0, TCK = ↑	Capture-IR		
32	TMS = 0, TCK = ↑	Shift-IR		
Loop6	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 0000 (Disable)
33	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 1 (Disable MSB)
34	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
35	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	
36	TMS = 1, TCK = ↑	Select DR-Scan		
37	TMS = 1, TCK = ↑	Select IR-Scan		

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

38	TMS = 1, TCK = \uparrow	Test-Logic/Reset	One negative edge clock	
39	TMS = 1,	Test-Logic/Reset	In user mode	DONE

XPLA3 256 MACROCELL DEVICE PROGRAMMING EXAMPLE

Rd_Security

The Rd_Security command reads the security bit of the device.

Read Security Bit Command Sequence

Command	Sequence
Rd_Security	<ol style="list-style-type: none"> 1. Ensure device is in Test-Logic/Reset state 2. shift in the ENABLE instruction 3. shift in the VERIFY instruction 4. shift in the 304 data bits (all 0's) and illegal EEPROM row address 0xFF. 5. Pause for voltages to settle. 6. execute the command 7. shift out the data from the ISP Shift Register (data = 0 \rightarrow device secure, data = 1 \rightarrow device not secure) 8. shift in the INIT instruction 9. execute the command 10. shift in the DISABLE instruction 11. execute the instruction

Read Security Bit Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
Loop0	TMS = 1, TCK = \uparrow	Test-Logic/Reset	Ensure device in Test-Logic/Reset State	Loop 5 times
1	TMS = 0, TCK = \uparrow	Run-Test/Idle		
2	TMS = 1, TCK = \uparrow	Select DR-Scan		
3	TMS = 1, TCK = \uparrow	Select IR-Scan		
4	TMS = 0, TCK = \uparrow	Capture-IR		
5	TMS = 0, TCK = \uparrow	Shift-IR		
Loop1	TMS = 0, TCK = \uparrow	Shift-IR	Shift in instruction bits (0-3)	TDI = 1001 (Enable)
6	TMS = 1, TCK = \uparrow	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Enable MSB)
7	TMS = 1, TCK = \uparrow	Update-IR	Load the Instruction Register ; Set Enable Flip-flop	
8	TMS = 1, TCK = \uparrow	Select DR-Scan		
9	TMS = 1, TCK = \uparrow	Select IR-Scan		
10	TMS = 0, TCK = \uparrow	Capture-IR		
11	TMS = 0, TCK = \uparrow	Shift-IR		
Loop2	TMS = 0, TCK = \uparrow	Shift-IR	Shift in instruction bits (0-3)	TDI = 0011 (Verify LSB)
12	TMS = 1, TCK = \uparrow	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Verify MSB)
13	TMS = 1, TCK = \uparrow	Update-IR	Load the Instruction Register	
14	TMS = 1, TCK = \uparrow	Select DR-Scan		
15	TMS = 0, TCK = \uparrow	Capture-DR		
16	TMS = 0, TCK = \uparrow	Shift-DR		
Loop3	TMS = 0, TCK = \uparrow	Shift-DR	Shift in data bits (303-0)	TDI = All data bits = 0's
Loop4	TMS = 0, TCK = \uparrow	Shift-DR	Shift in address bits (8-1)	TDI = 11111111 (MSB,...)
17	TMS = 1, TCK = \uparrow	Exit1-DR	Shift in address bit 0	TDI = 1 (LSB)
18	TMS = 0, TCK = \uparrow	Pause-DR	Pause for voltages to settle	Loop for 20us

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

19	TMS = 1, TCK = ↑	Exit2-DR	Load address in Address Latch	
20	TMS = 1, TCK = ↑	Update-DR	Load the Shift Register.	
21	TMS = 0, TCK = ↑	Run-Test/Idle		
22	TMS = 1, TCK = ↑	Select DR-Scan		
23	TMS = 0, TCK = ↑	Capture-DR		
Loop5	TMS = 0, TCK = ↑	Shift-DR	Shift out data bit 303	TDO = 0 → device secure
24	TMS = 1, TCK = ↑	Exit1-DR		
25	TMS = 0, TCK = ↑	Pause-DR		
26	TMS = 1, TCK = ↑	Exit2-DR		
27	TMS = 1, TCK = ↑	Update-DR		

Read Security Bit Detailed Algorithm

28	TMS = 1, TCK = ↑	Select DR-Scan		
29	TMS = 1, TCK = ↑	Select IR-Scan		
30	TMS = 0, TCK = ↑	Capture-IR		
31	TMS = 0, TCK = ↑	Shift-IR		
Loop6	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 1011 (Init)
32	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 0 (Init MSB)
33	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
34	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	Loop for 200 us
35	TMS = 1, TCK = ↑	Select DR-Scan		
36	TMS = 1, TCK = ↑	Select IR-Scan		
37	TMS = 0, TCK = ↑	Capture-IR		
38	TMS = 0, TCK = ↑	Shift-IR		
Loop7	TMS = 0, TCK = ↑	Shift-IR	Shift in instruction bits (0-3)	TDI = 0000 (Disable)
39	TMS = 1, TCK = ↑	Exit1-IR	Shift in instruction bit 4	TDI = 1 (Disable MSB)
40	TMS = 1, TCK = ↑	Update-IR	Load the Instruction Register	
41	TMS = 0, TCK = ↑	Run-Test/Idle	Initialize device with new program data	
42	TMS = 1, TCK = ↑	Select DR-Scan		
43	TMS = 1, TCK = ↑	Select IR-Scan		
44	TMS = 1, TCK = ↑	Test-Logic/Reset	One negative edge clock	
45	TMS = 1,	Test-Logic/Reset	In user mode	DONE

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

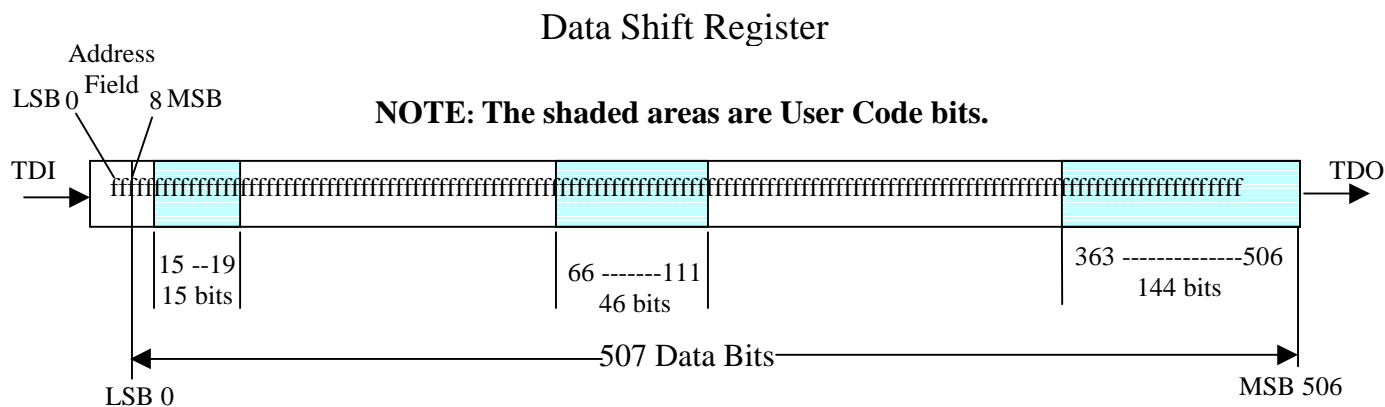
CoolRunner XPLA3 FAMILY

XPLA3 User Code defined

XPLA3 User Codes						
	32XL	64XL	128XL	256XL	384XL	512XL
User Code Address	53L 0101111 53U 1101111	105L 01011101 105U 11011101	105L 01011101 105U 11011101	209L 010101011 209U 110101011	209L 010101011 209U 110101011	209L 010101011 209U 110101011
#.of Addr. bits	7	8	8	9	9	9
# of User Code bits	53L, 53U Total=106	53L, 53U Total=106	138L, 138U Total=278	157L, 157U Total=314	222L, 222U Total=444	388L, 388U Total=766
User Code Locations	5 - 9, 66 - 113	5-9, 75 -122	5 - 19, 47 - 73, 170 - 265	5 - 19, 66 - 111, 208 - 303	15 - 29, 156 - 218, 363 - 506	5 - 19, 103 - 185, 282-377, 383 -397, 481- 563, 660 - 756
Data Reg. Length	114 bits	123 bits	266 bits	304 bits	507 bits	755 bits

Example is 384XL

NOTE: There are 2 addresses for USERCODE storage, Upper and Lower address.



NOTE: When Reading the User Code, the first bit out of TDO is the User Code MSB

0000 1001 1101 0111 1111 1111 1111 0100 0001 0100 0011 1111 1111

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Example: Programming a UserCode in 384XL device.

Program the UserCode Row just like any other row: ISC_ENABLE must be loaded before any other ISC instructions can be executed.

Usercode in text ABCDEFGHIH

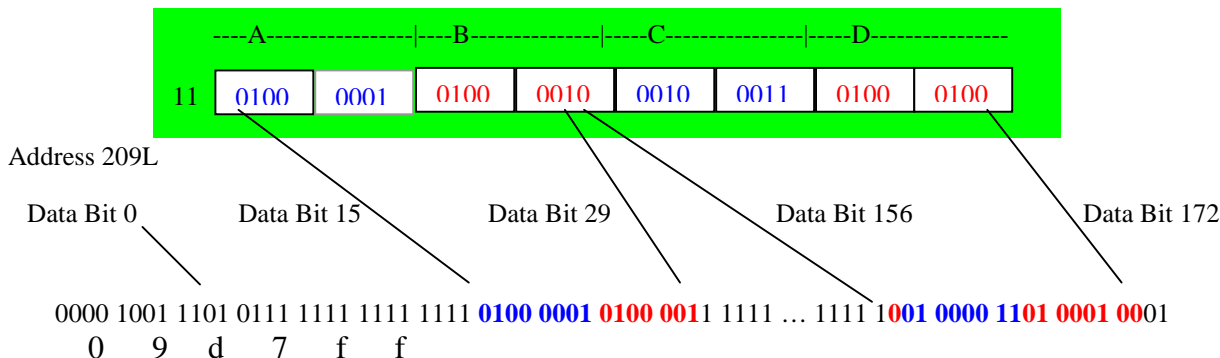
Ascii converted data 0x41 0x42 0x43 0x44 0x45 0x46 0x47 0x48

Usercode In Binary 01100101 01100110 01100111 01101000 01101001 01101010 01101011 0110 1100

Usercode Location

From Fuse Map file 506, 505, 504, 503, 502, 501, 474. In Address 209L

The Fuse Map for this family is available in Excel Spead Sheet files.



ScanDR TDI 09d7fff4143ffffffffffffffffffffffffffffffff90d1115191d2083ffffff...ff TDO

9 bits Address, + 507 bits of data

Procedure to set usercode bits in
UserCode in Xpla3 devices is specified in text. Before it is programmed it needs to be converted to its binary equivalent.

- Step1: Convert usercode from text to its Ascii value and then to Binary.
 - Step2: Get Usercode row address and Bit locations from map file.
 - Step3: Convert usercoderow address to Grey code. Set first nine bits to the usercode row address.
 - Step4: set the Data bits between valid USERCODE bits in the above example to 1).
 - Step5: Overlay usercode bits at the locations specified in the map file (bits 506-474 in the above example).
- The usercode data can then be programmed to the device as described in the spec. under Row Programming.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

JTAG Instructions

The JTAG commands supported by the ISP PC Parallel Port Programmer are described in the following subsections. These commands are basic JTAG commands which are required by the ISP programmer to control multiple JTAG/ISP devices in a JTAG chain.

Bypass

The Bypass command passes data from TDI to TDO with a one half clock cycle delay. The outputs of the device are not affected by this operation.

BYPASS Command Sequence

Command	Sequence
BYPASS	1. shift in the BYPASS instruction 2. shift in/out data while in the DR-Shift TAP Controller State

BYPASS Detailed Algorithm

Step	Transition Conditions	TAP State	CPLD Event Description	Programmer Action
0	TMS = 1	Test-Logic/Reset	BEGIN	BEGIN
loop0	TMS = 1, TCK = \uparrow	Test-Logic/Reset	Ensure device in Test-Logic/Reset State	Loop 5 times
1	TMS = 0, TCK = \uparrow	Run-Test/Idle		
2	TMS = 1, TCK = \uparrow	Select DR-Scan		
3	TMS = 1, TCK = \uparrow	Select IR-Scan		
4	TMS = 0, TCK = \uparrow	Capture-IR		
5	TMS = 0, TCK = \uparrow	Shift-IR		
loop1	TMS = 0, TCK = \uparrow	Shift-IR	Shift in instruction bits (0-3)	TDI = 1111 (BYPASS)

BYPASS Detailed Algorithm Continued

6	TMS = 1, TCK = \uparrow	Exit1-IR	Shift in instruction bit 4	TDI = 1 (BYPASS MSB)
7	TMS = 1, TCK = \uparrow	Update-IR	Load the Instruction Register	
8	TMS = 1, TCK = \uparrow	Select DR-Scan		
9	TMS = 0, TCK = \uparrow	Capture-DR		
10	TMS = 0, TCK = \uparrow	Shift-DR		
loop2	TMS = 0, TCK = \uparrow	Shift-DR	Shift in/out Data bits	TDI=TDO (1/2 TCK delay)
11	TMS = 1, TCK = \uparrow	Exit1-DR	Shift in/out last Data bit	TDI=TDO (1/2 TCK delay)
12	TMS = 1, TCK = \uparrow	Update-DR		
13	TMS = 1, TCK = \uparrow	Select DR-Scan		
14	TMS = 1, TCK = \uparrow	Select IR-Scan		
15	TMS = 1, TCK = \uparrow	Test-Logic/Reset		
	TMS = 1	Test-Logic/Reset	DONE	DONE

Please note that the device must remain in loop2, “Shift-DR State”, to remain in the BYPASS mode.

IDcode

The IDcode command reads the IDcode of the device. The outputs of the device are not affected by this operation.

XILINX PROGRAMMER QUALIFICATION SPECIFICATION

CoolRunner XPLA3 FAMILY

Added to Specification on April 5, 2000.
Information dated 12/23/99

The additional pin for JTAG port enabling (porten) is required to be grounded during the power-up cycle and permits enabling the JTAG port when the port had been reconfigured as I/Os. XPLA 3 devices are shipped with the JTAG port enabled. During device programming, the pins can be left as dedicated JTAG ports or reconfigured as normal I/O pins. If the JTAG ports are reconfigured as I/O pins the change takes effect upon execution of the ISP reinit command and with all subsequent power-up cycles. Note that reconfiguring the JTAG port pins as I/Os, makes these pins non-JTAG ISP functional; however, the porten pin can be used to reclaim these pins for ISP programming by applying Vdd to the porten pin. This forces the JTAG port pins to be functional for ISP programming; after completing the desired ISP function, bringing porten to grd re-establishes the JTAG port pins as I/O pins if programmed as I/Os. If the JTAG ports are configured during part programming as dedicated JTAG ports (i.e. not normal I/Os) then the porten pin has no effect. External circuitry must be compatible with this dual use of JTAG port pins.