

Course Description

Learn the tips and tricks of PCI designs in this two-day course. This course provides an introduction to basic PCI concepts and architecture and intensive training on designing with the Xilinx PCI core. This course emphasizes and illustrates how PCI transactions take place and gives you an overview of Xilinx PCI solutions. You will learn the basics of Xilinx PCI cores including PCI 64/66 and PCI 32. You will also learn design concepts and basic verification strategies for creating a PCI system design. The labs cover basic transaction analysis with the ModelSim™ simulator and the general design flow, from core to verification, with ISE 6.3i.

Level – Intermediate

Course Duration – 2 days

Course Part Number – PCI28000-6.3-ILT

Who Should Attend? – Engineers who are interested in Xilinx PCI products and who want to maximize their productivity

Prerequisites

- Some knowledge of PCI
- Working experience with digital design
- Basic knowledge of Verilog or VHDL
- Experience with either Xilinx Alliance Series™ or Foundation™ ISE software tools

Software Tools

- ISE 6.3i
- ModelSim 5.8c

After completing this comprehensive training, you will have the necessary skills to:

- Describe the basics of the PCI specification
- Select the appropriate PCI solution for a specific application
- Describe the basic LogiCORE™ PCI design flow
- Use available product documentation to successfully complete a LogiCORE PCI user application, including configuration, logic design, implementation, and verification

Course Outline

Day 1

- Introduction
- PCI Local Bus Architecture
- PCI Signals
- Basic Bus Operations: Transactions, Decoding, and Wait States
- Basic Bus Operations: Target, Parity, and Arbitration
- PCI Addressing and Bus Commands
- PCI Configuration
- 64-Bit and 66-MHz PCI
- PCI Timing
- The LogiCORE PCI Solution
- Xilinx 32/33 and 64/66 LogiCORE PCI

Day 2

- User Application Interface for Target
- User Application Interface for Initiator
- Other User Interface Signals
- Practical Design of PCI Agents
- Xilinx PCI 64-Bit and 66 MHz
- Implementing the LogiCORE PCI
- Device-Specific Considerations
- **Lab 1:** Analyzing PCI Bus Transactions
- **Lab 2:** Synthesis and Implementation Using XST

Lab Descriptions

- **Lab 1:** Analyzing PCI Bus Transactions – This lab demonstrates typical PCI bus transactions and the signals associated with each type of bus transaction. The relationship between various signals is identified. Various settings are changed and the behaviors are analyzed after each change is made.
- **Lab 2:** Synthesis and Implementation Using XST – This lab demonstrates the Xilinx PCI design flow, from synthesis to an implementation targeted for a device that supports Xilinx PCI using ISE 6.3i software. The lab uses the example “Ping” design (included with the PCI Core) to target a Virtex-II™ FPGA. Similar steps can be followed for other device families.

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