

## Course Description

This course focuses on the PCI-X Addendum to the PCI Local Bus Specification and provides a detailed investigation into the operation of the PCI-X LogiCORE™ solution. Explaining the basic principles and concepts introduced by the PCI-X Addendum, this course also provides an in-depth understanding of the PCI-X LogiCORE solution and how a digital designer may interface this solution to a typical user application to create a flexible PCI-X system design.

**Level** – Intermediate

**Course Duration** – 2 days

**Course Part Number** –PCIX28000-6.3-ILT

**Who Should Attend?** – This course is beneficial to any digital designer tasked with designing a PCI-X system where overall time-to-market is an important factor. This course is also beneficial to any engineer with a general interest in learning about PCI-X and the Xilinx PCI-X solution.

### Prerequisites

- Experience with either VHDL or Verilog languages
- Familiar with the Xilinx software tools

### Software Tools

- Xilinx ISE™ 6.3
- Mentor Graphics ModelSim 6.0 (SE or PE)

After completing this comprehensive training, you will have the necessary skills to:

- Identify differences between PCI and PCI-X
- Describe the basics of the PCI-X specification
- Describe the basic Xilinx PCI-X design flow
- Identify LogiCORE PCI-X signals
- Understand the behavior of the PCI-X LogiCORE solution and how to interface it to a typical user application
- Design a user application that can accommodate operation in both conventional PCI and PCI-X mode

## Course Outline

### Day 1

- Course Agenda
- PCI-X Local Bus Architecture
- PCI-X Signals and Terminology
- Basic Bus Operations: Transactions, Decoding, and Wait States
- Basic Bus Operations: Terminations, Parity, and Arbitration
- PCI-X Modes
- PCI-X Addressing and Bus Commands
- PCI-X Configuration
- 64-Bit Transactions
- **Lab 1:** Analyzing PCI and PCI-X Transactions

### Day 2

- The LogiCORE PCI-X Solution
- Xilinx LogiCORE PCI-X
- User Application Interface for Target
- User Application Interface for Initiator
- Design Considerations in LogiCORE PCI-X
- Designing Target Agent Using LogiCORE PCI-X
- Designing Initiator Agent Using LogiCORE PCI-X
- Implementing the LogiCORE PCI-X
- **Lab 2:** Analyzing PCI-X Bus Transactions
- **Lab 3:** Synthesis and Implementation Using XST

### Lab Descriptions

- **Lab 1:** Analyzing PCI and PCI-X Transactions – This lab introduces you to the PCI and PCI-X protocol and their typical transactions. The simulation will show different aspects of PCI and PCI-X transactions.
- **Lab 2:** Analyzing PCI-X Bus Transactions – This lab demonstrates typical PCI-X bus transactions and the signals associated with each type of bus transaction. The relationship between various signals is identified. Some settings are changed and the behaviors are analyzed after the change is made.
- **Lab 3:** Synthesis and Implementation Using XST – This lab demonstrates the Xilinx PCI-X design flow, from synthesis to an implementation targeted for a device that supports Xilinx PCI-X using ISE 6.3i SP1 software. The lab uses the simple transactions example design (included with the PCI-X Core) to target a Virtex™-II Pro device. Similar steps can be followed for other device families.

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