



CPLD Problem Solver

Welcome to the CPLD Debug Guide

Select your problem(s) below.

Select a Decision Tree below to help find your answers.

[I have a CPLD fitting problem.](#)

[The design doesn't work on my board.](#)

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How do I resolve a CPLD fitting problem?

Do you have the latest version of Xilinx software with all service packs installed?

Description

Service packs may be downloaded at:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp?iLanguageID=1&sGlobalNavPick=SUPPORT&sSecondaryNavPick=DOWNLOAD

WebPACK may be downloaded at:

<http://www.xilinx.com/webpack>

Action

Before continuing, ensure that you have the most recent service pack/WebPACK installed.

Is your design still not fitting after reimplementing with the latest version of software?

[Yes](#)

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Does the I/O needed by your design exceed the I/O available for your device/package combination?

Action

Please check the relevant [data sheet](#) to ensure that the device/package combination you are using contains enough pins.

Sample error message:

Insufficient number of input pins

Yes – See [AR #9150](#)

[No](#)

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Does the number of macrocells needed by your design exceed the number of macrocells in your selected device?

Description

The number of macrocells in each device is given in the device name, after the 95 for a 9500 family device, or after the 3 for a CoolRunner family device. For example: An XC9572XL has 72 macrocells. An XCR3032XL has 32 macrocells.

Sample error message:

Error: Insufficient number of macrocells: needs at least XX but only YY left after allocating other resources.

Device XC95ZZ was disqualified

Action

Does the number of macrocells needed by your design exceed the number of macrocells in your selected device?

Yes – See [AR # 9152](#)

[No](#)

[Return to start.](#)

Does the number of product terms needed by your design exceed the number of product terms available in your selected device?

Description

The 9500 family devices have 5 product terms per macrocell. An XC95144XL device has 144 macrocells so it has $144 * 5 = 720$ product terms.

The CoolRunner XPLA3 family devices have 48 product terms per function block (16 macrocells). An XCR3032XL device has 32 macrocells so it has two function blocks. $2 * 48 = 96$ product terms.

The CoolRunner-II family devices have 56 product terms per function block (16 macrocells). An XC2C64 device has 64 macrocells so it has 4 function blocks. $4 * 56 = 224$ product terms.

Sample error message:

Insufficient number of product terms: needs at least 194 but only 180 left after allocating other resources.

Action

Does the number of product terms needed by your design exceed the number of product terms available in your selected device?

Yes – See [AR# 9924](#)

[No](#)

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Have you locked any logic to a specific pin or macrocell?

[Yes](#)

[No](#)

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Disable physical location constraints. Does the design fit now?

Description

In the implementation options, release all pinlocks by going to:
Implementation Options -> Basic Tab -> Use Location Constraints -> *Never*
Refit the design.

Action

Does the design fit now?

Yes – See [AR #13605](#)

No

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Are there timing constraints on your design?

[Yes](#)

[No](#)

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Release timing constraints and refit the design. Does it fit now?

Description

In the implementation options, you can disable timing constraints without having to edit your UCF or design. In the implementation options, under the Basic tab, deselect *Use Timing Constraints*.

Action

Does the design fit now?

Yes – [AR #13606](#)

[No](#)

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Webcase

Please submit a WebCase to Xilinx Technical Support with the following information:

1. Whether the number of I/O used in the design is less than the total I/O available for device/speedgrade/package
2. Whether the registers + combinatorial output are less than total macrocells available for device (1 x macrocell = 1 x register)
3. If there are any timing constraints present but disabled in the UCF file
4. If there are any physical location constraints not present or disabled in the UCF file
5. If the design will not fit, any third-party vendor software used (*e.g.*, Synplicity), and version

Also, be prepared to submit the actual design files for analysis.

[Click here to begin a webcase.](#)

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Does the design pass timing simulation?

Description

It is strongly recommended that you use the latest version of software (including service packs) when doing fitting and timing simulation.

Service packs can be downloaded at:

http://www.support.xilinx.com/support/techsup/sw_updates

Timing simulation will show many timing problems that may arise from the way a design was fit into the device. During fitting, some logic may end up being partitioned into multiple levels of logic (either for purposes of sharing logic, or to get a design to fit) and, as a result, require more logic delays than expected.

Action

Does your design pass timing simulation?

[Yes, the design passes timing simulation](#)

[No, the design does not pass timing simulation](#)

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Does the device Verify correctly?

Description

A Verify instruction can be done using JTAG or through a hardware programmer (such as an HW-130, BP Microsystems, Data I/O, etc.). The purpose of this is to see whether the data programmed into the CPLD matches the data in the JEDEC.

Action

Does the device Verify?

[Yes, device passes Verify](#)

No, device fails Verify – [See AR #13611](#)

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Is the entire part unresponsive or is only part of the design not functioning?

Description

If the device does not respond to *any* input, it is likely that this part has been damaged. Select *part damaged*.

If the device has any outputs toggling, whether they are what you expect or not, select *design non-functional*.

Action

Part damaged – [Please see the RMA procedure / policy](#)

[Design nonfunctional](#)

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Do the outputs function if assigned to other pins?

Description

In your design, route the output(s) in question to an additional pin and probe that pin to see if it functions properly at that different location.

Example:

```
//Original design - dout not functioning properly
```

```
dout <= a and b;
```

```
//Modified design
```

```
dout <= a and b;
```

```
dout_test <= a and b;
```

Action

Does the output function on a different pin?

Yes, output is correct on a different pin. See [AR #13612](#)

No, output does not change on a different pin

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Are the inputs being seen properly by the CPLD?

Description

Are the inputs being recognized properly by the CPLD?

Action

Take the inputs to the equations in question and route them directly to output pins. Probe the outputs against the inputs to see if they are tracking correctly.

[Yes, inputs are being seen by the CPLD properly](#)

[No, inputs are not being seen by the CPLD properly](#)

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Is the problem caused by temperature?

Description

Speeds of CMOS devices are affected by operating temperature. A device at the cold end of the temperature range will run faster than the same device at the hot end of the temperature range.

Action

Try using cold spray and, conversely, a heat gun to see if temperature affects the design's functionality. Is there any effect?

Yes, the design is affected by temperature – [AR #13630](#)

[No, the design is not affected by temperature](#)

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Design not affected by temperature

Action

Try to remove as much of the design as possible, except the failing path, and save this as a separate project. Reimplement the design to ensure that the issue still exists. If it does, open a [Technical support case](#).

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Does the design pass functional simulation?

Description

Functional simulation can be considered a pure logic simulation. It is done prior to fitting/implementation so there are no timing delays considered (hence the naming difference of functional vs. timing simulation).

Action

Does the design pass functional simulation?

Yes, the design passes functional simulation - [AR # 13609](#)

No, the design does not pass functional simulation – [AR 13608](#)

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Inputs not seen by the CPLD.

Action

Ensure that the signal is entering the Xilinx CPLD. Verify that it:

1. Meets the data sheet V_{ih} and V_{il} specs (voltage minimum and maximum).
2. Has a fast and clean rise/fall time (ideally under 20ns).

Also consider the edge cases (voltage spikes during power-up/down) when observing these signals; it is possible that a voltage spike above the maximum voltage tolerance (V_{in}) has destroyed the I/O pin.

If all of these have been met, please open a [Technical Support Case](#).

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/16/05	1.0	Initial Xilinx release.