Designing with the Xilinx Analog Mixed Signal Solution

FPGA 3

FPGA34000-ILT (v1.0)

Course Specification

Course Description

This course introduces the Xilinx Analog Mixed Signal (AMS) solution and the appropriate tools and techniques for hardware engineers and analog engineers to utilize this solution. The complete front-to-back design flow is covered, including the evaluation of the Xilinx Analog-to-Digital Converter (XADC) block utilizing an evaluation board and the evaluator add-on card, the various ways to include the XADC in your design, XADC simulation of an analog input, viewing the digital output, and implementation. Additionally, labs are provided that support each topic, including the compete flow.

Level – FPGA 3

Course Duration – 1 day

Course Part Number – FPGA34000-ILT

Who Should Attend? – Hardware and analog designers who want to maximize utilization of the Xilinx AMS solution

Prerequisites

- *Essentials of FPGA Design*
- Basic VHDL or Verilog programming knowledge
- C programming knowledge recommended
- Experience with the Xilinx ISE and Embedded Development Kit (EDK) software tools

Software Tools

- Xilinx Vivado™ System Edition 2012.3 or Xilinx ISE® Design Suite: System Edition 14.3

Hardware

- Architecture: Xilinx 7 series FPGAs
- Demo boards: Kintex™-7 FPGA KC705 or Zynq™-7000 All Programmable SoC board and AMS evaluator card

* This course focuses on 7 series FPGA architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the basics of analog-to-digital converters (ADC)
- Describe the benefits of having a flexible analog interface (the XADC block) coupled with the programmable logic capability of 7 series FPGAs and the Zynq-7000 All Programmable SoC
- List the key specifications for the Xilinx Analog-to-Digital Converter block
- Identify the different flows for evaluating and adding the XADC core into your design using the ISE Design Suite tools

Course Outline

- AMS Overview
- ADC Theory
- XADC Architecture
- AMS Design Flow
- XADC Debug and Monitor
- **Lab 1:** Evaluating the XADC Block
- HDL Design Flow
- **Lab 2**: AMS HDL State Machine Control and Simulation
- EDK Design Flow
- **Lab 3**: EDK Design Flow
- Course Summary

Lab Descriptions

- **Lab 1:** Evaluating the XADC Block – Use the AMS TRD to evaluate the XADC performance, configure the XADC settings and view the sampled data using the Lab View GUI environment.
- **Lab 2:** AMS HDL State Machine Control and Simulation – Use the XADC wizard to generate an XADC core, instantiate the XADC core to a RTL project, and simulate and implement the design.
- **Lab 3:** EDK Design Flow – Use the EDK IP Catalog to add the XADC AXI IP core to the design, implement the design, and run a test application utilizing the XADC core.

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