How to Design a High-Speed Memory Interface
Connectivity 3

Course Specification

- Lab 1: MIG Core Generation
- MIG Design Simulation
- Lab 2: MIG Design Simulation

Day 2
- Memory Design Implementation
- Lab 3: MIG Design Implementation
- Memory Interface Test and Debugging
- Lab 4: MIG Design Debugging
- MIG in Embedded Designs
- Lab 5: MIG in IP Integrator
- Memory Interface Board-Level Design
- DDR3 PCB Simulation (optional)
- Lab 6: DDR3 Signal Integrity Simulation (optional)

Lab Descriptions

- Lab 1: MIG Core Generation — Create a DDR3 memory controller using the Memory Interface Generator (MIG) in the Vivado IP catalog. Customize the soft core memory controller for the board.
- Lab 2: MIG Design Simulation — Simulate the memory controller created in Lab 1 using the Vivado simulator or Mentor Graphics QuestaSim simulator.
- Lab 3: MIG Design Implementation — Implement the memory controller created in the previous labs. Modify constraints, synthesize, implement, create the bitstream, program the FPGA, and check the functionality.
- Lab 4: MIG Design Debugging — Debug the memory interface design utilizing the Vivado logic analyzer.
- Lab 5: MIG in IP Integrator — Use the block design editor to include the MIG IP in a given processor design.
- Lab 6: DDR3 Signal Integrity Analysis — Learn basic signal analysis options to check waveforms and design optimization (optional).

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