Course Description
This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

Level – DSP 3
Course Duration – 2 days
Course Part Number – DSP-SYSGENILT

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

Prerequisites
- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Software Tools
- Vivado® System Edition 2015.3
- MATLAB with Simulink software R2015b

Hardware
- Architecture: 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board and Zynq®-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the 7 series architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations. The ZC702 or ZedBoard is required for the “AXI4-Lite Interface Synthesis” lab.

After completing this comprehensive training, you will have the necessary skills to:
- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Run hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Implement multi-rate systems in System Generator
- Integrate System Generator models into the Vivado IDE
- Design a processor-controllable interface using System Generator for DSP
- Generate IPs from C-based design sources for use in the System Generator environment

Course Outline

Day 1
- Introduction to System Generator
- Simulink Software Basics
- Lab 1: Using the Simulink Software
- Basic Xilinx Design Capture
- Demo: System Generator Gateway Blocks
- Lab 2: Getting Started with Xilinx System Generator
- Signal Routing
- Lab 3: Signal Routing

Lab Descriptions

Lab 1: Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.

Lab 2: Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.

Lab 3: Signal Routing – Design padding and unpadding logic by using signal routing blocks.

Lab 4: Implementing System Control – Design an address generator circuit by using blocks and Mcode.

Lab 5: Designing a MAC-Based FIR Filter Design

Lab 6: Designing an FIR Filter Using the FIR Compiler Block

Lab 7: System Generator and Vivado IDE Integration

Lab 8: System Generator and Vivado HLS Tool Integration

Lab 9: AXI4-Lite Interface Synthesis

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